LM5037 Dual-Mode PWM Controller With Alternating Outputs

Check for Samples: LM5037

FEATURES

- **High Voltage (100V) Start-up Regulator**
- **Alternating Outputs for Double-ended Topologies**
- **Current-mode or Feed-forward Voltage-mode Control**
- **Programmable Maximum Duty Cycle Limit**
- **2% Feedback Reference Accuracy**
- **High Gain-bandwidth Error Amplifier**
- **Programmable Line Under-voltage Lockout (UVLO) with Adjustable Hysteresis**
- **Versatile Dual Mode Over-current Protection with Hiccup Delay Timer**
- **Programmable Soft-start**
- **Precision 5V Reference Output**
- **Current Sense Leading Edge Blanking**
- **Resistor Programmed 2 MHz Capable Oscillator**
- **Oscillator Synchronization Capability with Low Frequency Lockout Protection**

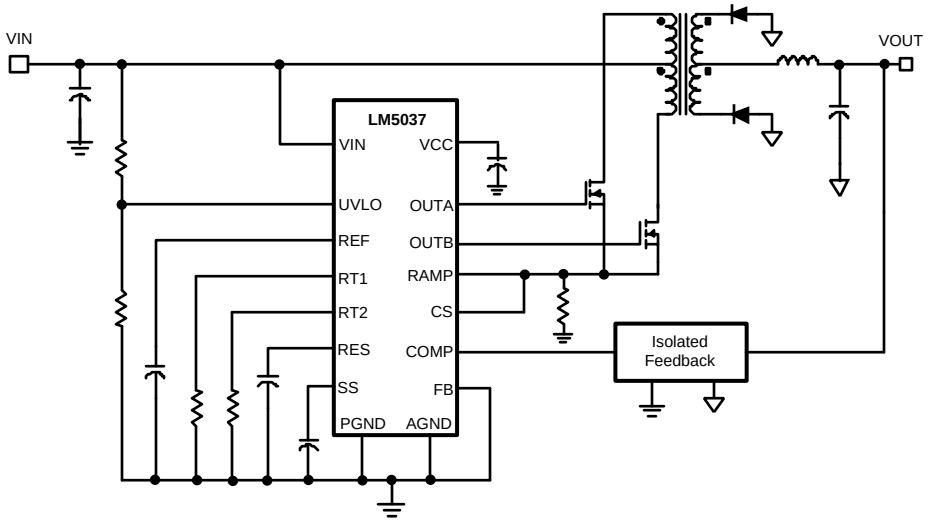
Package

- TSSOP-16

DESCRIPTION

The LM5037 PWM controller contains all the features necessary to implement balanced double-ended power converter topologies, such as push-pull, half-bridge and full-bridge. These double-ended topologies allow for higher efficiencies and greater power densities compared to common single-ended topologies such as the flyback and forward. The LM5037 can be configured for either voltage mode or current mode control with minimum external components. Two alternating gate drive outputs are provided, each capable of 1.2A peak output current. The LM5037 can be configured to operate directly from the input voltage rail over a wide range of 13V to 100V. Additional features include programmable maximum duty cycle limit, line under-voltage lockout, cycle-by-cycle current limit and a hiccup mode fault protection with adjustable timeout delay, soft-start and a 2 MHz capable oscillator with synchronization capability, precision reference and thermal shutdown.

Simplified Push-Pull Power Converter



Connection Diagram

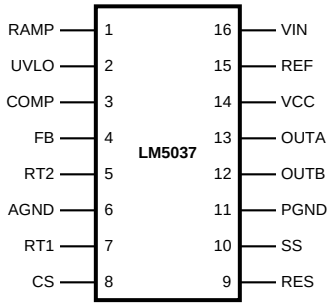


Figure 1. Top View
16-Lead TSSOP Package

Pin Descriptions

Pin	Name	Description	Application Information
1	RAMP	Pulse width modulator ramp	Modulation ramp for the PWM comparator. This ramp can be a representative of the primary current (current mode) or proportional to input voltage (feed-forward voltage mode). This pin is reset to ground at the conclusion of every cycle by an internal FET.
2	UVLO	Line under-voltage lockout	An external voltage divider from the power source sets the shutdown and standby comparator threshold levels. When UVLO exceeds the 0.45V shutdown threshold, the VCC and REF regulators are enabled. When UVLO exceeds the 1.25V standby threshold, the SS pin is released and the device enters the active mode.
3	COMP	Input to the pulse width modulator	Output of the error amplifier and input to the PWM comparator.
4	FB	Feedback	Connected to inverting input of the error amplifier. An internal 1.25V reference is connected to the non-inverting input of the error amplifier. In isolated applications using an external error amplifier, this pin should be connected to the AGND pin.
5	RT2	Oscillator dead-time control	The resistance connected between RT2 and AGND sets the forced dead-time between switching periods of the alternating outputs.
6	AGND	Analog ground	Connect directly to Power Ground.
7	RT1	Oscillator maximum on-time control	The resistance connected between RT1 and AGND sets the oscillator maximum on-time. The sum of this maximum on-time and the forced dead-time (set by RT2) sets the oscillator period.
8	CS	Current sense input	If CS exceeds 250 mV the output pulse will be terminated, entering cycle-by-cycle current limit. An internal switch holds CS low for 65 nS after either output switches high to blank leading edge transients.
9	RES	Restart timer	If cycle-by-cycle current limit is reached during any cycle, a 18 µA current is sourced to the external RES pin capacitor. If the RES capacitor voltage reaches 2.0V, the soft-start capacitor will be fully discharged and then released with a pull-up current of 1 uA. After the first output pulse (when SS = 1V), the SS pin charging current will increase to the normal level of 100 µA.
10	SS	Soft-start	An external capacitor and an internal 100uA current source set the soft-start ramp. The SS current source is reduced to 1 µA following a restart event (RES pin high).
11	PGND	Power ground	Connect directly to Analog Ground
12	OUTB	Output driver	Alternating gate drive output of the pulse width modulator. Capable of 1.2A peak source and sink current.
13	OUTA	Output driver	Alternating gate drive output of the pulse width modulator. Capable of 1.2A peak source and sink current.
14	VCC	Output of the high voltage start-up regulator. The VCC voltage is regulated to 7.7 V.	If an auxiliary winding raises the voltage on this pin above the regulation set point, the internal start-up regulator will shutdown thus reducing the IC power dissipation. Locally decouple VCC with a 0.47 µF or greater capacitor.
15	REF	Output of a 5V reference	Locally decouple with a 0.1 µF or greater capacitor. Maximum output current is 10 mA (typ).

Pin Descriptions (continued)

Pin	Name	Description	Application Information
16	VIN	Input voltage source	Input to the VCC Start-up regulator. Operating input range is 13V to 100V. For power sources outside of this range, the LM5037 can be biased directly at VCC by an external regulator.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

VIN to GND		-0.3V to 105V
VCC, OUTA, OUTB to GND		-0.3V to 16V
CS to GND		-0.3V to 1.0V
UVLO, FB, RT2, RT1, RAMP, SS, REF to GND COMP, RES (3)		-0.3V to 7V
ESD Rating(4)	Human Body Model	2kV
Storage Temperature Range		−65°C to + 150°C
Junction Temperature		150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) COMP, RES are output pins. As such, it is not recommended that external power sources be connected to these pins.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. 2kV for all pins.

Operating Ratings

VIN Voltage	13V to 100V
External Voltage Applied to VCC	8V to 15V
Operation Junction Temperature	−40°C to + 125°C

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{VIN} = 48V, V_{VCC} = 10V, R_{RT1} = 30.1 kΩ, R_{RT2} = 30.1 kΩ, V_{UVLO} = 3V unless otherwise stated. See (1) and (2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Startup Regulator (VCC Pin)						
V_{VCC}	VCC voltage	I_{VCC} = 10 mA	**7.4**	7.7	**8**	V
$I_{VCC(Lim)}$	VCC current limit	V_{VCC} = 7V	**45**	60		mA
$V_{VCC(UV)}$	VCC Under-voltage threshold	V_{VIN} = V_{VCC}	**VCC Reg-0.2**	VCC Reg-0.1		V
	Hysteresis			1.5		V
I_{VIN}	Startup regulator current	V_{VIN} = 100V, V_{UVLO} = 0V		350	**430**	µA
		V_{VIN} = 48V, V_{UVLO} = 0V		325	**370**	µA
	Supply current into VCC from external source	Outputs & COMP = Open		3	**5.5**	mA
Voltage Reference Regulator (REF Pin)						
V_{REF}	REF Voltage	I_{REF} = 0 mA	**4.75**	5	**5.15**	V
	REF Voltage Regulation	I_{REF} = 0 to 2.5 mA		7	**25**	mV
$I_{REF(Lim)}$	REF Current Limit	V_{REF} = 4.5V	**5**	10		mA
	VREF Under-Voltage Threshold		**3.7**	4	**4.3**	V
$V_{REF(UV)}$	Hysteresis			0.35		V

(1) All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production at T_A = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Typical specifications represent the most likely parametric norm at 25°C operation.

Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{VIN} = 48V, V_{VCC} = 10V, R_{RT1} = 30.1 kΩ, R_{RT2} = 30.1 kΩ, V_{UVLO} = 3V unless otherwise stated. See (1) and (2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Under-Voltage Lock Out and Shutdown (UVLO Pin)						
V_{UVLO}	Under-voltage threshold		**1.20**	1.25	**1.295**	V
I_{UVLO}	Hysteresis current	UVLO pin sinking	**18**	22	**25**	µA
	Under-voltage Shutdown Threshold	UVLO voltage rising	**0.37**	0.42	**0.47**	V
	Hysteresis			0.1		V
Current Sense Input (CS Pin)						
V_{CS}	Current Limit Threshold		**0.22**	0.25	**0.29**	V
	CS delay to output	CS from zero to 1V. Time for OUTA and OUTB to fall to 90% of VCC. Output load = 0 pF.		27		ns
	Leading edge blanking time at CS			65		ns
	CS sink impedance (clocked)	Internal FET sink impedance		21	**45**	Ω
Current Limit Restart (RES Pin)						
V_{RES}	RES Threshold		**1.9**	2	**2.2**	V
	Charge source current	V_{RES} = 1.5V	**14**	18	**22**	µA
	Discharge sink current	V_{RES} = 1V	**5**	8	**11**	µA
Soft-Start (SS Pin)						
I_{SS}	Charging current in normal operation	V_{SS} = 0	**70**	100	**130**	µA
	Charging current during a hiccup mode restart	V_{SS} = 0	**0.6**	1	**1.4**	µA
	Soft-Stop Current Sink	V_{SS} = 2.0V	**70**	100	**130**	µA
Oscillator (RT1 and RT2 Pins)						
DT	Dead-Time	R_{RT2} = 15 kΩ	**40**	75	**105**	ns
		R_{RT2} = 75 kΩ		250		ns
F_{SW1}	Frequency 1 (at OUTA, half oscillator frequency)	R_{RT1} = 30.1 kΩ, R_{RT2} = 30.1 kΩ, T_J = 25°C T_J = -40°C to 125°C	**176**	200	**223**	kHz
F_{SW2}	Frequency 2 (at OUTA, half oscillator frequency)	R_{RT1} = 11 kΩ, R_{RT2} = 30.1 kΩ, T_J = 25°C T_J = -40°C to 125°C	**441**	508	**571**	kHz
	DC level			2		V
	Input Sync threshold		**2.5**	3	**3.4**	V
PWM Controller (Comp Pin)						
	Delay to output			65		ns
V_{PWM-OS}	SS to RAMP offset		**0.7**	1	**1.2**	V
	Minimum duty cycle	V_{SS} = 0V			0	%
	COMP Open Circuit Voltage	V_{FB} = 0V	**4.5**	4.75	**5**	V
	COMP short circuit current	V_{FB} = 0V, COMP = 0V	**0.5**	1	**1.5**	mA
Voltage Feed-Forward (RAMP Pin)						
	RAMP sink impedance(Clocked)			5	**20**	Ω
Error Amplifier						
GBW	Gain Bandwidth			4		MHz
	DC Gain			75		dB
	Input Voltage	V_{FB} = COMP	**1.22**	1.245	**1.27**	V
	COMP sink capability	V_{FB} = 1.5V COMP=1V	5	13		mA

Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{VIN} = 48V, V_{VCC} = 10V, R_{RT1} = 30.1 kΩ, R_{RT2} = 30.1 kΩ, V_{UVLO} = 3V unless otherwise stated. See (1) and (2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	FB Bias Current			10		nA
Main Output Drivers (OUTA and OUTB Pins)						
	Output high voltage	I_{OUT} = 50 mA, (Source)	**Vcc-0.5**	Vcc-0.25		V
	Output low voltage	I_{OUT} = 100 mA (Sink)		0.2	**0.5**	V
	Rise time	C_{LOAD} = 1 nF		15		ns
	Fall time	C_{LOAD} = 1 nF		13		ns
	Peak source current	V_{VCC} = 10V		1.2		A
	Peak sink current	V_{VCC} = 10V		1.2		A
Thermal Shutdown						
T_{SD}	Thermal Shutdown Threshold			165		°C
	Thermal Shutdown Hysteresis			25		°C
Thermal Resistance						
θ_{JC}	Junction to Case	TSSOP-16		29		°C/W
θ_{JA}	Junction to Ambient	TSSOP-16		125		°C/W

Typical Performance Characteristics

Typical Application Circuit Efficiency

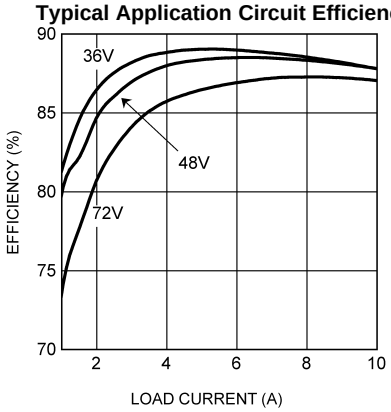


Figure 2.

V_{VCC} and V_{REF} vs V_{VIN}

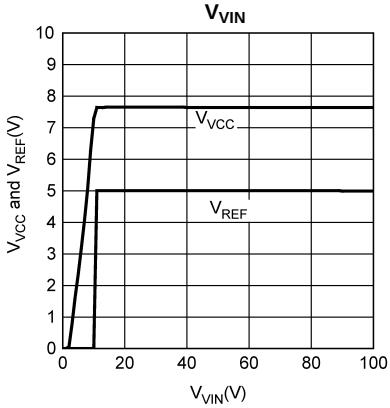


Figure 3.

Start-Up Regulator Current (UVLO = 0)

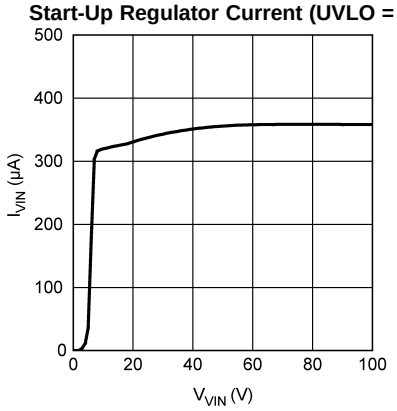


Figure 4.

V_{VCC} vs I_{VCC}

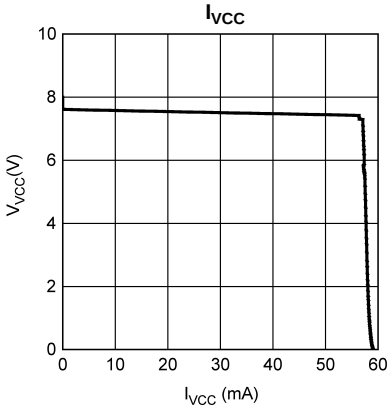


Figure 5.

V_{REF} vs I_{REF}

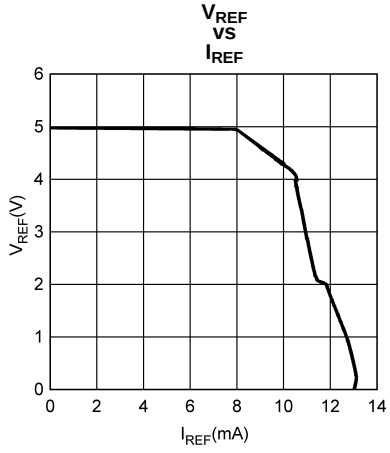


Figure 6.

Feedback Amplifier Gain/Phase

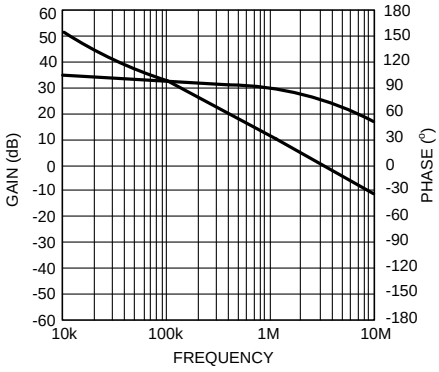


Figure 7.

Typical Performance Characteristics (continued)

Oscillator Frequency vs RT1

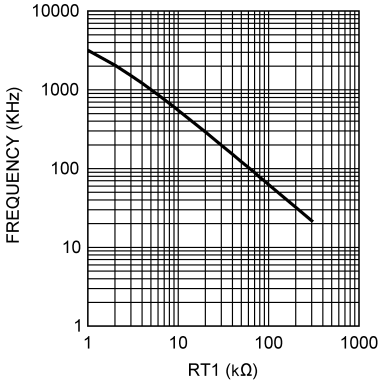


Figure 8.

Dead-Time vs RT2

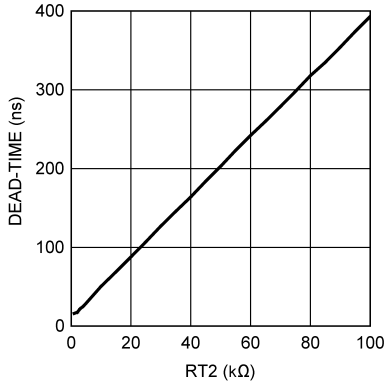


Figure 9.

V_{FB} vs Temperature

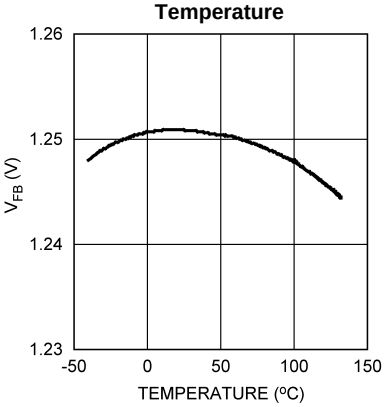


Figure 10.

Oscillator Frequency vs Temperature

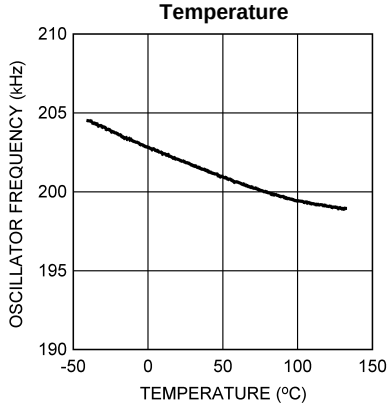


Figure 11.

Dead-Time vs Temperature

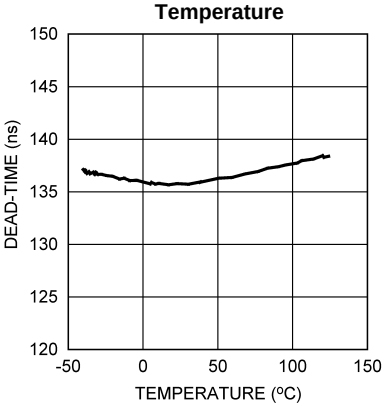


Figure 12.

Soft-Start and Restart Current vs Temperature

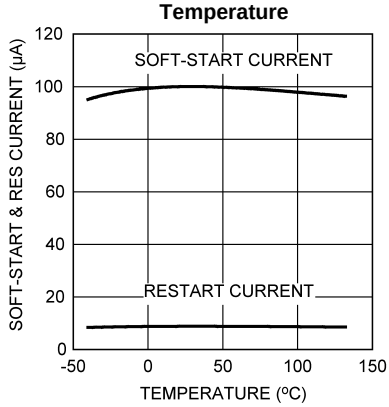


Figure 13.

Block Diagram

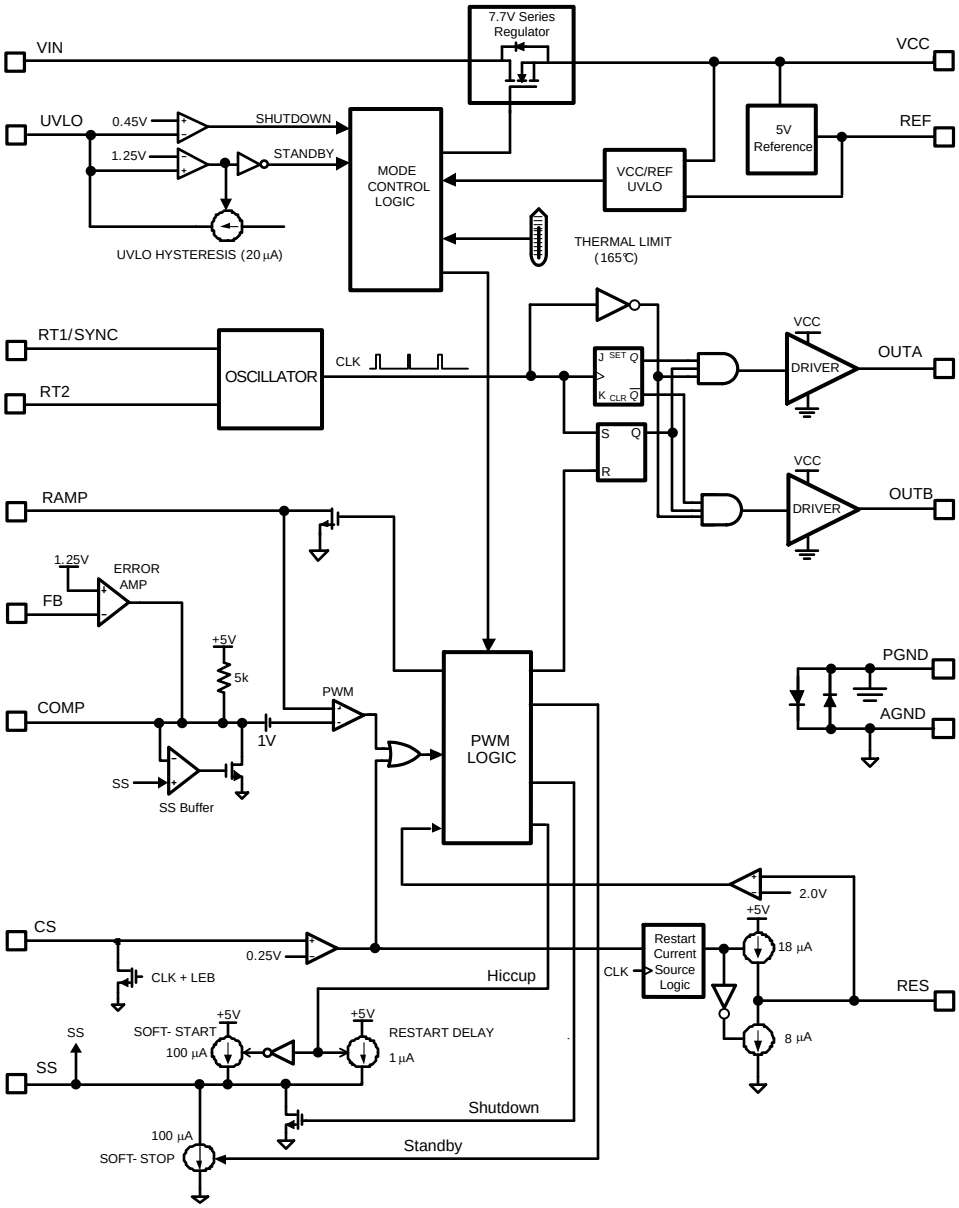


Figure 14. Simplified Block Diagram

FUNCTIONAL DESCRIPTION

The LM5037 PWM controller contains all the features necessary to implement double-ended power converter topologies such as push-pull, half-bridge and full-bridge. The unique architecture allows the modulator to be configured for either voltage-mode or current-mode control. The LM5037 provides two alternative gate driver outputs to drive the primary side power MOSFETs with programmable forced dead-time. The LM5037 can be configured to operate with bias voltages ranging from 13V to 100V. Additional features include line under-voltage lockout, cycle-by-cycle current limit, voltage feed-forward compensation, and hiccup mode fault protection with adjustable delays, soft-start, and a 2MHz capable oscillator with synchronization capability, precision reference and thermal shutdown. These rich set of features simplify the design of double ended topologies. The functional block diagram is shown in Figure 14.

HIGH-VOLTAGE START-UP REGULATOR

The LM5037 contains an internal high voltage, start-up regulator that allows the input pin (VIN) to be connected directly to the supply voltage over a range of 13V to a maximum of 100V. The regulator input can withstand transients up to 105V. The regulator output at VCC (7.7V) is internally current limited with a guaranteed minimum of 45 mA. When the UVLO pin potential is greater than 0.45V, the VCC regulator is enabled to charge an external capacitor connected to the VCC pin. The VCC regulator provides power to the voltage reference (REF) and the gate drivers (OUTA and OUTB). When the voltage on the VCC pin exceeds its Under-Voltage (VCC UV) threshold, the internal voltage reference (REF) reaches its regulation set point of 5V and the UVLO voltage is greater than 1.25V, the controller outputs are enabled. The value selected for the VCC capacitor depends on the total system design, and its start-up characteristics. The recommended range of values for the VCC capacitor is 0.47 µF to 10 µF.The internal power dissipation of the LM5037 can be reduced by powering VCC from an external supply. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.1V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves efficiency while reducing the controller's power dissipation. The VCC UV circuit will still function in this mode, requiring that VCC never falls below its nominal threshold during the start-up sequence. The VCC regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation. Therefore the auxiliary VCC voltage should never exceed the VIN voltage.

An external DC bias voltage can be used instead of the internal regulator by connecting the external bias voltage to both the VCC and the VIN pins. In this particular case, the external bias must be greater than max VCC regulation of 8V and less than the VCC maximum operating voltage rating (15V).

LINE UNDER-VOLTAGE DETECTOR

The LM5037 contains a dual level line Under-Voltage Lock Out (UVLO) circuit. When the UVLO pin voltage is below 0.45V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.45V but less than 1.25V, the controller is in standby mode. In standby mode the VCC and REF bias regulators are active while the controller outputs are disabled. When the VCC and REF outputs exceed their respective under-voltage thresholds and the UVLO pin voltage is greater than 1.25V, the outputs are enabled and normal operation begins. An external set-point voltage divider from VIN to GND can be used to set the minimum operating voltage of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25V when VIN enters the desired operating range. UVLO hysteresis is accomplished with an internal 22 µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO pin voltage exceeds 1.25V threshold, the current source is activated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25V threshold, the current source is disabled causing the voltage at the UVLO pin to quickly fall. The hysteresis of the 0.45V shutdown comparator is internally fixed at 100 mV.

The UVLO pin can also be used to implement various remote enable/disable functions. Turning off the converter by forcing the UVLO pin to standby condition provides a controlled soft-stop. See the Soft-Start section for more details.

REFERENCE

The REF pin is the output of a 5V linear regulator that can be used to bias an opto-coupler transistor and external housekeeping circuits. The regulator output is internally current limited to 10 mA (typical).

ERROR AMPLIFIER

An internal high gain error amplifier is provided within the LM5037. The amplifier's non-inverting reference is tied to a 1.25V reference. In non-isolated applications the power converter output is connected to the FB pin via the voltage setting resistors and loop compensation is connected between the COMP and FB pins. A typical gain/phase plot is shown in performance curves section.

For most isolated applications the error amplifier function is implemented on the secondary side. Since the internal error amplifier is configured as an open drain output, it can be disabled by connecting FB to ground. The internal 5K pull-up resistor connected between the COMP pin and the 5V reference can be used as the pull-up for an opto-coupler or other isolation device .

CYCLE-BY-CYCLE CURRENT LIMIT

The CS pin is to be driven by a signal representative of the transformer primary current. The current sense signal can be generated by using a sense resistor or a current sense transformer. If the voltage sensed at the CS pin exceeds 0.25V, the current sense comparator terminates the output driver pulse. If the high current condition persists, the controller operates in a cycle-by-cycle current limit mode with duty cycle determined by the current sense comparator instead of the PWM comparator. Cycle-by-cycle current limiting may eventually trigger the hiccup mode restart cycle; depending on the configuration of the RES pin (see Overload Protection Timer below). To suppress noise, a small R-C filter connected to the CS pin and located near the controller is recommended. An internal 21Ω MOSFET discharges the external current sense filter capacitor at the conclusion of every cycle. The discharge MOSFET remains on for an additional 65 ns after either OUTA or OUTB driver switches high to blank leading edge transients in the current sensing circuit. Discharging the CS pin filter each cycle and blanking leading edge spikes reduces the filtering requirements and improves the current sense response time. The current sense comparator is very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the CS and AGND pins. If a sense resistor located in the source of the main MOSFET switch is used for current sensing, a low inductance type of resistor is required. When designing with a current sense resistor, all the noise sensitive, low power ground connections should be connected together near the AGND pin, and a single connection should be made to the power ground (sense resistor ground point).

OVERLOAD PROTECTION TIMER

The LM5037provides a current limit restart timer to disable the outputs and force a delayed restart (hiccup mode) if a current limit condition is repeatedly sensed. The number of cycle-by-cycle current limit events required to trigger the restart is programmed by the external capacitor at the RES pin. During each PWM cycle, the LM5037 either sources to or sinks current from the RES pin capacitor. If no current limit is detected during a cycle, a 8 µA discharge current sink is enabled to pull the RES pin towards ground. If a current limit is detected, the 8 µA sink current is disabled and a 18 µA current source causes the voltage at the RES pin to gradually increase. The LM5037 protects the converter with cycle-by-cycle current limiting while the voltage at RES pin increases. If the RES voltage reaches the 2.0V threshold, the following restart sequence occurs (also see Figure 15):

- The RES capacitor and SS capacitors are fully discharged.
- The soft-start current source is reduced from 100 µA to 1 µA.
- The SS capacitor voltage slowly increases. When the SS voltage reaches ≅1V, the PWM comparator will produce the first narrow output pulse. After the first pulse occurs, the SS source current reverts to the normal 100 µA level. The SS voltage increases at its normal rate, gradually increasing the duty cycle of the output drivers.
- If the overload condition persists after restart, cycle-by-cycle current limiting will begin to increase the voltage on the RES capacitor again, repeating the hiccup mode sequence.
- If the overload condition no longer exists after restart, the RES pin will be held at ground by the 8 µA current sink and normal operation resumes.

The overload timer function is very versatile and can be configured for the following modes of protection:

1. **Cycle-by-cycle only:** The hiccup mode can be completely disabled by connecting a zero to 50 kΩ resistor from the RES pin to AGND. In this configuration, the cycle-by-cycle protection will limit the output current indefinitely and no hiccup sequences will occur.
2. **Hiccup only:** The timer can be configured for immediate activation of a hiccup sequence upon detection of an overload by leaving the RES pin open circuit. In this configuration, the first detection of current limit

condition by the CS pin comparator will initiate a hiccup cycle with SS capacitor fully discharged and a delayed restart.

3. **Delayed Hiccup:** Connecting a capacitor to the RES pin provides a programmed interval of cycle-by-cycle limiting before initiating a hiccup mode restart, as previously described. The dual advantages of this configuration are that a short term overload will not cause a hiccup mode restart but during extended overload conditions, the average dissipation of the power converter will be very low.
4. **Externally Controlled Hiccup:** The RES pin can also be used as an input. By externally driving the pin to a level greater than the 2.0V hiccup threshold, the controller will be forced into the delayed restart sequence. For example, the external trigger for a delayed restart sequence could come from an over-temperature protection circuit or an output over-voltage sensor

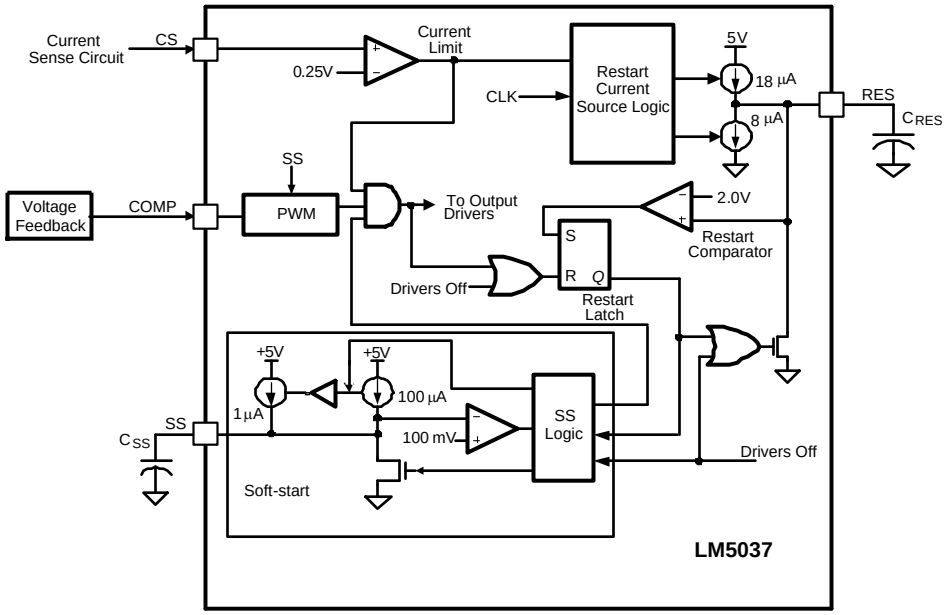


Figure 15. Current Limit Restart Circuit

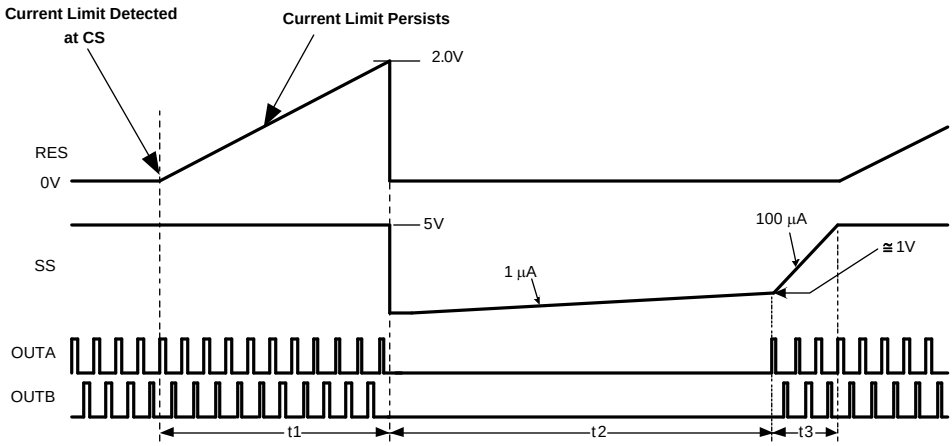


Figure 16. Current Limit Restart Timing

SOFT-START

The soft-start circuit allows the regulator to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. When bias is supplied to the LM5037, the SS pin capacitor is discharged by an internal MOSFET. When the UVLO, VCC and REF pins reach their operating thresholds, the SS capacitor is released and charged with a 100 µA current source. The PWM comparator control voltage at the COMP pin is clamped to the SS pin voltage by an internal amplifier. When the PWM comparator input reaches 1V, output pulses commence with slowly increasing duty cycle. The voltage at the SS pin eventually increases to 5V, while the voltage at the PWM comparator increases to the value required for regulation as determined by the voltage feedback loop.

One method to disable the regulator is to ground the SS pin. This forces the internal PWM control signal to ground, reducing the output duty cycle quickly to zero. Releasing the SS pin initiates a soft-start sequence and normal operation resumes. A second shutdown method is discussed in the UVLO section.

PWM COMPARATOR

The pulse width modulation (PWM) comparator compares the voltage ramp signal at the RAMP pin to the loop error signal. The loop error signal is derived from the internal error amplifier (COMP pin). The resulting control voltage passes through a 1V level shift before being applied to the PWM comparator. This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The common mode input voltage range of the PWM comparator is from 0 to 4.3V.

RAMP PIN

The voltage at the RAMP pin provides the modulation ramp for the PWM comparator. The PWM comparator compares the modulation ramp signal at the RAMP pin to the loop error signal to control the output duty cycle. The modulation ramp can be implemented either as a ramp proportional to input voltage, known as feed-forward voltage mode control, or as a ramp proportional to the primary current, known as current mode control. The RAMP pin is reset by an internal FET with an $R_{DS(ON)}$ of 5Ω (typical) at the end of every cycle. The ability to configure the RAMP pin for either voltage mode or current mode allows the controller to be implemented for the optimum control method for the selected power stage topology. Configuring RAMP pin is explained below and the differences between voltage mode control and current mode control in various double-ended topologies is explained in Applications Information section.

FEED-FORWARD VOLTAGE MODE

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pins is required to create the PWM ramp signal as shown in Figure 17 below. It can be seen that the slope of the signal at RAMP will vary in proportion to the input line voltage. This varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal by the pulse width modulator comparator to control the duty cycle of the outputs. With a constant error signal, the on-time (t_{ON}) varies inversely with the input voltage (VIN) to stabilize the Volt • Second product of the transformer primary. At the end of clock period, an internal FET will be enabled to reset the C_{FF} capacitor. The formulae for R_{FF} and C_{FF} and component selection criteria are explained in Applications Information section. The amplitude of the signal driving RAMP pin must not exceed the common mode input voltage range of the PWM comparator (3.3V) while in normal operation.

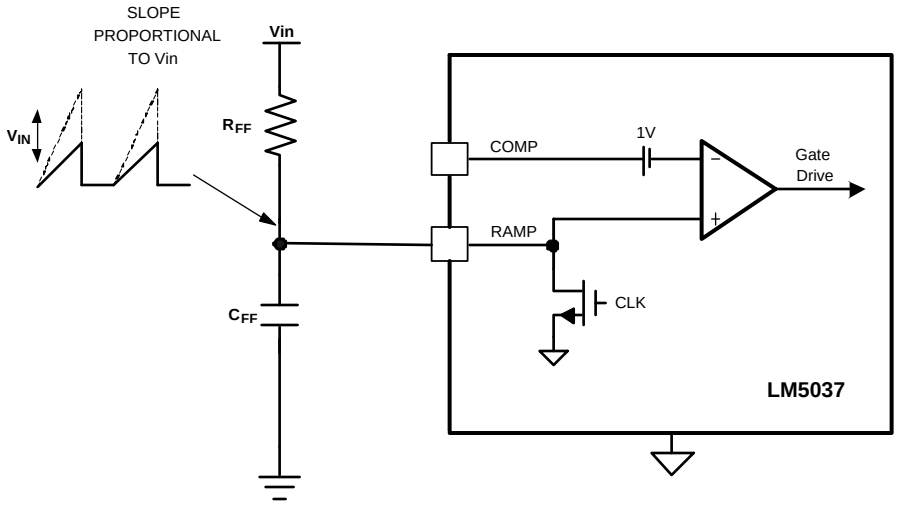


Figure 17. Feed-Forward Voltage Mode Configuration

CURRENT MODE

The LM5037 can be configured for current mode control by injecting a signal representative of primary current into the RAMP pin. One way to achieve this is shown in Figure 18. Filter components R_{filter} and C_{filter} are used to filter leading edge noise spikes. The signal at the CS pin is thus a ramp on a pedestal. The pedestal corresponds to the continuous conduction current in the transformer at the beginning of an OUTA or OUTB conduction cycle. The R-C circuit (R_{Slope} and C_{Slope}), shown in Figure 18, tied to V_{REF} adds an additional ramp to the current sense signal. This additional ramp signal, known as slope compensation, is required to avoid instabilities at duty cycles above 50% (25% per phase). The compensated RAMP signal consists of two parts, the primary current signal and the slope compensation. The compensated RAMP signal is compared to the error signal by the PWM comparator to control the duty cycle of the outputs. The RAMP capacitor and CS capacitor are reset through internal discharge FETs. The $R_{DS(ON)}$ of RAMP discharge FET is 5Ω (typical); this ensures fast discharge of the RAMP reset capacitor. Any dc voltage source can be used in place of V_{REF} to generate the slope compensation ramp.

The timing diagram shown in Figure 19 depicts the current mode waveforms and relative timing. When OUTA or OUTB is enabled, the signal at the RAMP pin consists of the CS pin signal (current ramp on a pedestal) plus the slope compensation ramp (dotted lines). When OUTA or OUTB is turned off, the primary current component is absent but the voltage at the RAMP pin continues to rise due to slope compensation component until the end of the clock period, after which it is reset by the RAMP discharge FET. A component selection example is explained in detail in the Applications Information section.

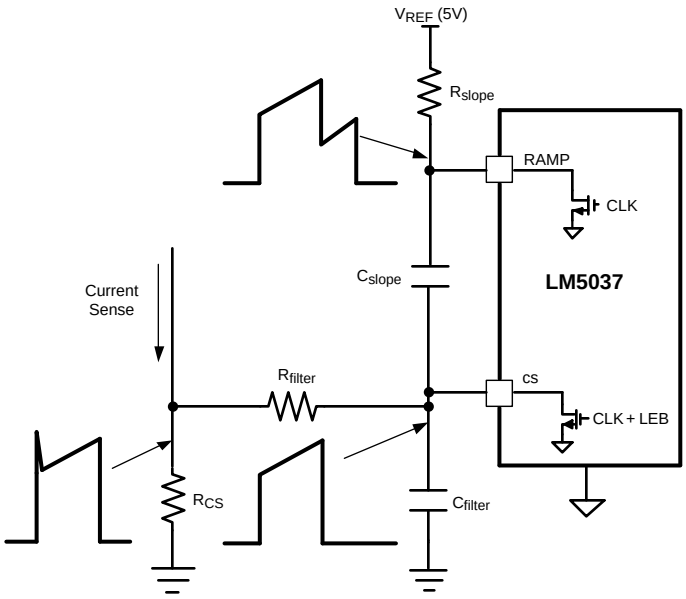


Figure 18. Current Mode Configuration with Slope Compensation

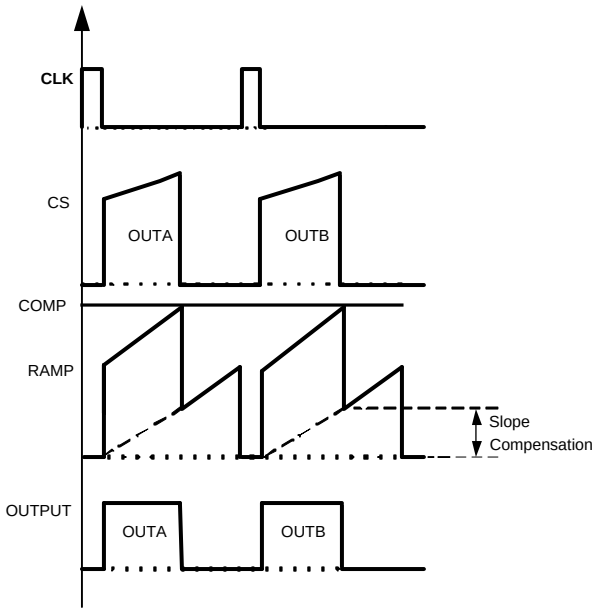


Figure 19. Timing Diagram for Current Mode Configuration

OSCILLATOR

The LM5037 oscillator frequency and the maximum duty cycle are set by two external resistors connected between the RT1 and RT2 pins to AGND. The minimum dead-time between OUTA and OUTB pulses is proportional to the RT2 resistor value and the overall oscillator frequency is inversely proportional to RT1 and RT2 resistor values. Each output switches at half the oscillator frequency. Initially, RT2 should be selected for the desired dead-time or for the desired maximum duty cycle (D_{max}).

$$RT2 = \frac{\text{Dead-Time}}{5.0 \times 10^{-12}} \quad 50\ \text{ns} < DT < 250\ \text{ns}$$

or

$$RT2 = \frac{(1 - D_{max})/F_{OSC}}{5.0 \times 10^{-12}} \tag{1}$$

It is recommended to set the dead-time range between 50 ns and 250 ns. Beyond 250 ns, RT2 becomes excessively large, and is prone to noise pickup. Fixed internal delays limit the dead-time to greater than 50 ns. After the dead-time has been programmed by RT2, the overall oscillator frequency can be set by selecting resistor RT1 from :

$$RT1 = \frac{\frac{1}{F_{OSC}} - (\text{Dead-Time})}{0.162 \times 10^{-9}} \tag{2}$$

For example, if the desired oscillator frequency is 400 kHz (OUTA and OUTB each switching at 200 kHz) and desired dead-time is 100 ns, the maximum duty cycle for each output will be 96% and the values of RT1 and RT2 will be 15 kΩ and 20 kΩ respectively.

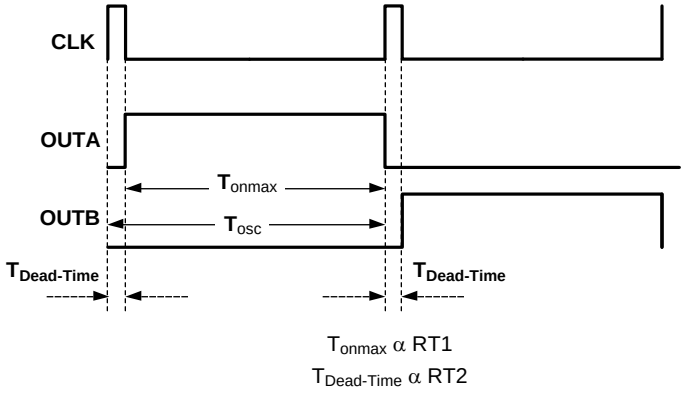


Figure 20. Timing Diagram of OUTA, OUTB and Dead-Time Set by RT2

As shown in Figure 20, the internal clock pulse width is the same as the dead-time set by RT2. This dead-time pulse is used to limit the maximum duty cycle for each of the outputs. Also, the discharge FET connected to the RAMP pin is enabled during the dead-time every clock period. The voltages at both the RT1 and RT2 pins are internally regulated to a nominal 2V. Both the resistors RT1 and RT2 should be located as close as possible to the IC, and connected directly to the pins. The tolerance of the external resistors and the frequency tolerance indicated in the Electrical Characteristics table must be taken into account when determining the worst case frequency range.

SYNC CAPABILITY

The LM5037 can be synchronized to an external clock by applying a narrow ac pulse to the RT1 pin. The external clock must be at least 10% higher than the free-running oscillator frequency set by the RT1 and RT2 resistors. If the external clock frequency is less than the programmed frequency, the LM5037 will ignore the synchronizing pulses. The synchronization pulse width at the RT1 pin must be a minimum of 15 ns wide. The synchronization signal should be coupled into the RT1 pin through a 100 pF capacitor or another value small enough to ensure the sync pulse width at RT1 is less than 60% of the clock period under all conditions. When the synchronizing pulse transitions from low-to-high (rising edge), the voltage at the RT1 pin must be driven to exceed 3.0V from its nominal 2.0V volt dc level. During the synchronization clock signal's low time, the voltage at the RT1 pin will be clamped at 2V volts by an internal regulator. The RT1 and RT2 resistors are always required, whether the oscillator is free running or externally synchronized.

GATE DRIVER OUTPUTS (OUTA & OUTB)

The LM5037 provides two alternating gate driver outputs, OUTA and OUTB. The internal gate drivers can each source and sink 1.2A peak each. The maximum duty cycle is inherently limited to less than 50% and is based on the value of RT2 resistor. As an example, if the COMP pin is in a high state, RT1 = 15K and RT2 = 20K then the outputs will operate at maximum duty cycle of 96%.

THERMAL PROTECTION

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum rated junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state with the output drivers (OUTA and OUTB) and the bias regulators (VCC and REF) disabled. This helps to prevent catastrophic failures from accidental device overheating. During thermal shutdown, the soft-start capacitor is fully discharged and the controller follows a normal start-up sequence after the junction temperature falls to the operating level (140°C).

Application Information

The following information is intended to provide guidelines for the design process when applying the LM5037.

TOPOLOGY and CONTROL ALGORITHM CHOICE

The LM5037 has all the features required to implement double-ended power converter topologies such as push-pull, half-bridge and full-bridge with minimum external components. One key feature is the flexibility in control algorithm selection, i.e., the LM5037 can be used to implement either voltage mode control or current mode control. Designers familiar with these topologies recognize that conventionally, current mode control is used for push-pull and full-bridge topologies while voltage mode control is required for the half-bridge topology. In limited applications, voltage mode control can be used for push-pull and full-bridge topologies as well, with special care to maintain flux balance, such as using a dc-blocking capacitor in the primary (full-bridge). The goal of this section is to illustrate implementation of both current mode control and voltage mode control using the LM5037 and aid the designer in the design process.

VOLTAGE MODE CONTROL USING THE LM5037

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pins is required to create a saw-tooth modulation ramp signal shown in Figure 21. The slope of the signal at RAMP will vary in proportion to the input line voltage. The varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. With a constant error signal, the on-time (t_{ON}) varies inversely with the input voltage (VIN) to stabilize the Volt • Second product of the transformer primary. Using a line feed-forward ramp for PWM control requires very little change in the voltage regulation loop to compensate for changes in input voltage, as compared to a fixed slope oscillator ramp. Furthermore, voltage mode control is less susceptible to noise and does not require leading edge filtering, and is therefore a good choice for wide input range power converters. Voltage mode control requires a more complicated compensation network, due to the complex-conjugate poles of the L-C output filter.

In push-pull and full-bridge topologies, any asymmetry in the volt-second product applied to primary in one phase may not be cancelled by subsequent phase, possibly resulting in a dc current build-up in the transformer, which pushes the transformer core towards saturation. Special care in the transformer design, such as gapping the core, or adding ballasting resistance in the primary is required to rectify this imbalance when using voltage mode control with these topologies. Current mode control naturally corrects for any volt-second asymmetry in the primary.

The recommended capacitor value range for C_{FF} is 100 pF to 1500 pF. Referring to Figure 21, it can be seen that value C_{FF} must be small enough such that the capacitor can be discharged within the clock (CLK) pulse width each cycle. The CLK pulse width is same as the dead-time set by RT2. The minimum possible dead-time for LM5037 is 50 ns and the internal discharge FET $R_{DS(ON)}$ is 5Ω (typical),

The value of R_{FF} required can be calculated from

$$R_{FF} = \frac{-1}{F_{OSC} \times C_{FF} \times \ln\left(1 - \frac{V_{RAMP}}{VIN_{min}}\right)} \quad (3)$$

For example, assuming a V_{Ramp} of 1 volt at VIN_{min} (a good compromise of signal range and noise immunity), oscillator frequency, F_{OSC} of 250 kHz, VIN_{min} of 24 Volts, and C_{FF} = 270 pF results in a value for R_{FF} of 348 kΩ.

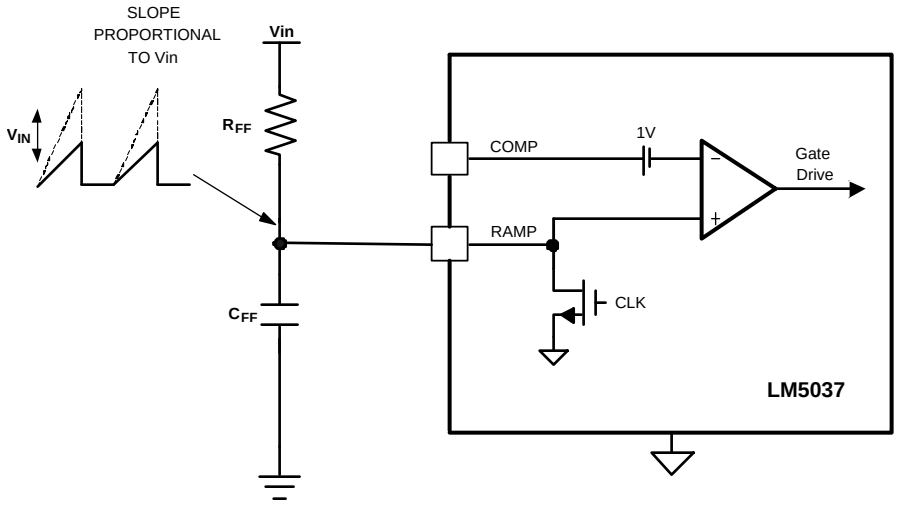


Figure 21. Feed-Forward Voltage Mode Configuration

CURRENT MODE CONTROL USING THE LM5037

The LM5037 can be configured in current mode control by applying the primary current signal into the RAMP pin. One way to achieve this is shown in Figure 22, which depicts a simplified push-pull converter. The primary current is sensed using a sense resistor and the current information is then filtered and applied to the RAMP pin through capacitor C_{slope}, for use as the modulation ramp. It can be seen that the signal applied to the RAMP pin consists of the primary current information from the CS pin plus an additional ramp for slope compensation, added by R_{slope} and C_{slope}.

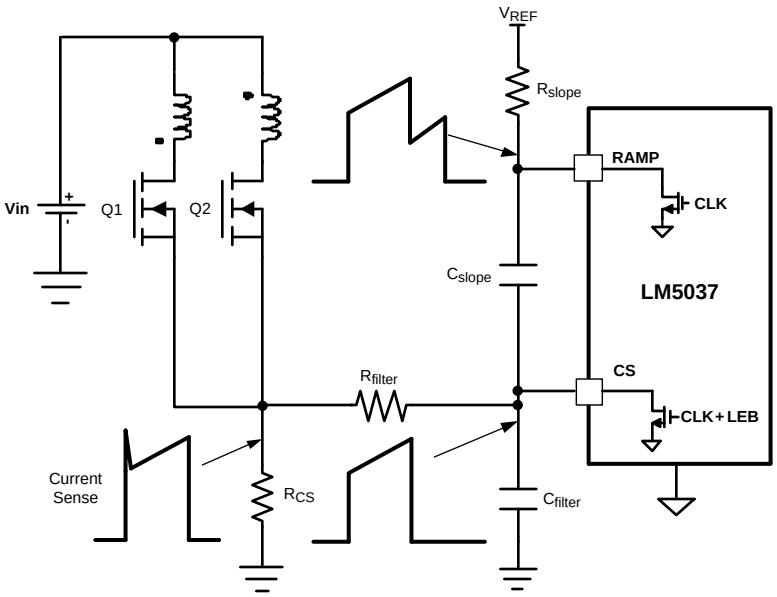


Figure 22. Current Mode Configuration

Current mode control inherently provides line voltage feed-forward, cycle-by-cycle current limiting and ease of loop compensation as it removes the additional pole due to output inductor. Also, in push-pull and full-bridge converters, current mode control inherently balances volt-second product in both the phases by varying the duty cycle as needed to terminate the cycle at the same peak current for each output phase. For duty cycles greater than 50% (25% for each phase), peak current mode controlled circuits are subject to sub-harmonic oscillation.

Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow duty cycles at the controller output. Adding an artificial ramp (slope compensation) to the current sense signal will eliminate this potential oscillation. Current mode control is also susceptible to noise and layout considerations. It is recommended that C_{Filter} and C_{slope} be placed as close to the IC as possible to avoid any noise pickup and trace inductance. When the converter is operating at low duty cycles and light load, the primary current amplitude is small and is susceptible to noise. The artificial ramp, added to avoid sub-harmonic oscillations, provides additional benefits by improving the noise immunity of the converter.

Configuration and component selection for current mode control is recommended as follows: The current sense resistor is selected such that during over current condition, the voltage across the current sense resistor is above the minimum CS threshold of 220 mV. It is recommended to set the impedances of R_{Filter} and C_{Filter} as seen from C_{slope} at relatively low values, so that the slope compensation is primarily dictated by R_{slope} and C_{slope} components. For example, if the filtering time (R_{Filter} and C_{Filter}) for leading edge noise is selected for 50 ns and if the value selected for R_{Filter} = 25Ω, then

$$C_{Filter} = \frac{50 \times 10^{-9}}{3 \times 25\Omega} \tag{4}$$

Resulting in a value of C_{Filter} = 680 pF (approximated to a standard value). In general, the amount of slope compensation required to avoid sub-harmonic oscillation is equal to at least one-half the down-slope of the output inductor current, transformed to the primary. To mitigate sub-harmonic oscillation after one switching period, the slope compensation has to be equal to one times the down slope of the filter inductor current transformed to primary. This is known as deadbeat control. For circuits where primary current is sensed using a resistor, the amount of slope compensation for dead-beat control required can be calculated from:

$$\text{Slope-Comp} = \frac{\text{Turns-Ratio} \times \text{Vout} \times R_{CS}}{F_{OSC} \times L_{filter}} \tag{5}$$

Where, Turns-Ratio is referred with respect to the primary. For example, for a 5V output converter with a turns ratio between secondary and primary of 1:2, an oscillator frequency (F_{OSC}) of 250 kHz, a filter inductance of 4 µH (L_{Filter}) and a current sense resistor (R_{CS}) of 32 mΩ, slope compensation of 80 mV will suffice. The slope compensation "volts" that results from the above expression is the maximum voltage of the artificial ramp added linearly to the RAMP pin till the end of maximum switching period. For circuits where a current sense tramsformer is used for primary current sensing, the turns-ratio of the current sense transformer has to be taken into account.

C_{slope} should be selected such that it can be fully discharged by the internal RAMP discharge FET. Capacitor values ranging from 100 pF to 1500 pF are recommended. The value must be small enough such that the capacitor can be discharged within the clock (CLK) pulse width each cycle.

R_{slope} can be selected from the following formula:

$$R_{slope} = \frac{-1}{F_{OSC} \times C_{slope} \times \ln\left(1 - \frac{\text{Slope-Comp}}{V_{REF}}\right)} - R_{filter} \tag{6}$$

For example, with a C_{slope} of 1500 pF, F_{OSC} of 250 kHz, reference voltage of 5V (V_{REF}), slope compensation of 80 mV and R_{filter} = 25Ω results in R_{slope} value of 165 kΩ.

VIN and VCC

The voltage applied to the VIN pin, which may be the same as the system voltage applied to the power transformer's primary (V_{PWR}), can vary in the range from 8V to 100V. The current into the VIN pin depends primarily on the gate charge provided by the output drivers, the switching frequency, and any external loads on the VCC and REF pins. It is recommended that the filter shown in Figure 23 be used to suppress transients that may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM5037.

When power is applied to VIN and the UVLO pin voltage is greater than 0.45V, the VCC regulator is enabled and supplies current into an external capacitor connected to the VCC pin. When the voltage on the VCC pin reaches the regulation point of 7.7V, the voltage reference (REF) is enabled. The reference regulation set point is 5V. The outputs (OUTA and OUTB) are enabled when the two bias regulators reach their set point and the UVLO pin potential is greater than 1.25V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.1V to shut off the internal start-up regulator.

After the outputs are enabled and the external VCC supply voltage has begun supplying power to the IC, the current into the VIN pin drops below 1 mA. VIN should remain at a voltage equal to or above the VCC voltage to avoid reverse current through protection diodes.

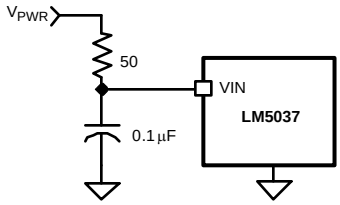


Figure 23. Input Transient Protection

FOR APPLICATIONS WITH >100V INPUT

For applications where the system input voltage exceeds 100V or the IC power dissipation is of concern, the LM5037 can be powered from an external start-up regulator as shown in Figure 24. In this configuration, the VIN and the VCC pins should be connected together. The voltage at the VCC and VIN pins must be greater than 8.1V (> Max VCC reference voltage) yet not exceed 15V. An auxiliary winding can be used to reduce the power dissipation in the external regulator once the power converter is active. The NPN base-emitter reverses breakdown voltage, which can be as low as 5V for some transistors, should be considered when selecting the transistor.

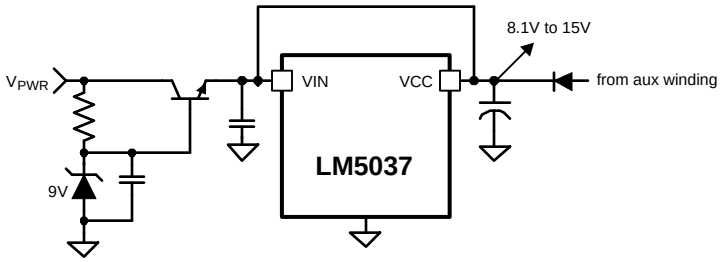


Figure 24. Start-up Regulator for VPWR >100V

CURRENT SENSE

The CS pin should receive an input signal representative of the transformer's primary current, either from a current sense transformer or from a resistor in series with the source of the OUTA and OUTB MOSFET switches. In both cases, the sensed current creates a voltage ramp across R1, and the R_F/C_F filter suppresses noise and transients as shown in Figure 25 and Figure 26. R1, R_F and C_F should be located as close to the LM5037 as possible, and the ground connection from the current sense transformer, or R1, should be a dedicated track to the AGND pin. The current sense components must provide greater than 220 mV at the CS pin when an over-current condition exists.

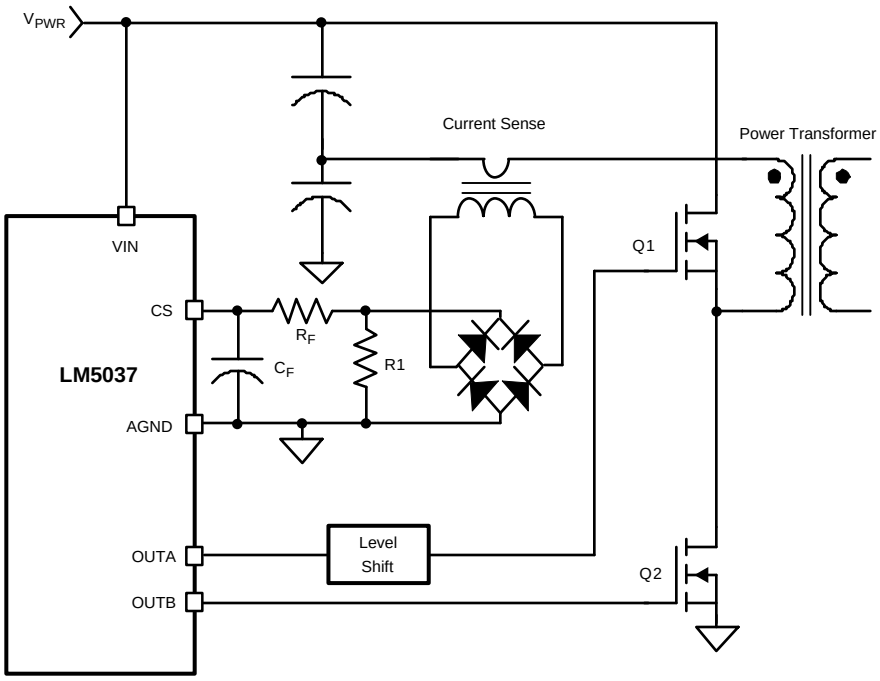


Figure 25. Current Sense Using Transformer

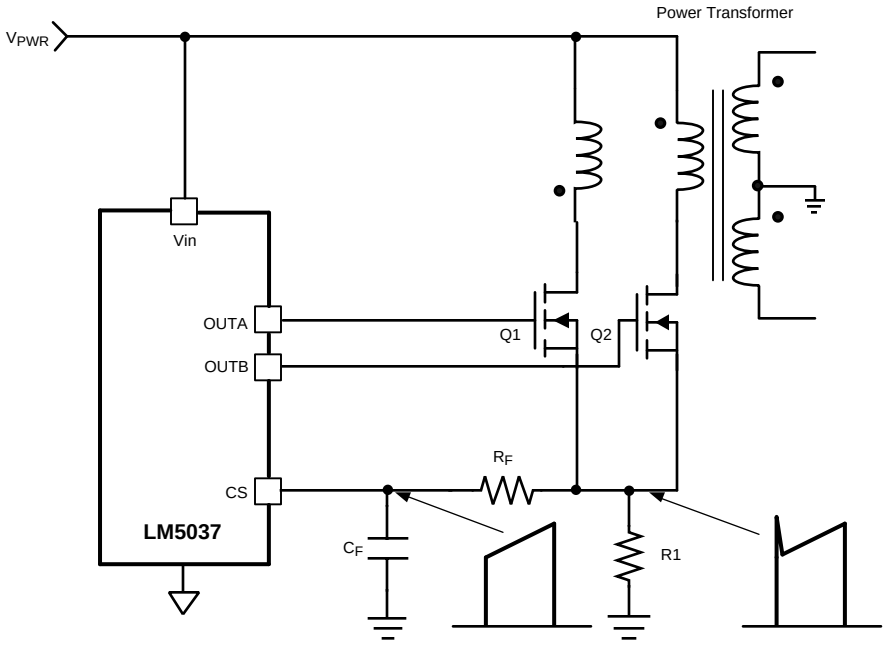


Figure 26. Current Sense Using Current Sense Resistor (R1)

UVLO DIVIDER SELECTION

A dedicated comparator connected to the UVLO pin detects an input under-voltage condition. When the UVLO pin voltage is below 0.45V, the LM5037 controller is in a low current shutdown mode. For a UVLO pin voltage greater than 0.45V but less than 1.25V, the controller is in standby mode with VCC and REF regulators active but no switching. Once the UVLO pin voltage is greater than 1.25V, the controller is fully enabled. When the UVLO pin voltage rises above the 1.25V threshold, an internal 22 µA current source as shown in Figure 27, is activated thus providing threshold hysteresis. The 22 µA current source is deactivated when the voltage at the UVLO pin falls below 1.25V. Resistance values for R1 and R2 can be determined from the following equations:

$$R_1 = \frac{\left(V_{HYS} - \frac{20 \times 10^{-3} \times V_{PWR}}{1.25}\right)}{22\ \mu A}$$

$$R_2 = \frac{1.25 \times R_1}{V_{PWR} - 1.25} \quad (7)$$

Where V_{PWR} is the desired turn-on voltage and V_{HYS} is the desired UVLO hysteresis at V_{PWR}.

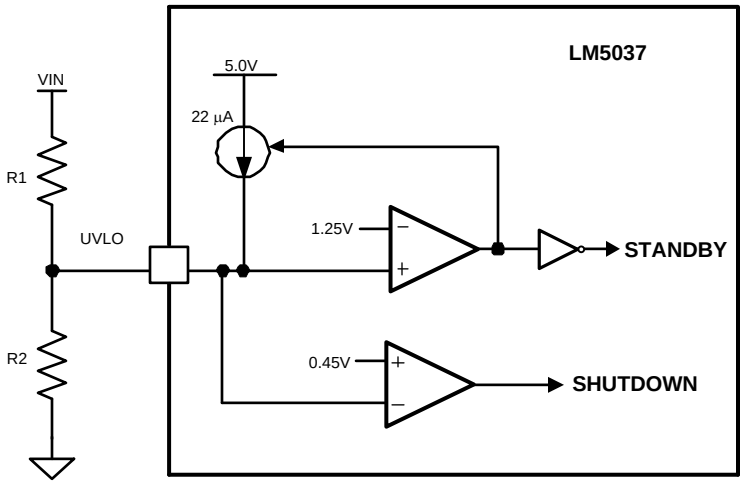


Figure 27. Basic UVLO Configuration

For example, if the LM5037 is to be enabled when V_{PWR} reaches 33V, and disabled when V_{PWR} decreases to 30V, R1 should be 113 kΩ, and R2 should be 4.42 kΩ. The voltage at the UVLO pin should not exceed 7V at any time. Be sure to check both the power and voltage rating (0603 resistors can be rated as low as 50V) for the selected R1 resistor. To maintain the UVLO threshold accuracy, a resistor tolerance of 1% or better is recommended.

Remote control of the LM5037 operational modes can be accomplished with open drain device(s) connected to the UVLO pin as shown in Figure 28.

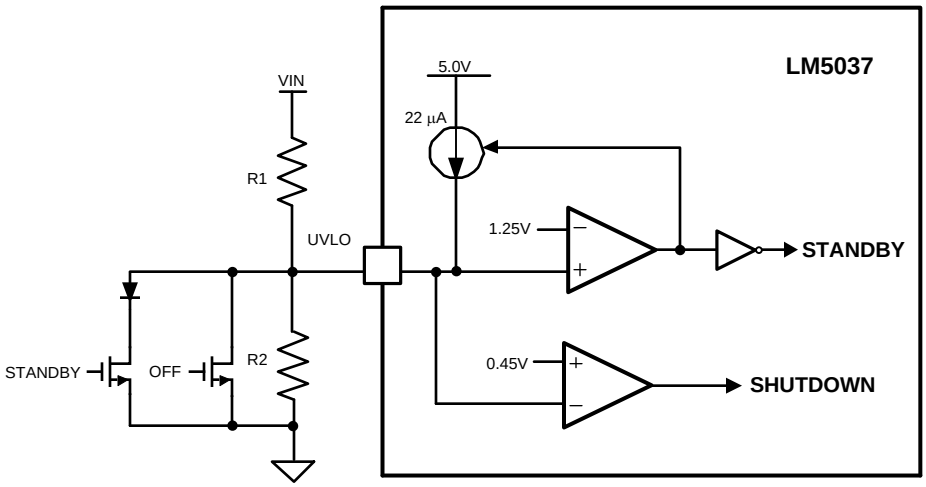


Figure 28. Remote Standby and Disable Control

HICCUP MODE CURRENT LIMIT RESTART (RES)

The basic operation of the hiccup mode current limit is described in the functional description. The delay time to the initiation of a hiccup cycle is programmed by the selection of the RES pin capacitor C_{RES} as illustrated in Figure 29.

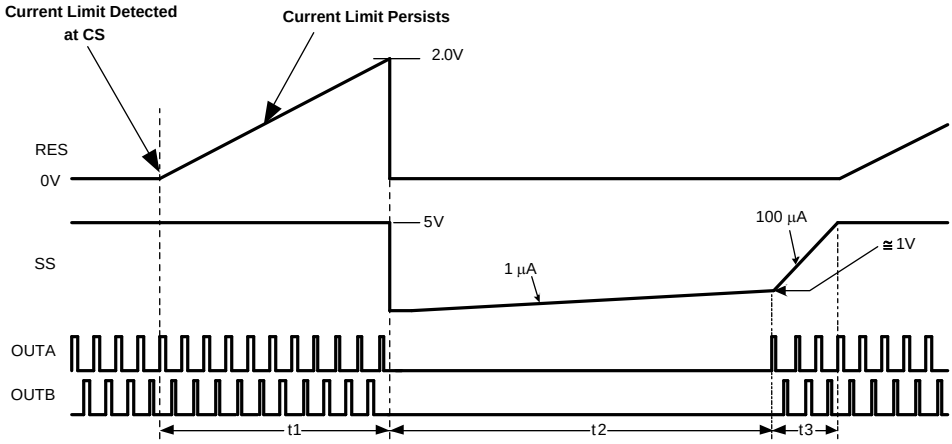


Figure 29. Hiccup Over-Load Restart Timing

In the case of continuous cycle-by-cycle current limit detection at the CS pin, the time required for C_{RES} to reach the 2.0V hiccup mode threshold is:

$$t1 = \frac{C_{RES} \times 2.0V}{18\ \mu A} = 111K \times C_{RES} \quad (8)$$

For example, if C_{RES} = 0.01 µF the time t1 is approximately 2.0 ms. The cool down time, t2 is set by the soft-start capacitor (C_{SS}) and the internal 1 µA SS current source, and is equal to:

$$t2 = \frac{C_{SS} \times 1V}{1\ \mu A} = 1M \times C_{SS} \quad (9)$$

If C_{SS} = 0.01 µF, t2 is ≅10 ms.

The soft-start time t3 is set by the internal 100 µA current source, and is equal to:

$$t3 = \frac{C_{SS} \times 4V}{100\ \mu A} = 40K \times C_{SS} \quad (10)$$

If C_{SS} = 0.01 µF, t3 is ≅ 400 µs.

The time t2 provides a periodic cool-down time for the power converter in the event of a sustained overload or short circuit. This off time results in lower average input current and lower power dissipation within the power components. It is recommended that the ratio of t2 / (t1 + t3) be in the range of 5 to 10 to take advantage of this feature.

If the application requires no delay from the first detection of a current limit condition to the onset of the hiccup mode (t1 = 0), the RES pin can be left open (no external capacitor). If it is desired to disable the hiccup mode entirely, the RES pin should be connected to ground (AGND).

PRINTED CIRCUIT BOARD LAYOUT

The LM5037 Current Sense and PWM comparators are very fast, and respond to short duration noise pulses. The components at the CS, COMP, SS, UVLO, RT2 and the RT1 pins should be as physically close as possible to the IC, thereby minimizing noise pickup on the PC board trace inductances.

Layout considerations are critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of the transformer should be connected via a dedicated PC board trace to the AGND pin, rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor source, low inductance resistors should be used. In this case, all the noise sensitive, low-current ground trace should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point).

While employing current mode control, RAMP pin capacitor and CS pin capacitor must be placed close to the IC. Also, a short direct trace should be employed to connect RAMP capacitor to the CS pin.

The gate drive outputs of the LM5037 should have short, direct paths to the power MOSFETs in order to minimize inductance in the PC board The two ground pins (AGND, PGND) must be connected together with a short, direct connection, to avoid jitter due to relative ground bounce.

If the internal dissipation of the LM5037 produces high junction temperatures during normal operation, the use of multiple vias under the IC to a ground plane can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) will help reduce the junction temperatures. If using forced air cooling, avoid placing the LM5037 in the airflow shadow of tall components, such as input capacitors.

APPLICATION EXAMPLE

The following schematic shows an example of a 50W half-bridge converter controlled by LM5037. The operating input voltage range is 36V to 72V, and the output voltage is 5V. The output current capability is 10 Amps. The converter is configured for feed-forward voltage-mode control. An auxiliary winding of the power transformer is used to raise the VCC voltage to reduce the power dissipation.

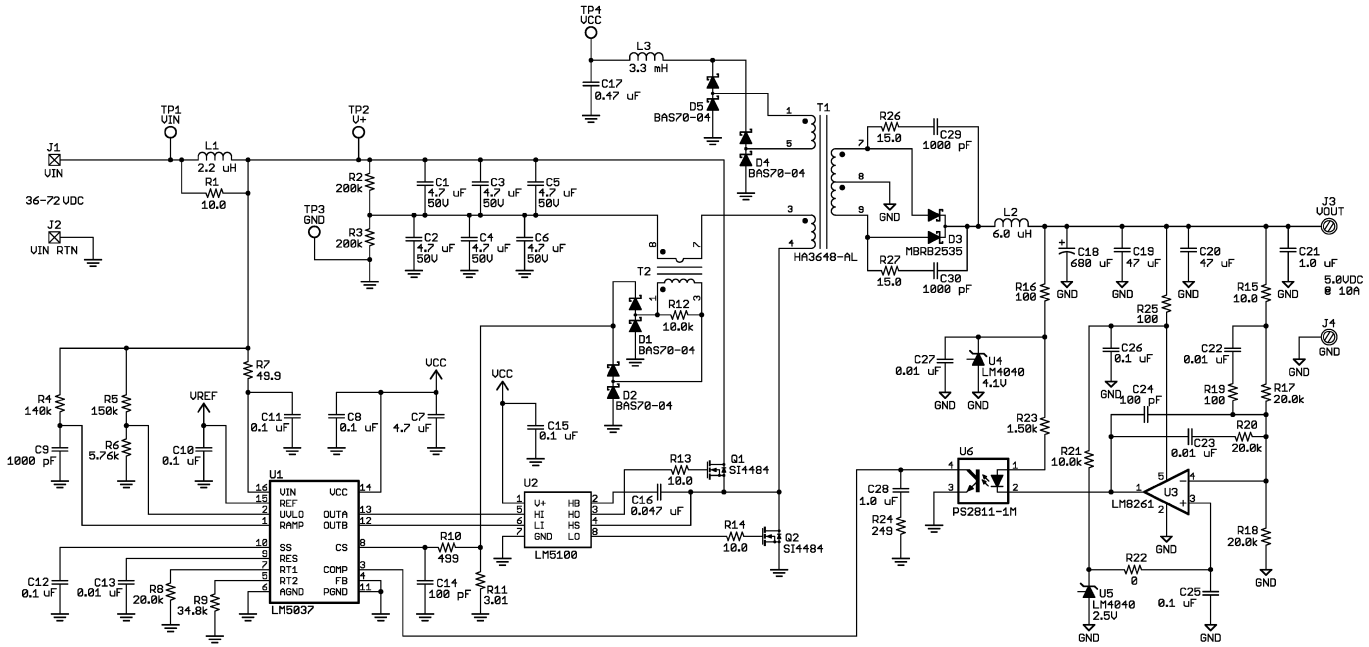


Figure 30. Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM5037MT/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5037 MT	Samples
LM5037MTX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5037 MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

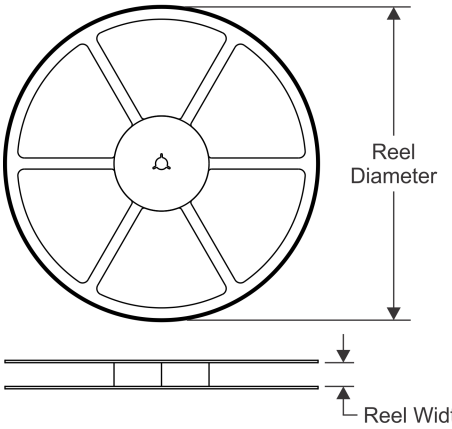
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

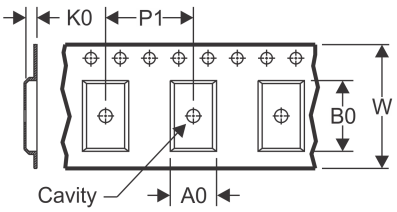
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

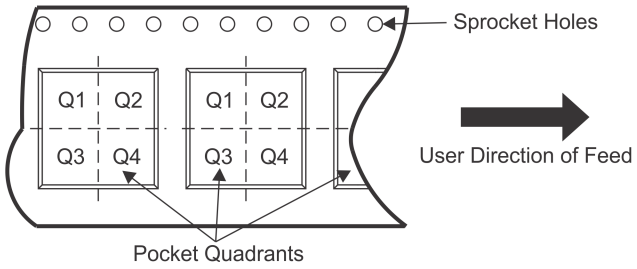


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

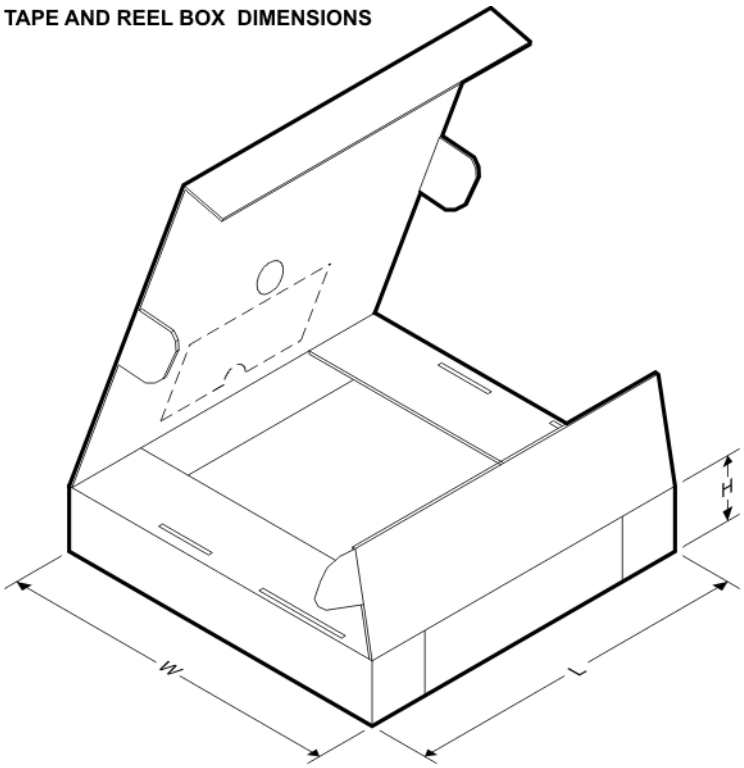
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5037MTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

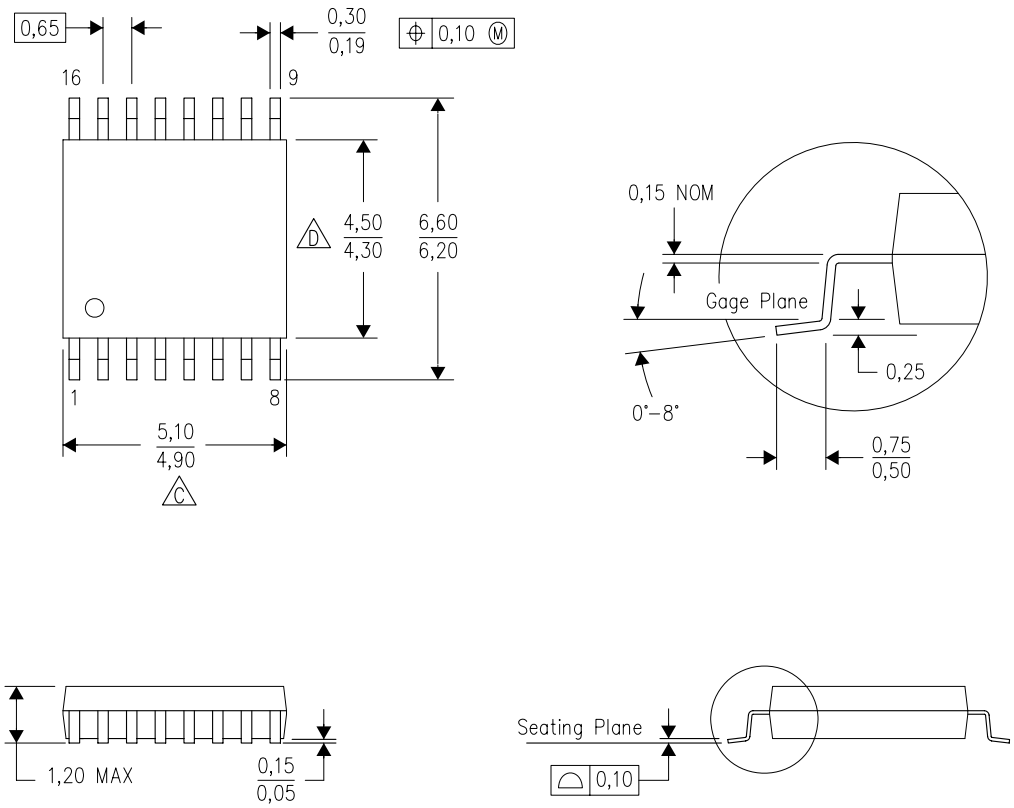
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5037MTX/NOPB	TSSOP	PW	16	2500	349.0	337.0	45.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265