LM3880/LM3880Q Power Sequencer

Check for Samples: LM3880, LM3880Q

FEATURES

- **Easiest Method to Sequence Rails**
- **Power Up and Power Down Control**
- **Input Voltage Range of 2.7V to 5.5V**
- **Small Footprint SOT-23-6**
- **Low Quiescent Current of 25 µA**
- **Standard Timing Options Available**
- **Customization of Timing and Sequence Available through Factory Programmability**
- **LM3880Q is AEC-Q100 Grade 1 Qualified and is Manufactured on an Automotive Grade Flow**

APPLICATIONS

- **Multiple Supply Sequencing**
- **Microprocessor / Microcontroller Sequencing**
- **FPGA Sequencing**
- **Automotive**

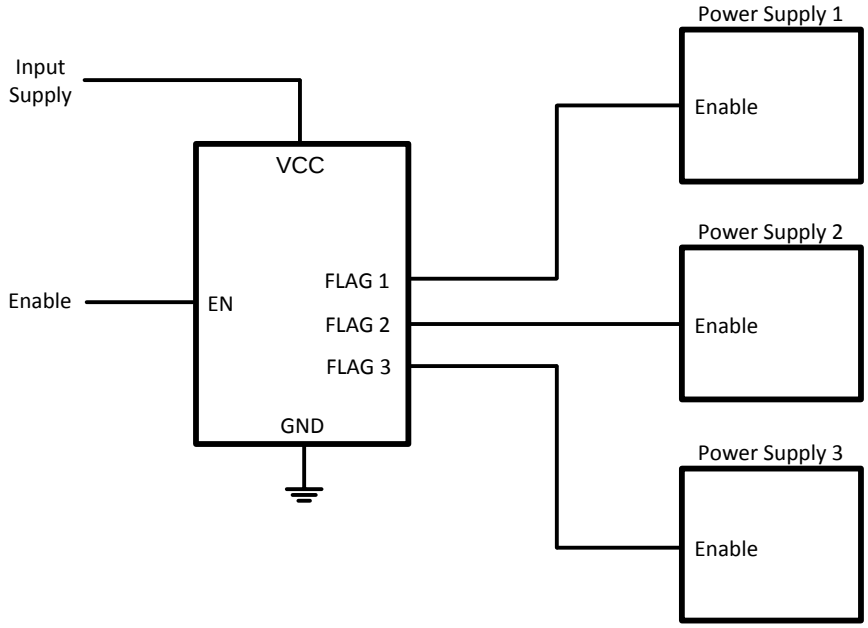
DESCRIPTION

The LM3880 Power Sequencer offers the easiest method to control power up and power down of multiple power supplies (switchers or linear regulators). By staggering the startup sequence, it is possible to avoid latch conditions or large in-rush currents that can affect the reliability of the system.

Available in a SOT-23-6 package, the Power Sequencer contains a precision enable pin and three open drain output flags. Upon enabling the LM3880 the three output flags will sequentially release, after individual time delays, permitting the connected power supplies to startup. The output flags will follow a reverse sequence during power down to avoid latch conditions.

EPROM capability allows every delay and sequence to be fully adjustable. Contact Texas Instruments if a non-standard configuration is required.

Typical Application Circuit



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Connection Diagram

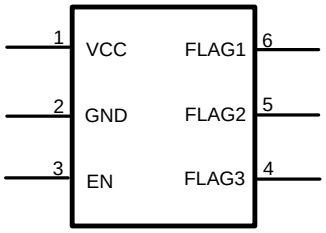

Figure 1. Top View
SOT-23–6 Package

PIN DESCRIPTIONS

Pin #	Name	Function
1	VCC	Input supply
2	GND	Ground
3	EN	Precision enable pin
4	FLAG3	Open drain output #3
5	FLAG2	Open drain output #2
6	FLAG1	Open drain output #1

Table 1. Sequence Designator Table

Sequence Number	Flag Order	
	Power Up	Power Down
1	1 - 2 - 3	3 - 2 - 1
2	1 - 2 - 3	3 - 1 - 2
3	1 - 2 - 3	2 - 3 - 1
4	1 - 2 - 3	2 - 1 - 3
5	1 - 2 - 3	1 - 3 - 2
6	1 - 2 - 3	1 - 2 - 3

Table 2. Timing Designator Table(1)

Timing Designator	t_{d1}	t_{d2}	t_{d3}	t_{d4}	t_{d5}	t_{d6}
AF	16ms	16ms	16ms	16ms	16ms	16ms
AE	2ms	2ms	2ms	2ms	2ms	2ms
AA	10ms	10ms	10ms	10ms	10ms	10ms
AB	30ms	30ms	30ms	30ms	30ms	30ms
AC	60ms	60ms	60ms	60ms	60ms	60ms
AD	120ms	120ms	120ms	120ms	120ms	120ms

(1) See timing diagrams for more information

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)

VCC	−0.3V to +6.0V
EN, FLAG1, FLAG2, FLAG3	−0.3V to 6.0V
Max Flag 'ON' Current	50 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 5 sec.)	260°C
Minimum ESD Rating	±2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

Operating Ratings (1)

VCC to GND	2.7V to 5.5V
EN, FLAG1, FLAG2, FLAG3	−0.3V to V_{CC} + 0.3V
Junction Temperature	−40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those in bold face type apply over the full Operating Temperature Range (T_J = -40°C to +125°C). Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. V_{CC} = 3.3V, and limits apply to all timing options, unless otherwise specified.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Unit
I_Q	Operating Quiescent current			25	**80**	µA
Open Drain Flags						
I_{FLAG}	FLAGx Leakage Current	V_{FLAGx} = 3.3V		1	**20**	nA
V_{OL}	FLAGx Output Voltage Low	I_{FLAGx} = 1.2mA			**0.4**	V
Power Up Sequence						
t_{d1}	Timer delay 1 accuracy		**-15**		**15**	%
		2ms Timing Option	**-20**		**20**	
t_{d2}	Timer delay 2 accuracy		**-15**		**15**	%
		2ms Timing Option	**-20**		**20**	
t_{d3}	Timer delay 3 accuracy		**-15**		**15**	%
		2ms Timing Option	**-20**		**20**	
Power Down Sequence						
t_{d4}	Timer delay 4 accuracy		**-15**		**15**	%
		2ms Timing Option	**-20**		**20**	
t_{d5}	Timer delay 5 accuracy		**-15**		**15**	%
		2ms Timing Option	**-20**		**20**	
t_{d6}	Timer delay 6 accuracy		**-15**		**15**	%
		2ms Timing Option	**-20**		**20**	

(1) Limits are 100% production tested at 25°. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

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Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those in bold face type apply over the full Operating Temperature Range (T_J = -40°C to +125°C). Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. V_{CC} = 3.3V, and limits apply to all timing options, unless otherwise specified.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Unit
Timing Delay Error						
($t_{d(x)}$ – 400 µs) / $t_{d(x+1)}$	Ratio of timing delays	For x = 1 or 4	**95**		**105**	%
		For x = 1 or 4, 2ms option	**90**		**110**	
$t_{d(x)}$ / $t_{d(x+1)}$	Ratio of timing delays	For x = 2 or 5	**95**		**105**	%
		For x = 2 or 5, 2ms option	**90**		**110**	
ENABLE Pin						
V_{EN}	EN pin threshold		**1.0**	1.25	**1.4**	V
I_{EN}	EN pin pull-up current	V_{EN} = 0V		7		µA

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Typical Performance Characteristics

Quiescent Current vs VCC

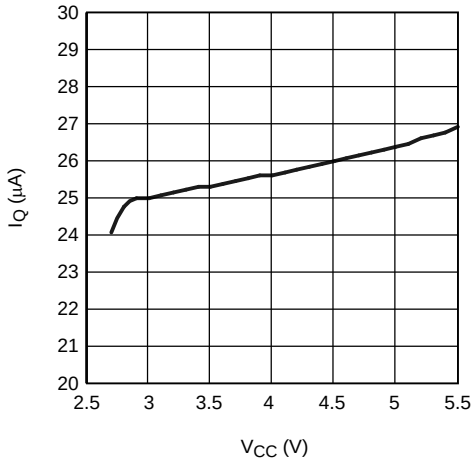

Figure 2.

Quiescent Current vs Temperature (VCC = 3.3V)

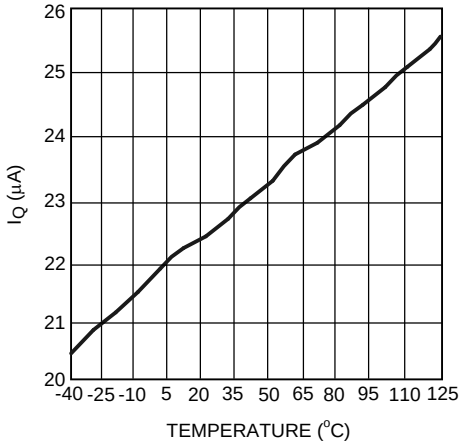

Figure 3.

Enable Threshold vs Temperature

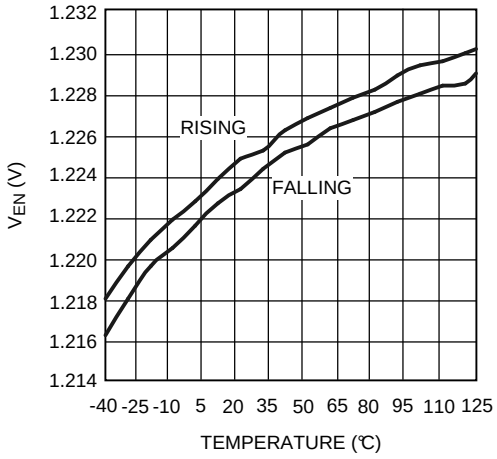

Figure 4.

Time Delay (30ms) vs VCC

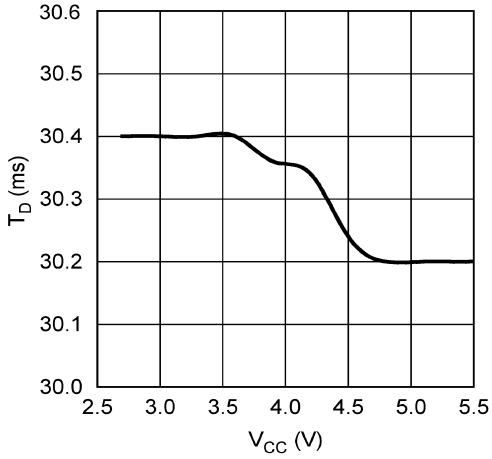

Figure 5.

Time Delay Ratio vs Temperature

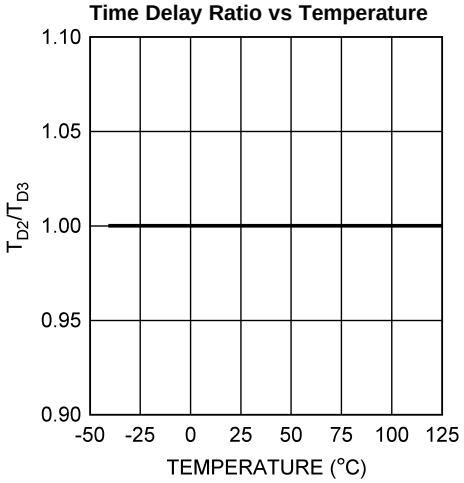

Figure 6.

Time Delay (30ms) vs Temperature

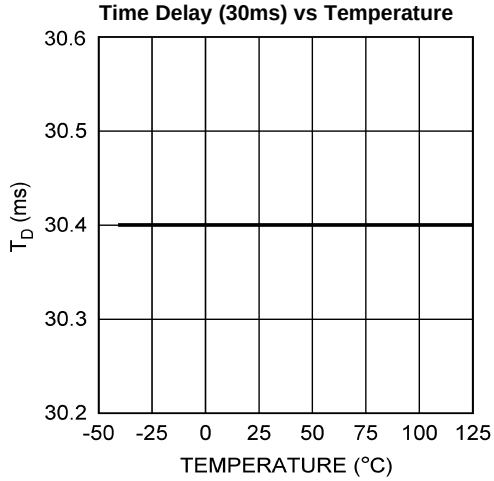

Figure 7.

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Typical Performance Characteristics (continued)

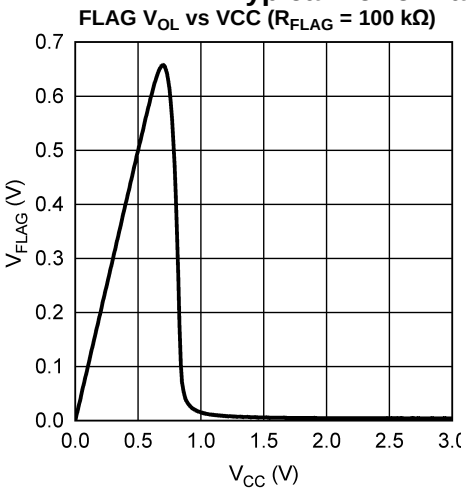

Figure 8.

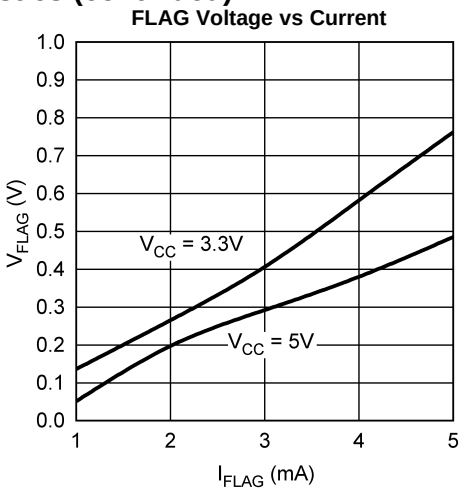

Figure 9.

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Block Diagram

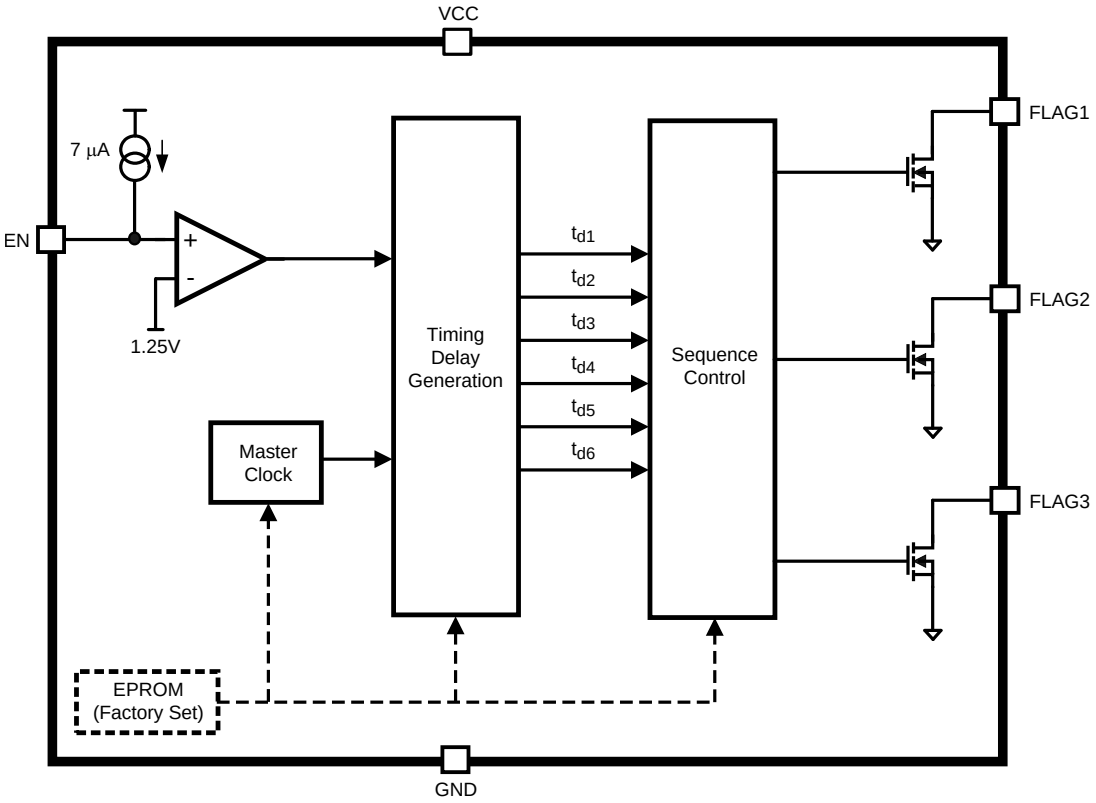

Figure 10. Block Diagram

Timing Diagrams (Sequence 1)

All standard options use this sequence for output flags rise and fall order.

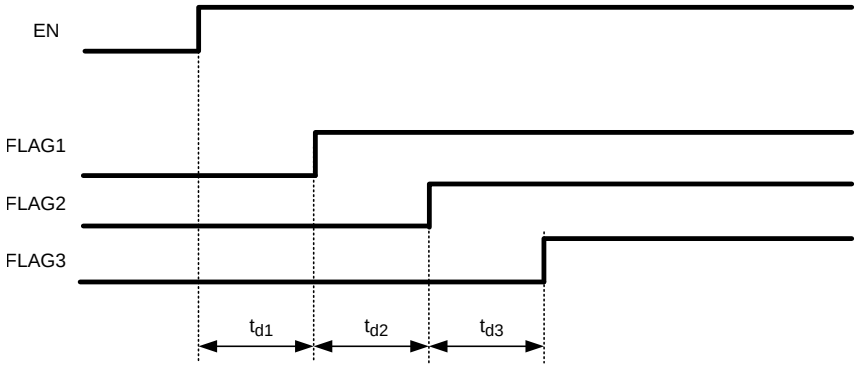

Figure 11. Power Up Sequence

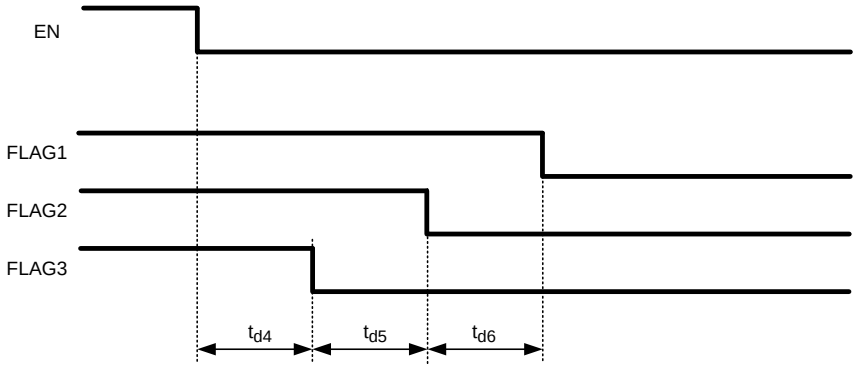

Figure 12. Power Down Sequence

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APPLICATION INFORMATION

OVERVIEW

The LM3880 Power Sequencer provides an easy solution for sequencing multiple rails in a controlled manner. Six independent timers are integrated to control the timing sequence (power up and power down) of three open drain output flags. These flags permit connection to either a shutdown / enable pin of linear regulators and switchers to control the power supplies' operation. This allows a complete power system to be designed without worrying about large in-rush currents or latch-up conditions that can occur.

The timing sequence of the LM3880 is controlled entirely by the enable (EN) pin. Upon power up, all the flags are held low until this precision enable is pulled high. After the EN pin is asserted, the power up sequence will commence. An internal counter will delay the first flag (FLAG1) from rising until a fixed time period has expired. Upon the release of the first flag another timer will begin to delay the release of the second flag (FLAG2). This process repeats until all three flags have sequentially been released. The three timers that control the delays are all independent of each other and can be individually programmed if needed. (See CUSTOM SEQUENCER section).

The power down sequence is the same as power-up, but in reverse. When EN pin is de-asserted a timer will begin that delays the third flag (FLAG3) from pulling low. The second and first flag will then follow in a sequential manner after their appropriate delays. The three timers that are used to control the power down scheme can also be individually programmed and are completely independent of the power up timers.

Additional sequence patterns are also available in addition to customizable timers. For more information see the CUSTOM SEQUENCER section.

PART OPERATION

The timing sequence of the LM3880 is controlled by the assertion of the enable signal. The enable pin is designed with an internal comparator, referenced to a bandgap voltage (1.25V), to provide a precision threshold. This allows a delayed timing to be externally set using a capacitor or to start the sequencing based on a certain event, such as a line voltage reaching 90% of nominal. For an additional delayed sequence from the rail powering VCC, simply attach a capacitor to the EN pin as shown below.

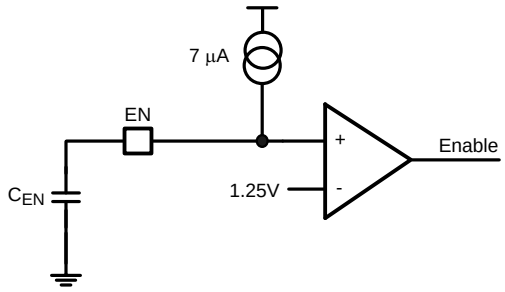

Figure 13. Cap Timing

Using the internal pull-up current source to charge the external capacitor (C_{EN}) the enable pin delay can be calculated by the equation below:

$$t_{enable\_delay} = \frac{1.25V \times C_{EN}}{7\ \mu A} \quad (1)$$

A resistor divider can also be used to enable the LM3880 based on a certain voltage threshold. Care needs to be taken when sizing the resistor divider to include the effects of the internal current source.

One of the features of the enable pin is that it provides glitch free operation. The first timer will start counting at a rising threshold, but will always reset if the enable pin is de-asserted before the first output flag is released. This can be shown in the timing diagram below:

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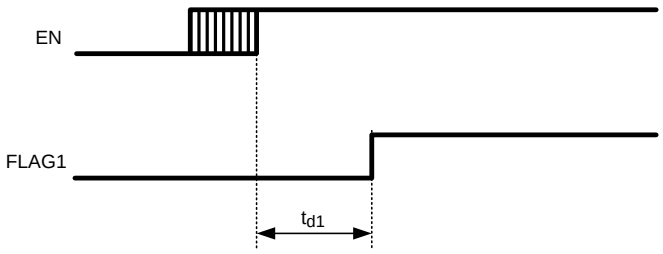

Figure 14. EN Glitch

If the enable signal remains high for the entire power-up sequence, then the part will operate as shown in the standard timing diagrams. However, if the enable signal is de-asserted before the power-up sequence is completed the part will enter a controlled shutdown. This allows the system to walk through a controlled power cycling, preventing any latch conditions from occuring. This state only occurs if the enable pin is de-asserted after the completion of timer 1, but before the entire power-up sequence is completed.

When this event occurs, the falling edge of enable pin resets the current timer and will allow the remaining power-up cycle to complete before beginning the power down sequence. The power down sequence starts approximately 120ms after the final power-up flag. This allows output voltages in the system to stabilize before everything is shutdown. An example of this operation can be seen below:

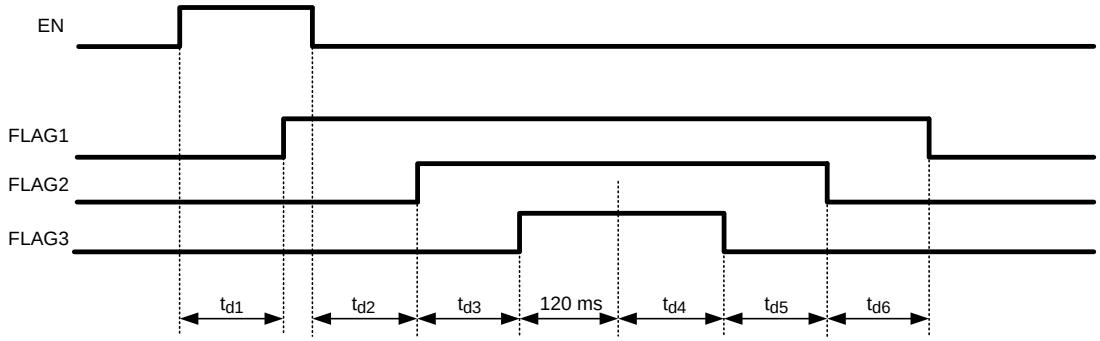

Figure 15. Incomplete Sequence

All the internal timers are generated by a master clock that has an extremely low tempco. This allows for tight accuracy across temperature and a consistent ratio between the individual timers. There is a slight additional delay of approximately 400 µs to timers 1 and 4 which is a result of the EPROM refresh. This refresh time is in addition to the programmed delay time and will be almost insignificant to all but the shortest of timer delays.

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CUSTOM SEQUENCER

The LM3880 Power Sequencer is based on a CMOS process utilizing an EPROM that has the capability to be custom programmed at the factory. Approximately 500,000,000 different options are available allowing even the most complex system to be simply sequenced. Because of the vast options that are possible, customization is limited to orders of a certain quantity. Please contact National Semiconductor for more information.

The variables that can be programmed include the six delay timers and the reverse sequence order. For the timers, each can be individually selected from one of the timer selector columns in the table shown below. However, all six time delays must be from the same column.

Timer Options 1 (1)	Timer Options 2 (1)	Timer Options 3 (1)	Timer Options 4 (1)
0	0	0	0
2	4	6	8
4	8	12	16
6	12	18	24
8	16	24	32
10	20	30	40
12	24	36	48
14	28	42	56
16	32	48	64
18	36	54	72
20	40	60	80
22	44	66	88
24	48	72	96
26	52	78	104
28	56	84	112
30	60	90	120

(1) All times listed are in milliseconds

The sequencing order for power up is always controlled by layout. The flag number translates directly into the sequence order during power up (ie FLAG1 will always be first). However, for some systems a different power down order could be required. To allow flexibility for this aspect in a design, the Power Sequencer incorporates six different options for controlling the power down sequence. These options can be seen in the timing diagrams on the next page. This ability can be programmed in addition to the custom timers.

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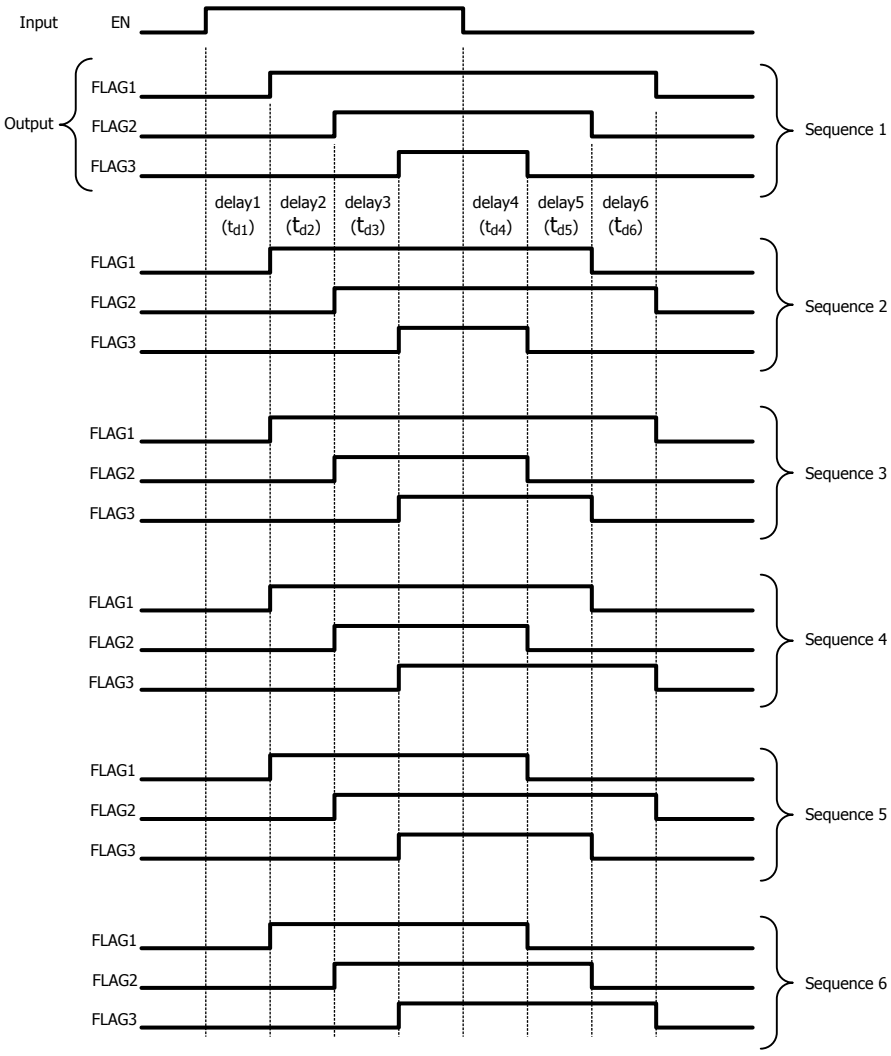

Figure 16. Power Down Sequence Options

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3880MF-1AA	ACTIVE	SOT-23	DBV	6	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	F20A	Samples
LM3880MF-1AA/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F20A	Samples
LM3880MF-1AB/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F21A	Samples
LM3880MF-1AC/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F22A	Samples
LM3880MF-1AD/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F23A	Samples
LM3880MF-1AE/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		F25A	Samples
LM3880MF-1AF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		F31A	Samples
LM3880MFE-1AA/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		F20A	Samples
LM3880MFE-1AB/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		F21A	Samples
LM3880MFE-1AC/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		F22A	Samples
LM3880MFE-1AD/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		F23A	Samples
LM3880MFE-1AE/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		F25A	Samples
LM3880MFE-1AF/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		F31A	Samples
LM3880MFX-1AA/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F20A	Samples
LM3880MFX-1AB/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F21A	Samples
LM3880MFX-1AC/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F22A	Samples
LM3880MFX-1AD/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F23A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3880MFX-1AE/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		F25A	Samples
LM3880MFX-1AF/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		F31A	Samples
LM3880QMF-1AA/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F27A	Samples
LM3880QMF-1AB/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F28A	Samples
LM3880QMF-1AC/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F29A	Samples
LM3880QMF-1AD/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F30A	Samples
LM3880QMF-1AE/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F24A	Samples
LM3880QMF-1AF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F32A	Samples
LM3880QMFE-1AA/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F27A	Samples
LM3880QMFE-1AB/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F28A	Samples
LM3880QMFE-1AC/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F29A	Samples
LM3880QMFE-1AD/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F30A	Samples
LM3880QMFE-1AE/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F24A	Samples
LM3880QMFE-1AF/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F32A	Samples
LM3880QMFX-1AA/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F27A	Samples
LM3880QMFX-1AB/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F28A	Samples
LM3880QMFX-1AC/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F29A	Samples
LM3880QMFX-1AD/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F30A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3880QMFX-1AE/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F24A	Samples
LM3880QMFX-1AF/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F32A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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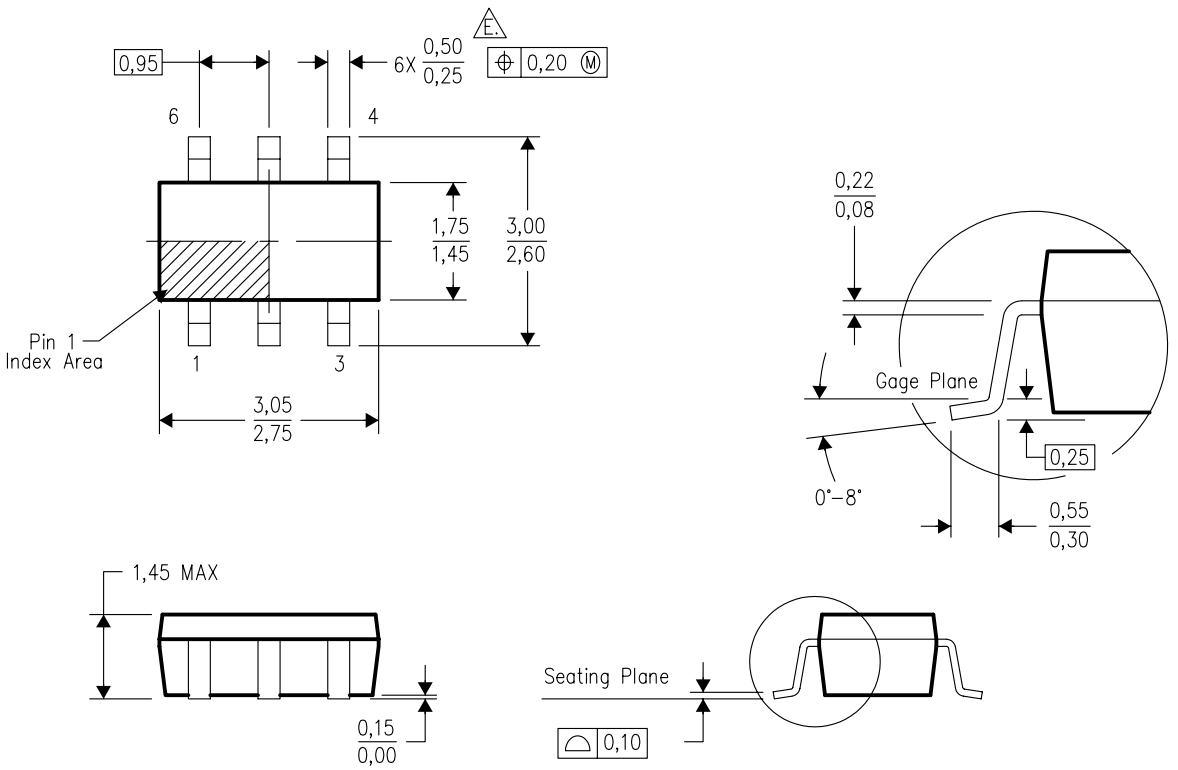
OTHER QUALIFIED VERSIONS OF LM3880, LM3880-Q1 :

- Catalog: LM3880
- Automotive: LM3880-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

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