National Semiconductor

LM1823 Video IF Amplifier/PLL Detector System

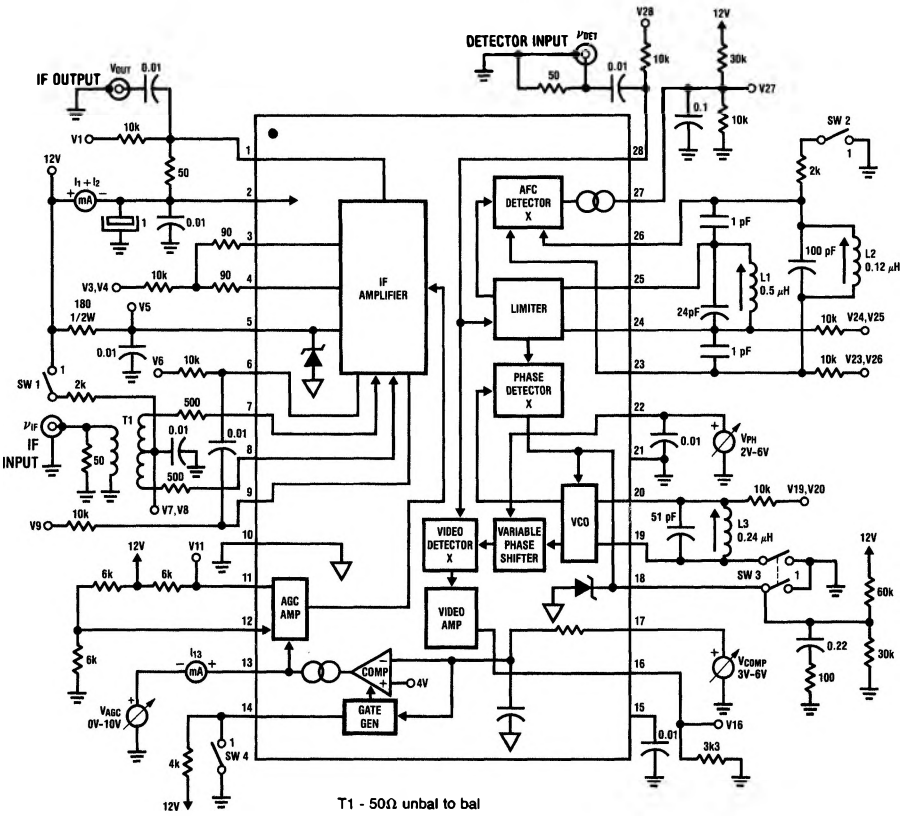
General Description

The LM1823 is a complete video IF signal processing system on a chip. It contains a 5-stage gain-controlled IF amplifier, a PLL synchronous amplitude detector, self-contained gated AGC, and a switchable AFC detector. The increased flexibility of the LM1823 makes it suitable for a wide variety of television applications where high quality video or sound carrier recovery is required. These include home receiver video IFs, cable and subscription TV decoders, and parallel sound IF/intercarrier detector systems. Typical operating frequencies are 38.9 MHz, 45.75 MHz, 58.75 MHz, and 61.25 MHz.

Features

- Low differential gain and phase
- IF and detector pin compatible with LM1822
- Common-base IF inputs for SAW filters
- True synchronous video detector using PLL
- Excellent stability at high system gains
- Noise-averaged gated AGC system
- Uncommitted AGC comparator input
- Internal AGC gate generator
- Superior small-signal detector linearity
- AFC detector with adjustable output bias
- 9 MHz video bandwidth
- Reverse tuner AGC output

Test Circuit Measure parameters at indicated test points



T1 - 50Ω unbal to bal
Mini-Circuits Lab TM01-1T

L1 - 9½T
L2 - 4½T
L3 - 6½T
#22 wire on 3/16" form with HF core, shielded

All caps in µF unless noted

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Order Number LM1823N
See NS Package N28B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage, V2	15V
IF Supply Current, I_5	60mA
AGC Gate Voltage, V14	±5V
Video Output Current, I_{16}	10 mA
PLL Filter Current, I_{18}	5 mA
Detector Input Signal, ν_{DET}	1 Vrms
Power Dissipation	2W
Thermal Resistance, θ_{JA}	50° C/W
Junction Temperature	125°C
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

DC Electrical Characteristics PARAMETERS GUARANTEED BY ELECTRICAL TESTING

$T_A = 25°C$, Test Circuit, $\nu_{IF} = \nu_{DET} = 0$, $V_{PH} = 4V$, $V_{COMP} = 4V$, and all switches in position 0 (open) unless noted.

Parameter	Conditions	Min	Typ	Max	Units
12V Supply Current, $I_1 + I_2$	$V_{AGC} = 6.7V$. $V_{COMP} = 6V$	35	60	80	mA
IF Regulator Voltage, V5	$V_{AGC} = 6.7V$, SW4 Position 1	5.8	6.4	7.0	V
IF Input Voltage, V7, V8	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1	3.2	3.7	4.1	V
IF Decouple Offset, V6–V9	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1		0	±30	mV
IF Peaker Voltage (Max Gain), V3, V4	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1	2.3	3.0	3.6	V
IF Output Current, I1	$V_{AGC} = 9V$, SW 2, 3, 4 Position 1, Measure V1, $I_1 = (12 - V1)/50$	3.1	5.5	7.8	mA
IF Peaker Voltage (Min Gain), V3, V4	$V_{AGC} = 9V$, SW 2, 3, 4 Position 1	5.5	6.2		V
Detector Input Voltage, V28	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.3	4.9	5.5	V
Limiter Tank Voltage, V24, V25	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	6.4	7.0	7.6	V
AFC Tank Voltage, V23, V26	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.3	4.9	5.5	V
VCO Tank Voltage, V19, V20	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.7	5.2	5.7	V
AGC Sync Threshold, V17	SW 1, 2 Position 1, Adjust V_{COMP} for $I_{13} = 0$	3.8	4.0	4.2	V
AGC Filter Leakage Current, I_{13}	SW 1, 2, 4 Position 1		0	±5	μA
AGC Filter Charge Current, I_{13}	SW 1, 2 Position 1, $V_{COMP} = 3.5V$	1.6	2.2	2.8	mA
AGC Filter Discharge Current, I_{13}	SW 1, 2 Position 1, $V_{COMP} = 4.5V$	−0.45	−0.70	−0.90	mA
RF AGC Leakage current, I_{11}	$V_{AGC} = 2V$, All Switches Position 1, Measure V11, $I_{11} = (12 - V11)/6000$		0	20	μA
RF AGC Output Current, I_{11}	$V_{AGC} = 10V$, All Switches Position 1, Measure V11, $I_{11} = (12 - V11)/6000$	1.5	1.8		mA

Detector AC Set-Up Procedure SW 1, 4 position 1, $V_{AGC}=0V$

1. Apply $v_{DET}=10$ mVrms, 45.75 MHz CW at the detector input. Tune L1 for maximum AC signal at pin 25, measured with a 10x FET probe or through a 1 pF capacitor to prevent loading of the limiter tank.
2. Increase v_{DET} to 60 mVrms. Adjust L3 until the PLL locks, as indicated by a DC voltage at the video output pin 16.
3. With the detector locked, adjust L3 for 4.0V at pin 18.
4. Adjust V_{PH} for maximum detector efficiency by monitoring pin 16 for a minimum DC voltage.
5. Adjust L2 for 3.0V at pin 27 (on sensitive slope of AFC curve).

AC Electrical Characteristics PARAMETERS GUARANTEED BY ELECTRICAL TESTING

T_A = 25°C, Test Circuit, detector set-up as above, f = 45.75 MHz, V_{AGC} = 6.7V, V_{COMP} = 4V, and all switches in position 0 (open) unless noted.

Parameter	Conditions	Min	Typ	Max	Units
IF Amplifier Gain, v_{OUT}/v_{IF} (Note 1)	$V_{AGC}=2V$, SW 2, 3, 4 Position 1, $v_{IF}=500\ \mu$Vrms	25	35		dB
V_{AGC} for 15 dB Gain Reduction	SW 2, 3, 4 Position 1, $v_{IF}=2.8$ mVrms, Adjust V_{AGC} for Same v_{OUT} as Gain Test	4.2	4.6	5.0	V
V_{AGC} for 45 dB Gain Reduction	SW 2, 3, 4 Position 1, $v_{IF}=89$ mVrms, Adjust V_{AGC} for Same v_{OUT} as Gain Test	5.1	5.5	6.1	V
Zero Carrier Level, V16	SW 1, 2, 4 Position 1, $v_{DET}=0$	6.6	7.4	8.4	V
Detected Output Level, ΔV16	SW 1, 2, 4 Position 1, $v_{DET}=60$ m/Vrms, Measure Change in V16 from Zero Carrier Test	2	3	4.3	V
Overload Output Voltage, V16	SW 1, 2, 4 Position 1, $v_{DET}=600$ mVrms		2	3	V
AFC Output Voltage (OFF), V27	SW 1, 2, 4 Position 1, $v_{DET}=0$	2.8	3.0	3.2	V
AFC Minimum Output Voltage, V27	SW 1, 4 Position 1, $v_{DET}=60$ mVrms, 46.75 MHz		0.5	1.0	V
AFC Maximum Output Voltage, V27	SW 1, 4 Position 1, $v_{DET}=60$ mVrms, 44.75 MHz	9	10		V
PLL Pull-In Range, Δf	SW 1, 4 Position 1, $v_{DET}=60$ mVrms, Vary Frequency and Measure the Difference between Lock Points	2	3		MHz

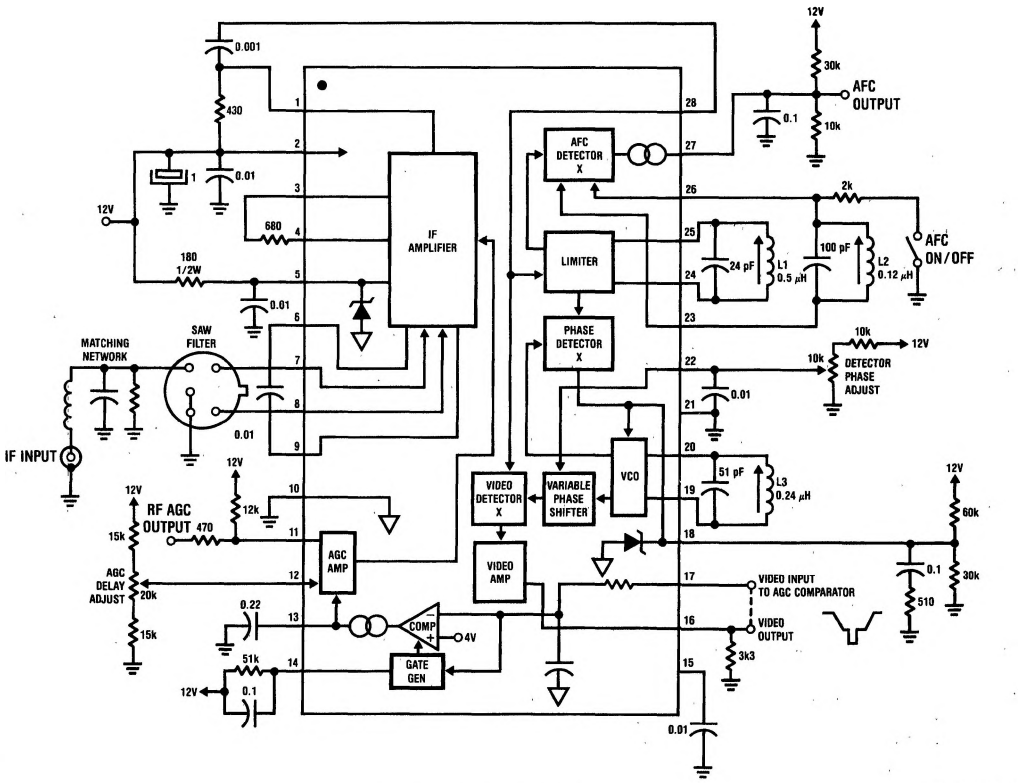
Note 1: The IF amplifier gain is specified with the IF output connected to a 50Ω measurement system which results in a 25Ω loaded impedance. The gain in an actual application will typically be 26 dB higher.

Design Parameters NOT TESTED OR GUARANTEED Typical Application Circuit

Parameter	Typ	Units
Maximum System Operating Frequency	70	MHz
IF Input Impedance (Differential Pin 7–8), 45 MHz	60	Ω
IF Output Impedance, 45 MHz	10	kΩ
IF Gain Control Range	55	dB
Detector Input Impedance, 45 MHz	2	kΩ
Detector Output Bandwidth, −3 dB	9	MHz
Detector Differential Gain (Note 2)	3	%
Detector Differential Phase (Note 2)	1	deg
Detector Output Harmonic Levels below 3 Vp-p Video	−40	dB
VCO Temperature Coefficient	−150	ppm/°C

Note: 2: Differential gain and phase measured with the limiter tank adjusted for minimum differential phase.

Typical Application 45.75 MHz (see Application Notes)



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SAW Filter - MuRata SAF45MC/MA

L1 - 9½T, L2 - 4½T, L3 - 6½T } #22 wire on 3.16" form with HF core, shielded

All caps in μF unless noted

Application Notes Refer to Typical Application Circuit

COMMENTS ON RF Coupling

The LM1823 is a high gain RF system which is critically dependent on the ground plane and positioning of the external components. For this reason, it is suggested that the printed circuit layout shown in *Figure 3* be strictly adhered to.

The most sensitive points in the system to unwanted RF coupling are the IF input pins 6–9. There are two different signals which can cause different problems when coupling into the IF inputs. If the IF output is coupling to the input, it can cause bandpass tilting, peaking, and in extreme cases, oscillation. The other signal which can couple to the IF inputs is the PLL detector VCO. This VCO coupling can cause AFC skewing, non-symmetrical detector pull-in, and failure of the detector to acquire lock at weak signal levels. These input coupling problems will be most acute at maximum gain and will decrease as the IF is gain reduced by AGC action.

The differential IF inputs offer a large amount of inherent rejection to unwanted RF coupling. Therefore, A FULLY BALANCED INPUT SOURCE IS MANDATORY. The input leads must be routed together and socketless operation is recommended above 50 MHz. However, residual coupling may still dictate the maximum IF amplifier gain which can be taken (see Pin Descriptions).

PIN DESCRIPTIONS

Pin 1-IF Amplifier Output: Pin 1 is connected to an open-collector NPN device. The load on pin 1 must be returned to the 12V supply as close as possible to pin 2. The IF output load may be either resistive as shown in the Typical Application, or an LC tank. The tank need only be used if a tunable bandpass characteristic is desired, or in conjunction with a sound trap.

Pin 2–12V Supply: The LM1823 requires a nominal 12V supply but can accept a ±10% variation. Pin 2 must be RF decoupled to a good ground as close as possible to the IC.

Pins 3, 4-IF Gain Adjustment: Pins 3 and 4 are connected to the two emitters of the 4th IF differential amplifier such that the gain of the stage is set by the impedance between the pins. There is an internal 1360Ω resistor to set the minimum gain when the pins are left open. Adding an external resistor increases the gain by the ratio of the parallel impedance to the original 1360Ω. The pin 3 to 4 external resistor primarily affects the maximum IF gain; the relative gain increase goes away over the first 20 dB of AGC.

Pin 5-IF Supply: The IF supply employs an internal 6.4V shunt regulator which is fed by an external dropping resistor from pin 2 to pin 5. RF decoupling from pin 5 to the pin 10 ground plane is critical.

Pins 6–9-IF Input and Decouple Pins: The LM1823 uses a common-base differential input stage as shown in *Figure 1*. Pins 7 and 8 connect directly to the emitters of the input devices, while pins 6 and 9 decouple the DC feedback loop at the bases.

The gain of a common-base amplifier depends inversely on the source impedance. The LM1823 is designed to operate from differential impedances in the 500Ω to 2000Ω range, which is typical for surface acoustic wave (SAW) filters. Alternatively, the IF may be used with a transformer input configuration similar to that shown in the Test Circuit, as long as the required source impedance is maintained. In all cases a balanced source must be used.

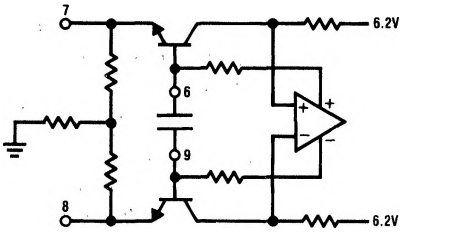

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FIGURE 1. IF Input Stage

Both the input network to pins 7 and 8 and decoupling capacitor between pin 6 and pin 9 must be as close to the device as is physically possible to minimize RF coupling.

Pin 10-IF Ground: Pin 10 grounds the IF and AGC circuits in the LM1823. It is separate from the detector and chip substrate grounds to prevent internal coupling.

Pin 11-RF AGC Output: Pin 11 is connected to an open-collector NPN device. It begins to conduct current when the voltage on the AGC filter capacitor at pin 13 exceeds the voltage set at the takeover pin 12 by approximately 0.6V. When connected to a resistor to 12V, this produces a falling voltage at pin 11 suitable for reverse tuner AGC inputs.

Pin 12-RF AGC Takeover Adjust: The voltage preset at pin 12 determines when the IF stops gain reducing and the tuner begins gain reducing as the pin 13 AGC filter capacitor voltage increases with signal level. A higher voltage at pin 12 delays the RF AGC takeover until more IF gain reduction has been taken (higher signal levels), while a lower voltage limits the IF gain reduction before RF takeover.

When the LM1823 is being used without a tuner, pin 12 may be connected to supply.

Pin 13-AGC Filter: Pin 13 is a push-pull current source output from the AGC comparator. The comparator compares the negative sync tips of noise-averaged pin 17 video with an internal 4V reference. Increases in signal produce a current out of pin 13 which charges the filter capacitor, while decreases discharge the capacitor. The resulting change in voltage at pin 13 controls the IF and tuner gains to maintain the pin 17 sync tip level at 4V. An optional capacitor between pin 13 and the takeover pin 12 couples the ripple produced by a rapidly varying signal into the takeover pin to enhance the AGC loop response.

Pin 14-AGC Gate Generator Time Constant: The AGC comparator is gated on during sync time by a pulse from an internal gate generator. The gate pulse which activates the comparator is derived from the sync pulse in the same video which feeds the comparator input (see pin 17 description). An RC time constant on pin 14 determines the slice level on the leading edge of the sync pulse at which the comparator is gated on. This level is approximately $V_{SLICE} = 1/(2RC)$ in millivolts above the sync tip, and should be set at ≤25% of the sync amplitude. Note that V_{SLICE} only determines when the AGC comparator turns on, and is unrelated to the comparator reference.

In the Typical Application, $V_{SLICE} = 100$ mV, or 10% of a 1V sync pulse. Increasing V_{SLICE} improves the AGC recovery from step changes in signal level but increases the risk of video interaction. When modifying the time constant, change the capacitor value only.

Application Notes (Continued) Refer to Typical Application Circuit

Pin 15-Supply Decouple: Pin 15 is an additional connection to the 12V supply to allow RF decoupling on the detector side of the chip.

Pin 16-Video Output: Pin 16 is a Darlington NPN emitter-follower output supplying negative sync video. With no detector input signal the pin 16 voltage sits at the zero carrier level, representing peak white. As the input signal level increases, the pin 16 voltage decreases towards black. The sync pulses are normally the most negative portion of the recovered video.

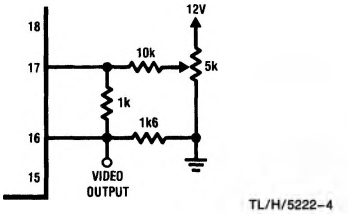

FIGURE 2. Adjustable Recovered Video Level

Pin 17-AGC Comparator Input: External negative sync video is fed to the AGC comparator and gate generator via pin 17. An internal low pass filter removes high frequency noise and transients. The peak-to-peak video level with the AGC loop active is determined by the difference between the zero carrier level at pin 17 and the 4V sync tip level being held by the AGC comparator (see pin 13 description).

When the LM1823 is being used to recover normal video, pin 17 may simply be returned to pin 16. This results in a nominal 3 Vp-p video level, but which is subject to variations in the pin 16 zero carrier level. The network shown in *Figure 2* can be used to change the zero carrier at pin 17, thus providing an adjustable recovered video level. The pin 16 video level should be maintained at between 1 Vp-p minimum and 4 Vp-p maximum.

In suppressed sync systems, the recovered video at pin 16 may require processing to restore normal sync amplitude before being fed to pin 17. In this case, it is mandatory that a DC path be maintained for the zero carrier level through any external circuitry. Any DC level shift between pins 16 and 17 will have the effect of changing the video level as previously described.

Pin 18-PLL Filter: Pin 18 is connected to both the output of the phase detector and the control input of the VCO. The polarity of the VCO control characteristic is such that increasing the pin 18 voltage increases the VCO frequency. An external resistive divider at pin 18 serves two functions. The divider parallel impedance sets the gain of the phase detector, while the divider ratio places the quiescent voltage at the center of the VCO control characteristic. The 20 kΩ impedance, ⅓ supply divider shown in the Typical Application has been chosen to provide optimum performance. The series capacitor and resistor to ground complete the PLL filter.

An internal zener clamp to ground at pin 18 prevents the phase detector output from pulling the VCO control input over 5.6V. For this reason, external voltages should not be forced at pin 18 to avoid damaging the clamp.

Pins 19, 20-VCO Tank: A parallel LC tank between pins 19 and 20 sets the VCO center frequency. The tank Q is RpL/Xc, where RpL is the coil Rp loaded by an internal 1500Ω resistor. Increasing the Q (larger C) improves stability but reduces the VCO control range. The tank shown in the Typical Application will yield a loaded Q of around 15, providing stable operation with a control range in excess of 2 MHz.

Pin 21-Substrate Ground: Pin 21 grounds the chip substrate along with all of the AFC and PLL detector grounds.

Pin 22-Detector Phase Adjust: The video detector requires a reference signal in phase with the input signal carrier for maximum detection efficiency. However, the action of the PLL inherently sets the VCO phase in quadrature (at 90 degrees) with the limiter output. Therefore a variable phase shift network, controlled by pin 22, is used internally between the VCO and video detector to insure proper phasing. Pin 22 requires an adjustment voltage centered at ⅓ supply with ±2V of control range.

The pin 22 adjustment procedure described in the Detector AC Set-Up Procedure is an open loop approach where the voltage is adjusted for maximum detected output with a fixed detector input signal. In the Typical Application, with the detector input being fed from the IF amplifier and the AGC loop active, the pin 22 adjustment is made by maximizing the AGC filter voltage at pin 13. In all cases the detector phase adjustment must be performed after the limiter is tuned.

Pins 23, 26-AFC Tank: A parallel LC tank between pins 23 and 26 sets the center of the AFC characteristic. The internal resistance is typically 20 kΩ, so that Q will be dominated by the coil Rp. The L/C ratio shown in the Typical Application maximizes Q to provide a steep AFC output slope.

A quadrature input signal is required at the AFC tank to operate the AFC detector. This signal is derived by light capacitive coupling from the limiter tank. For applications at 45 MHz and above, the stray printed circuit capacitance from the adjacent limiter tank couples sufficient signal for proper operation. However, at lower IF frequencies, small (1 pF–5 pF) capacitors may be required between the adjacent pins as shown in the Test Circuit.

A second function of pins 23 and 26 allows turning the AFC detector OFF by grounding either side of the AFC tank. Up to 2 kΩ may be placed in series with the switch connection to prevent unbalancing the tank.

Pins 24, 25-Limiter Tank: A parallel LC tank between pins 24 and 25 forms the tuned load for a single stage limiting amplifier which strips amplitude information from the signals feeding the AFC and phase detectors. The amplifier has a small signal gain of approximately 50, with internal Schottky diodes across the tank to limit the output amplitude to 500 mVp-p.

The linearity of the detector video outputs depends directly on limiter tuning. Making the limiter adjustment based on maximum signal level at pins 24, 25 as outlined in the Detector AC Set-Up Procedure results in nearly optimum output linearity. However, to completely null the output differential phase the limiter should be adjusted while monitoring this parameter.

Pin 27-AFC Detector Output: Pin 27 is push-pull current source output from the AFC detector. The polarity is such that pin 27 sources current when the input signal is below the center frequency, and sinks current above the center frequency. An external resistive divider sets both the gain and quiescent output voltage of the AFC. Although the net-

Application Notes (Continued) Refer to Typical Application Circuit

work shown in the Typical Application sets up the output at ¼ supply, it could easily be changed to ½ supply by using equal-valued resistors. When setting up the AFC detector, the tank should always be tuned so the output is at the quiescent divider voltage with the desired center frequency applied.

Pin 28-Detector Input: Pin 28 is internally DC-biased and requires an AC-coupled input signal. The network between pins 1 and 28 should not allow over 1 Vrms at the input during signal transients to prevent overloading the detector. When a tank is being used for the IF output load, a capacitive divider may be used from pin 1 to pin 28 in which the series equivalent capacitance resonates with the coil.

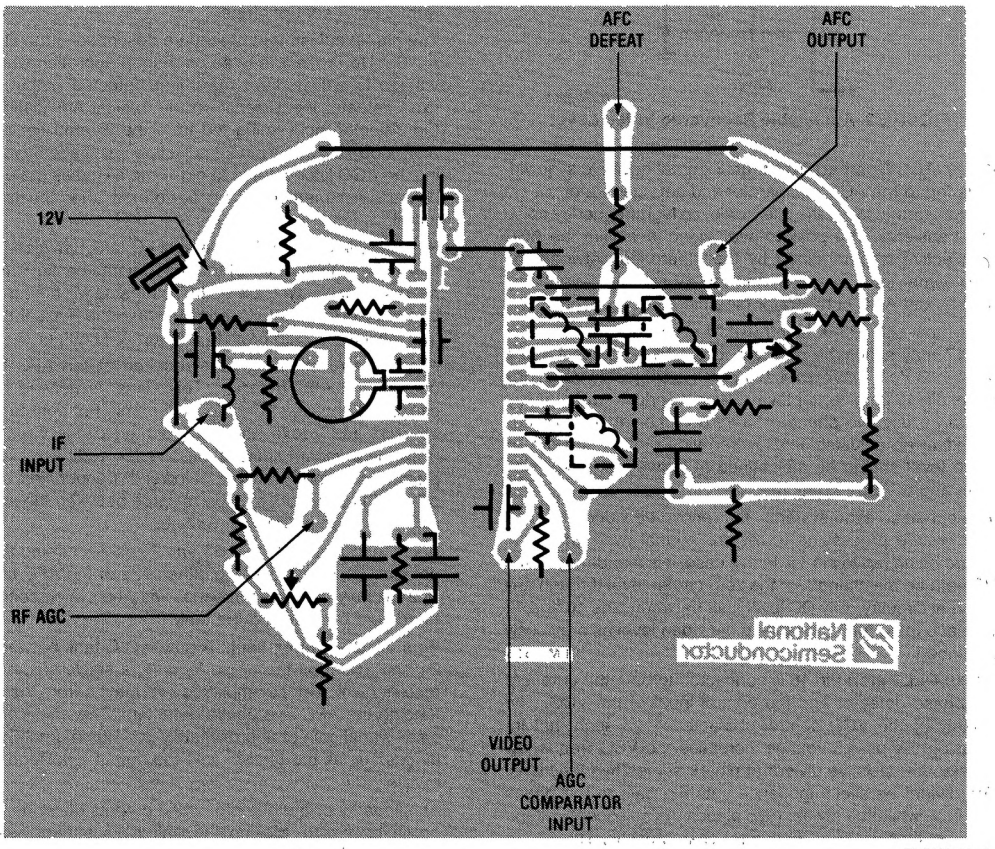

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FIGURE 3. Printed Circuit Layout (Component Side).