National Semiconductor

PRELIMINARY

LM1291
Video PLL System for Continuous Sync Monitors

General Description

The LM1291 is an integrated horizontal time base solution specifically designed to operate in continuous sync video monitors. It accepts all presently defined computer sync signals and generates the drive signal for a horizontal (line) output stage. The system automatically selects the active input based on the following (highest to lowest) priority: (1) separate H and V sync, (2) HV (composite) sync, and (3) composite video. Polarity-corrected H/HV and V sync outputs are provided, along with logic flags which show the respective input polarities.

The IC contains an FVC (frequency-to-voltage convertor) which sets the free-running frequency of the VCO (voltage-controlled oscillator). This technique allows operation over the entire frequency range, 30 kHz–125 kHz, using just one optimized set of external components.

A second phase detector is included which compensates for storage time variation in the horizontal output transistor; the picture's horizontal position is thus independent of temperature and component variance.

The LM1291 provides DC control pins for H Drive duty cycle and H Drive phase.

Features

- VCO precision trimmed on chip—no trimming or loop tuning required
- No costly high-precision components needed
- Low phase jitter (1.3 ns at 100 kHz)
- DC controlled H phase and duty cycle
- Frequency agile—30 kHz to 125 kHz with no external adjustment
- Video mute signal indicates changes in H input frequency
- Input signal prioritization
- Clamp pulse position and width control
- Clamp pulse continues in absence of H sync
- Resistor-programmable minimum and maximum VCO frequency
- X-ray shutdown input
- Under-voltage lockout for $V_{CC} < 9.5V$
- Horizontal output transistor forced off during flyback pulse

Applications

- Horizontal and vertical sync processor for continuous sync monitors
- Wide frequency range phase-locked loop

Connection Diagram

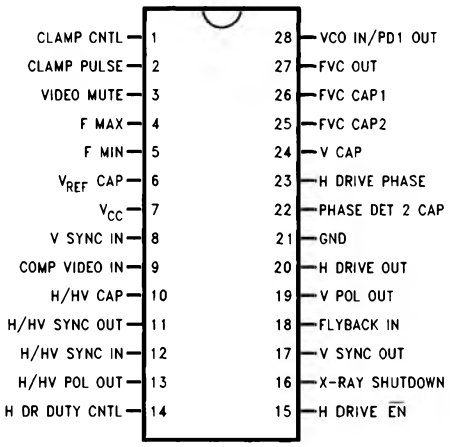

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FIGURE 1

Order Number LM1291N
See NS Package Number N28B

Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	14V
Input Voltage, V_{DC}	
Pins 15, 23	5V
Pins 4, 5	8V
Pins 8, 28	10V
Pins 1, 9, 12, 14, 16, 18	V_{CC}
Power Dissipation (P_D) (Above 25°C Derate Based on θ_{JA} and T_J)	2.5W
Thermal Resistance (θ_{JA})	50°C/W
Junction Temperature (T_J)	150°C
ESD Susceptibility (Note 5)	2 kV
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	265°C

Operating Ratings (Note 2)

Operating Temperature Range	−20°C to +80°C
Supply Voltage (V_{CC})	$10.8V \le V_{CC} \le 13.2V$

Electrical Characteristics See Test Circuit *(Figure 2)*; T_A = 25°C; V_{CC} = 12V

Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units
Supply Current		30	40	mA (max)
Jitter	H Sync frequency = 100 kHz (Note 8)	1.3		ns p-p
Minimum composite video input voltage	Pin 9, cap coupled (0.01 μF), sync tip to black level		0.14	V_{PP} (min)
DC clamp level, composite video input		2.0		V_{DC}
Clamp charging current, composite video input		1		mA
H/HV sync input amplitude	Cap coupled, 10% duty cycle		1.0	V_{PP} (min)
V sync input amplitude	Cap coupled, 1% duty cycle		1.0	V_{PP} (min)
High level output voltage V_{OH}, (Pins 2, 11, 13, 17, 19)	I_{OH} = −100 μA	4.3	4.0	V_{DC} (min)
Low level output voltage V_{OL}, (Pins 2, 11, 13, 17, 19)	I_{OL} = 1.6 mA	0.25	0.4	V_{DC} (max)
Video Mute low level output voltage	I_{OL} = 2 mA		0.4	V_{DC} (max)
Mute detection voltage threshold	ΔV, |FVC Cap 1 − FVC Cap 2| for Mute Output low	100		mV
Flyback input threshold	Positive-going flyback pulse	1.4		V
Under-voltage lockout	V_{CC} below threshold: H Drive Output open (unlatched)	9.5		V
Frequency to voltage gain	30 kHZ ≤ f_H ≤ 125 kHz	0.047		V/kHz
VCO gain constant	f_{VCO} = 100 kHz	1.34×10^5		Rad/s/V
PD1 Phase Detector gain constant	f_{VCO} = 100 kHz	130		μA/Radian
	f_{VCO} = 60 kHz	78.1		
	f_{VCO} = 30 kHz	39.0		
Frequency to voltage linearity	30 kHz ≤ f_H ≤ 125 kHz	1.0		%
VCO linearity	30 kHz ≤ f_{VCO} ≤ 125 kHz	1.0		%

Electrical Characteristics See Test Circuit *(Figure 2)*; T_A = 25°C; V_{CC} = 12V (Continued)

Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units
H Drive duty cycle control gain	DC input 0V–4V; 30%–70% allowed	0.1		T_H/V
H Drive Phase control gain	(Note 9)	47		°/V
PD1 Phase detector leakage current + VCO input bias current			1	μA (max)
H Drive low level output voltage	I_{OL} = 100 mA		0.8	V (max)
H Drive $\overline{EN}$ low level input voltage	H Drive output active		0.8	V (max)
H Drive $\overline{EN}$ high level input voltage	H Drive output open (unlatched)		2.0	V (min)
X-ray Shutdown threshold voltage	Above threshold H Drive Output Open (Latched)	1.72	1.65 1.8	V (min) V(max)
H/HV Sync out propagation delay change	H/HV in vs. Comp Video in	32		ns
Clamp Pulse width	(back porch) R_{SET} = 15k; V_{SET} = 0V	0.4		μs
	(back porch) R_{SET} = 15k; V_{SET} = 1.5V	1.4		μs
	(sync tip) R_{SET} = 15k; V_{SET} = 4V	0.6		μs
Clamp Pulse Delay	(back porch) Trailing edge H/HV Sync In to leading edge clamp pulse	0.1		μs
	(sync tip) Leading edge H/HV Sync In to leading edge clamp pulse	0.025 T_H		s
Internal Ref voltage at pin 6	No load	8.2		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any elevated temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 150°C. The typical thermal resistance (θ_{JA}) of these parts when board mounted follow: LM1291N 50°C/W.

Note 5: Human Body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at $T_A = T_J$ = 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Measured with hp 53310A Modulation Domain Analyzer, 50 ms sample window.

Note 9: Phase limits: $+\left(0.35 - \frac{t_{DFB}}{T_H}\right), -0.15$, expressed as a fraction of the horizontal period T_H, where t_{DFB} is the horizontal output transistor turn-off delay from the rising edge of H Drive to the FBP peak. A positive phase value represents a phase lead of the FBP peak with reference to the leading edge of H sync.

Test Circuit

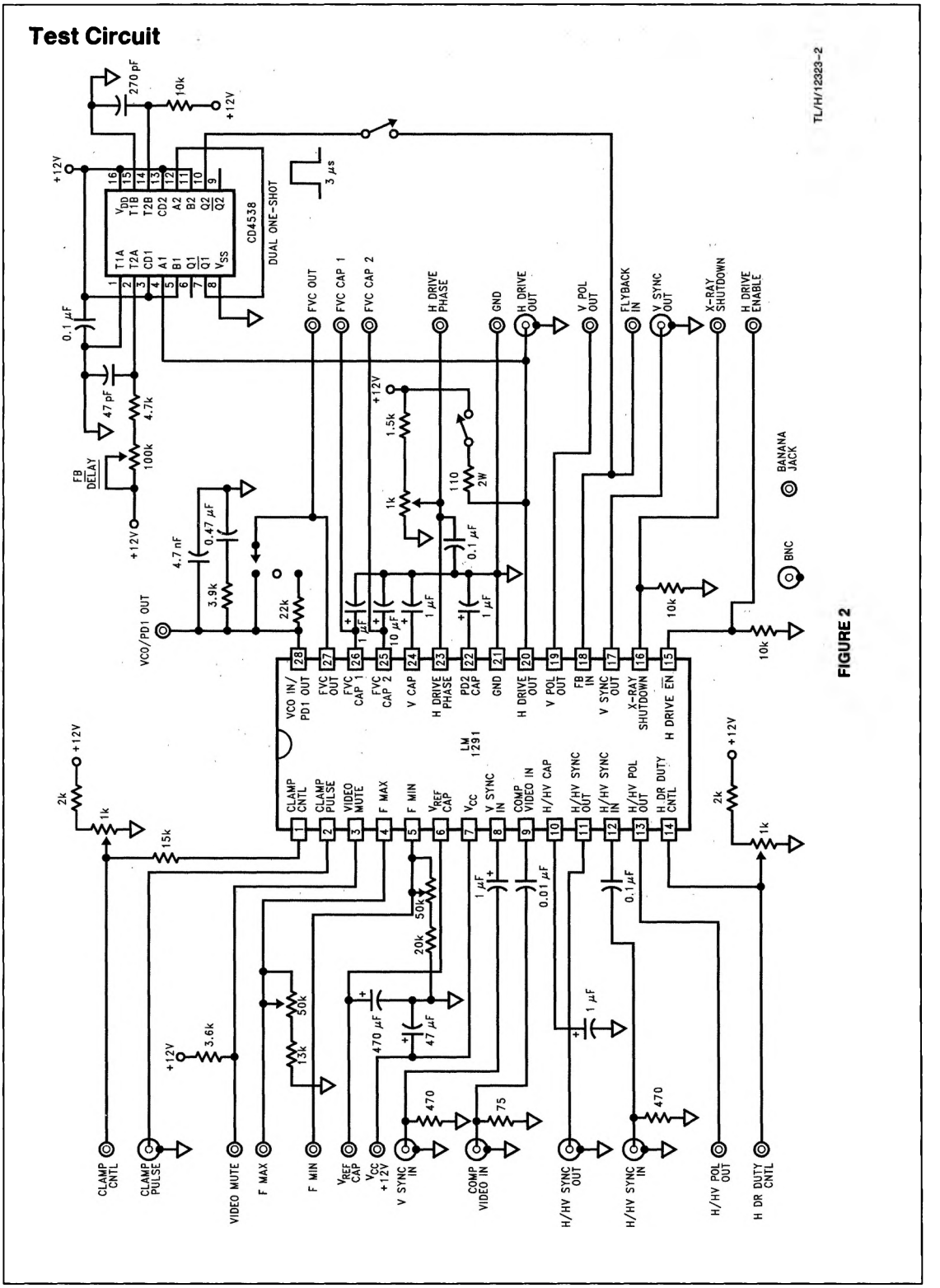

FIGURE 2

Block Diagram

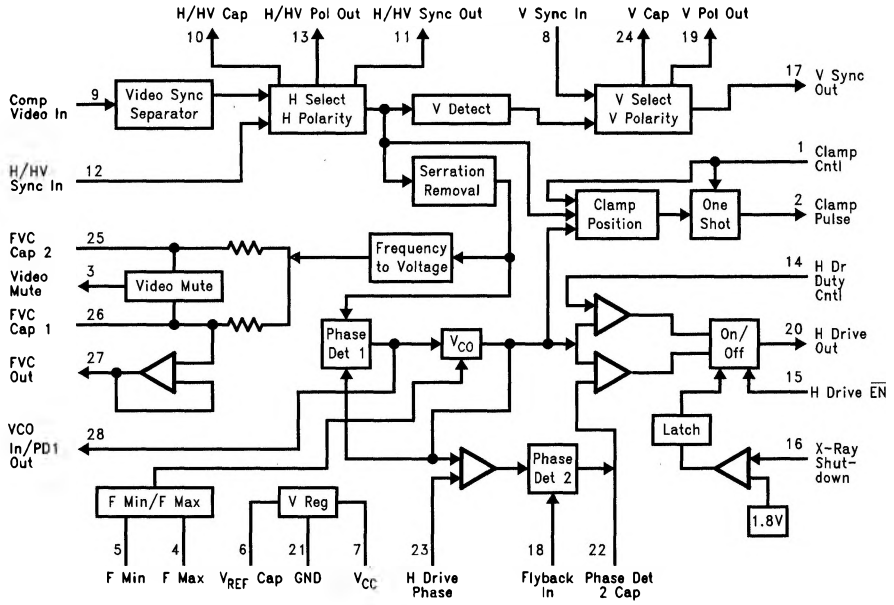

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FIGURE 3

Pin Descriptions

See *Figures 4* through *19* for input and output schematics.

CLAMP CNTL (Pin 1): Clamp Control. See CLAMP PULSE (Pin 2) description. A control voltage of 0V to 4V applied to this pin through a 15k resistor sets the position and width of the negative-going clamp pulse. A voltage below 2V positions the pulse on the back porch of the horizontal sync pulse and decreasing voltage narrows the pulse. A voltage above 2V sets the pulse within the H sync pulse (slightly delayed from the leading edge) and increasing voltage narrows the pulse. At the boundary of the switchover between the two modes, there is a narrow region of uncertainty resulting in oscillation, which should be no problem in most applications. If there is no H Sync and this pin is high, a clamp pulse will be generated from the VCO. This feature is useful with On Screen Displays which must display a message in the absence of sync inputs.

Note: The VCO frequency goes to F MIN in the absence of H sync.

CLAMP PULSE (Pin 2): This output provides a negative-going pulse for DC restoration or clamping in video systems. The pulse can be positioned coincident with the H sync pulse or on the back porch. The pulse width can be adjusted with the clamp control voltage.

VIDEO MUTE (Pin 3): This "open collector" output goes low if there is a sudden change in H sync frequency. It can be used to blank video or for other chores. The rate and amount of frequency change causing Video Mute is set by the values of the capacitors at FVC 1 (Pin 26) and FVC 2 (Pin 25). Video Mute is high in the absence of H sync. See *Figure 5* for the output schematic.

F MAX (Pin 4): Maximum VCO Frequency. A resistor to ground sets the upper limit of the VCO in case of too high H sync frequency. F MAX is approximately $1.8 \times 10^9/(R_{MAX} + 500\Omega)$.

F MIN (Pin 5): Minimum VCO Frequency. A resistor to ground sets the lower limit of the VCO. This is the frequency that the VCO goes to in the absence of H sync. F MIN is approximately $7.5\ kHz + 5.6 \times 10^8/(R_{MIN} + 500\Omega)$.

V_{REF} CAP (Pin 6): This is the output of the internal bandgap based 8.2V reference, which needs bypassing for low noise. The bypass cap should be connected via a short path to pin 21 (ground). The path should not be connected to any part of the circuit that has noise currents. The capacitor should be a minimum of 470 μF aluminum or tantalum electrolytic capacitor.

V_{CC} (Pin 7): V_{CC} (12V nominal) should be bypassed to ground (Pin 21) via a short path with a minimum of 47 μF aluminum or tantalum electrolytic capacitor.

V SYNC IN (Pin 8): Vertical Sync Input. V sync can be a positive or negative going 1.0 V_{PP} minimum signal, capacitively coupled with a 1 μF or larger capacitor. The input resistance is approximately 50k and is biased at 5.2V. V SYNC IN has priority over composite sync and composite video. See *Figure 6* for the input schematic.

COMP VIDEO IN (Pin 9): Composite Video Input. This is the sync input used for composite video; i.e., sync on green, and is the default input when no signals are present at V SYNC IN and H/HV IN. The signal must have negative going sync tips which are at least 0.14V below black level. See *Figure 7* for the input schematic.

Pin Descriptions (Continued)

H/HV CAP (Pin 10): Horizontal Capacitor. The H/HV Cap is the integration cap for the circuit that detects the polarity and existence of the horizontal sync pulses. A 1 μF aluminum or tantalum electrolytic capacitor is recommended.

H/HV SYNC OUT (Pin 11): H/HV Sync Out is the composite sync output. The sync pulses are negative-going with width equal to the sync input. H/HV Sync Out is a low level in the absence of H/HV sync input. This output can drive a standard TTL input and is CMOS compatible. See *Figure 4* for the output schematic.

H/HV SYNC IN (Pin 12): Horizontal or Composite Sync Input. H/HV sync can be a positive or negative-going 1.0 V_{PP} minimum sync signal, capacitively coupled with a 0.1 μF or larger capacitor. The input resistance is approximately 18k into a circuit with clamp levels of approximately 1.9V and 2.6V. See *Figure 8* for the input schematic. if this input is not used, the sync input end of its coupling cap should be connected to ground directly or via a resistor of 470Ω or less.

H/HV POL OUT (Pin 13): H/HV Polarity Out is a DC signal showing the polarity of the H/HV Sync input. A low level indicates positive-going sync, a high level negative-going. The output is low in the absence of H sync. This output can drive a standard TTL input and is CMOS compatible. See *Figure 9* for the output schematic.

H DRIVE DUTY CNTL (Pin 14): Horizontal Duty Cycle Control. A 0V to 4V control voltage applied to this pin sets the duty cycle of the horizontal drive output (pin 20), with a range of approximately 30% to 70%. 2V sets the duty cycle to 50%. See *Figure 10* for the input schematic.

H DRIVE $\overline{\text{EN}}$ (Pin 15): Horizontal Drive Enable. This pin turns the Horizontal Drive Output on and off with a TTL level signal, with low on and high off. See *Figure 11* for the input schematic.

X-RAY SHUTDOWN (Pin 16): This pin turns off the Horizontal Drive Output if its voltage equals or exceeds an internal reference of approximately 1.7V. The output is latched high, and V_{CC} has to be reduced to below approximately 2V to clear the latched condition; i.e., power must be turned off. This feature provides "X-Ray protection" by checking CRT anode voltage level through a resistive divider from a power supply voltage that is proportional to the CRT voltage. See *Figure 12* for the input schematic.

V SYNC OUT (Pin 17): Vertical Sync Out is a negative going pulse occurring approximately 0.3 horizontal lines after the beginning of the vertical interval. V Sync Out is a low level in the absence of vertical sync. V Sync Out width is the same as V Sync In, and is 3 to 5 lines longer for H/HV Sync In and Comp Video In. This output can drive a standard TTL input and is compatible with CMOS. See *Figure 4* for the output schematic.

FLYBACK IN (Pin 18): This is a positive-going pulse from the horizontal deflection circuit that is compared to the VCO phase in phase detector 2, whose output is used to control the phase of Horizontal Drive Out. This compensates for time delay changes in the horizontal deflection circuitry with temperature, etc. to keep the display position constant. See *Figure 13* for the input schematic.

V POL OUT (Pin 19): Vertical Polarity Out is a DC signal showing the polarity of the vertical sync input. A low level indicates positive-going sync and a high level negative-going. The output is low in the absence of vertical sync. This output can drive a standard TTL output and is compatible with CMOS. See *Figure 9* for the output schematic.

H DRIVE OUT (Pin 20): Horizontal Drive Out is a negative-going signal for driving the horizontal deflection system. H Drive Out is an open collector output capable of sinking up to 100 mA. Its duty cycle and its phase with respect to H sync are DC controlled. When the output is low, the horizontal yoke driver is on and when high the driver is off. See *Figure 5* for the output schematic.

GND (Pin 21): System ground. All LM1291 filter components and bypass capacitors should be connected to this pin via short paths.

PHASE DET 2 CAP (Pin 22): Phase Detector 2 Cap is the filter capacitor for the circuit that keeps the phase error between the flyback pulse and H Drive Out constant.

H DRIVE PHASE (Pin 23): A control voltage applied to this pin sets the phase of the flyback pulse with respect to the leading edge of H sync. See *Figure 14* for the input schematic.

V CAP (Pin 24): The Vertical Cap is the integration capacitor for the circuit that detects the polarity and existence of the vertical sync pulses.

FVC CAP 2 (Pin 25): The Frequency to Voltage Converter Capacitor 2 is the filter capacitor for the longer time constant filter for the Video Mute comparator.

FVC CAP 1 (Pin 26): The Frequency to Voltage Converter Capacitor 1 is the filter capacitor for the Frequency to Voltage Converter and is also the shorter time constant filter for the Video Mute comparator.

FVC OUT (Pin 27): The Frequency to Voltage Converter Output is a DC voltage proportional to frequency and is used to set the free-running frequency of the Voltage Controlled Oscillator. This signal goes to the VCO input via a resistor which is part of the PLL filter. The voltage range is approximately 0.6V to 6.0V for 15 kHz to 125 kHz. See *Figure 15* for the output schematic.

VCO IN/PD1 OUT (Pin 28): The Voltage Controlled Oscillator input and Phase Detector 1 output are connected internally at this pin. The phase locked loop filter components are connected here. See Circuit Description for information about this pin.

Input/Output Schematics

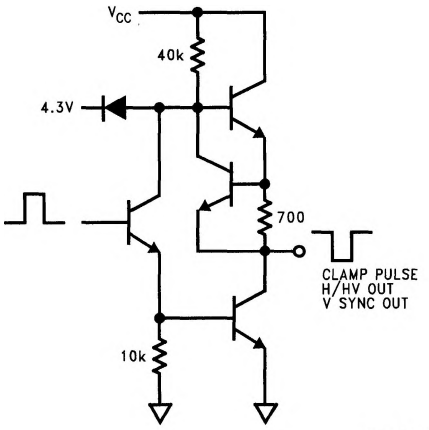

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FIGURE 4

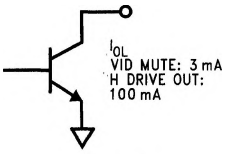

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FIGURE 5

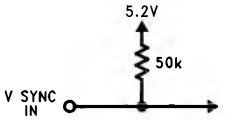

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FIGURE 6

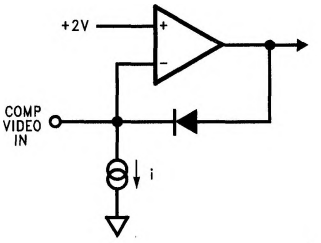

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FIGURE 7

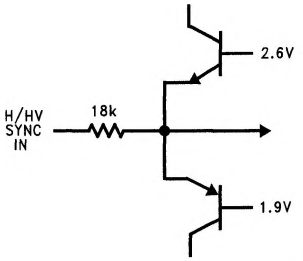

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FIGURE 8

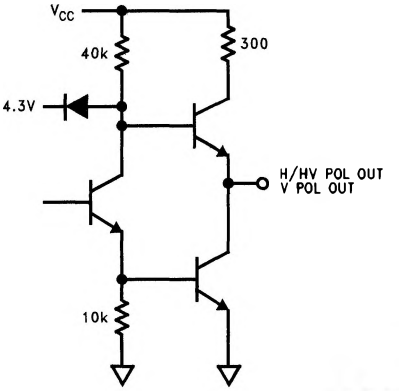

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FIGURE 9

Input/Output Schematics (Continued)

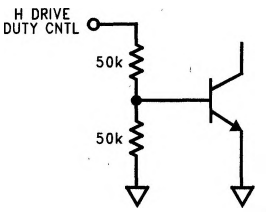

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FIGURE 10

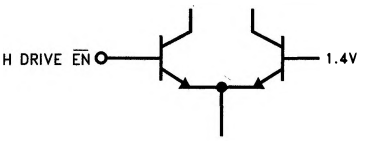

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FIGURE 11

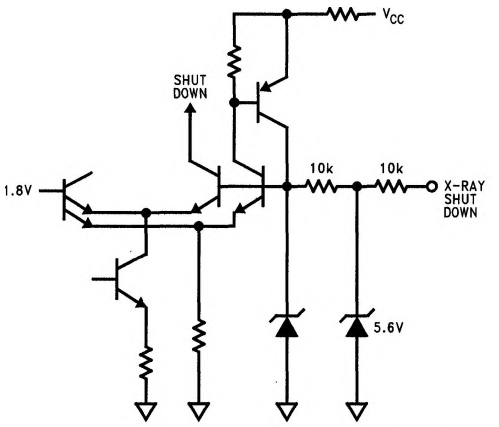

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FIGURE 12

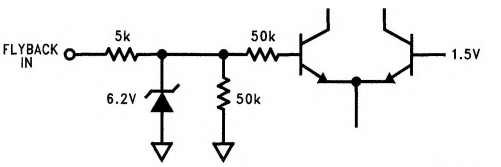

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FIGURE 13

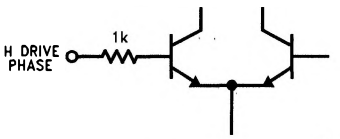

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FIGURE 14

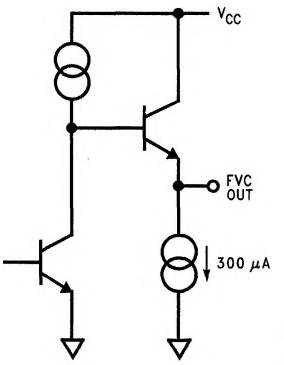

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FIGURE 15

Typical Application

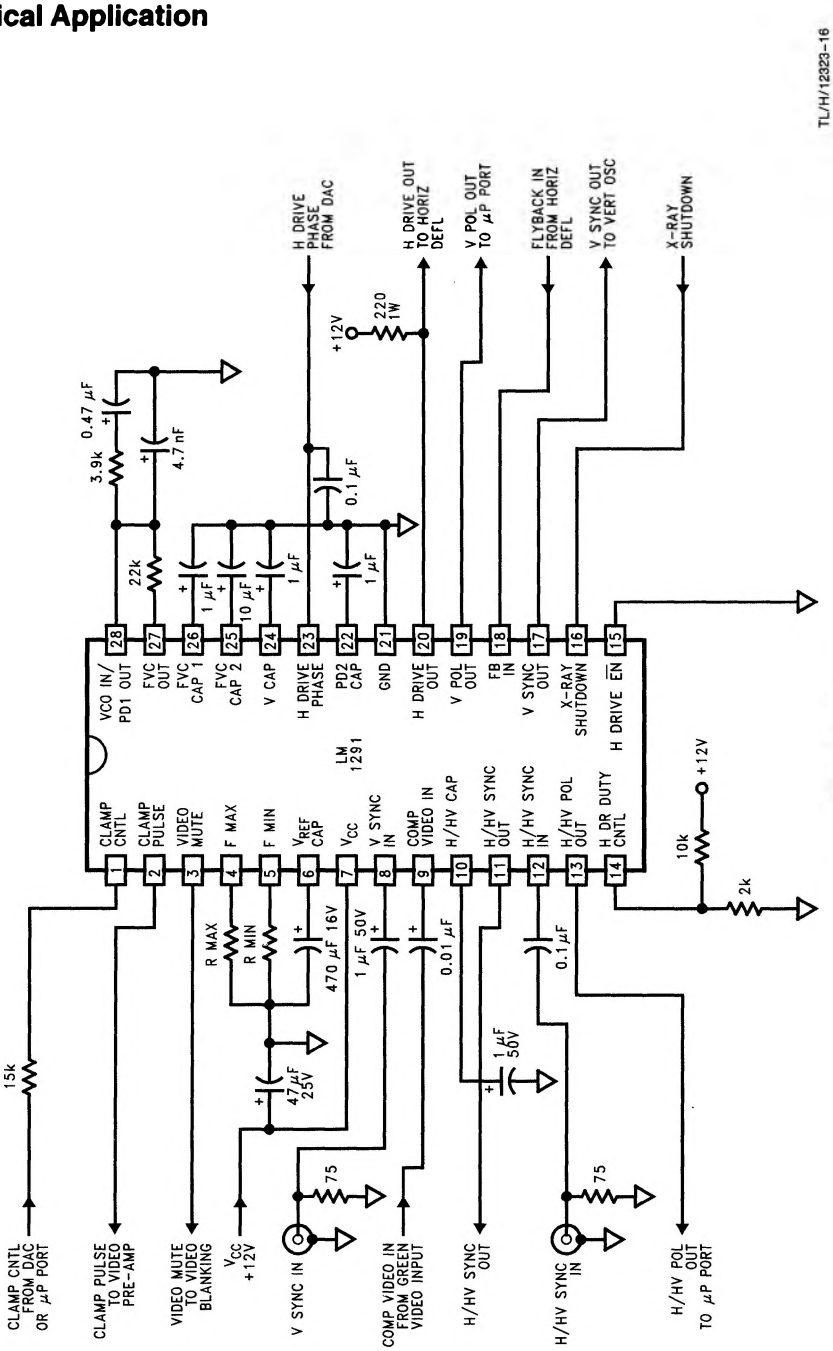

FIGURE 16