LH604256

CMOS 1M (256K × 4) Dynamic RAM

FUNCTION

- 262,144 Words × 4-Bit Dynamic RAM
- Access times: 80/100 ns (MAX.)
- Power supply: +5V ± 10%
- Power consumption (MAX.):
  Operating: 374/340 mW
  Standby: 374/340 mW
- TTL compatible I/O
- Early-write or $\overline{OE}$ control allows bus management of the data-out buffer
- $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh capability
- 512 refresh cycle
  (refresh period (MAX.) = 8 ms)
- Packages:
  20-pin, 300-mil DIP
  26-pin, 300-mil SOJ
  20-pin, 400-mil ZIP

DESCRIPTION

The LH604256 is a 262,144 word × 4 bit dynamic RAM which provides a high-speed page mode operation.

The LH604256 is fabricated using advanced CMOS process technology. With multiplexed address inputs and standard 20-pin DIP/ZIP or 26-pin SOJ packages, it is easy to comprise memory systems with high speed, lower power consumption and large memory capacity. The LH604256 operates on a single 15 V power supply.

PIN CONNECTIONS

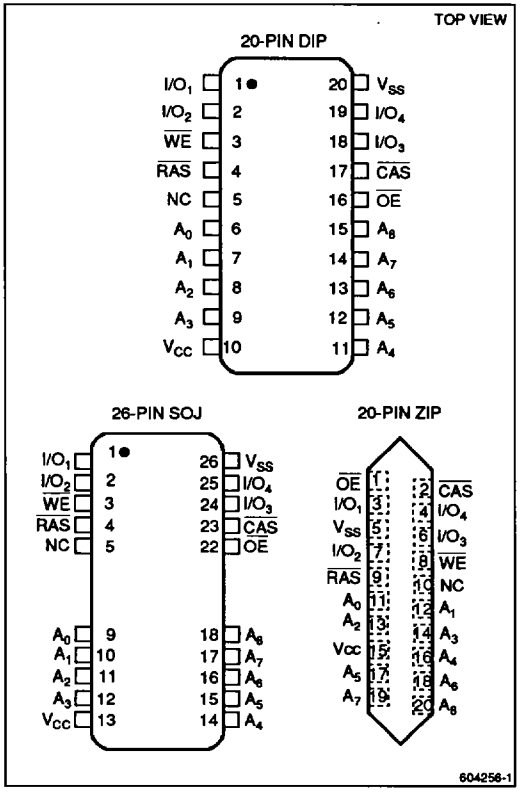

Figure 1. Pin Connections for DIP, SOJ, and ZIP Packages

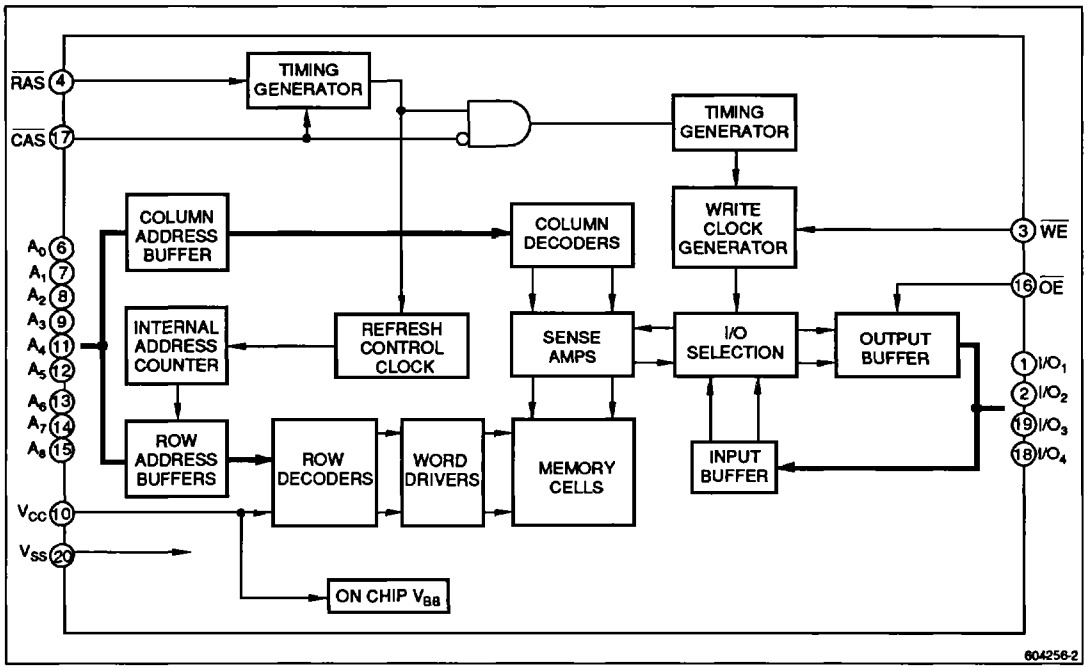

Figure 2. LH604256 Block Diagram

PIN DESCRIPTION

PIN NAME	FUNCTION
A_0 - A_8	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
DQ_1 - DQ_4	Data input/output
$\overline{OE}$	Output enable

PIN NAME	FUNCTION
$\overline{WE}$	Write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground (0 V)
NC	No connection

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	CONDITIONS	VALUE	UNIT
Voltatge on any pin relative to V_{SS}	V_T	T_A - 25°C	-1 to +7.0	V
Short circuit output current	I_{OS}	T_A - 25°C	50	mA
Power dissipation	P_D	T_A - 25°C	1	W
Operating temperature	Topr		0 to +70	°C
Strorage temperature	Tstg		-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}		4.5	5	5.5	V
	V_{SS}		0	0	0	V
Input high voltage	V_{IH}		2.4		6.5	V
Input low voltage	V_{IL}		-1		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		LH604256-80A		LH604256-10A		UNIT	NOTE
				MIN.	MAX.	MIN.	MAX.		
Output high voltage	V_{OH}	I_{OH} = -5 mA		2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V ≤ V_I ≤ 6.5 V all other pins not under test = 0 V		-10	10	-10	10	µA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≤ V_O ≤ 5.5 V		-10	10	-10	10	µA	
Average power supply current (operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.			75		65	mA	1
Power supply current (standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IH} D_{OUT} = Hz	TTL		2		2	mA	1
			MOS		1		1	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min.			75		65	mA	1
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}	$\overline{RAS}$ cycling $\overline{CAS}$ before $\overline{RAS}$			75		65	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$ - V_{IL} $\overline{CAS}$ cycling t_{PC} - min.			65		60	mA	1

NOTE:
1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the outputs open.

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1MHz, T_A = 0 to 70°C)

PARAMETER		SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Input capacitance	A_0 - A_8	C_{IN1}	—	—	6	pF
	$\overline{RAS}$,$\overline{CAS}$,$\overline{OE}$,$\overline{WE}$	C_{IN2}	—	—	7	pF
Input/Output capacitance	I/O_1 - I/O_4	$C_{I/O}$		—	7	pF

AC CHARACTERISTICS [1,2,3] (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH604256-80A		LH604256-10A		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	160	–	–	–	ns	
Read/write cycle time	t_{RWC}	215	–	–	–	ns	
Fast page mode cycle time	t_{PC}	50	–	–	–	ns	
Fast page mode read/write cycle time	t_{PRMW}	105	–	–	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4, 5, 6
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4, 5
Access time from column address	t_{AA}	–	40	–	50	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	7
Write command hold time	t_{WCH}	15	–	20	–	ns	
Write command pulse time	t_{WP}	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	50	–	60	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	110	–	135	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	70	–	85	–	ns	7
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CAS}$ precharge time(Refresh counter test)	t_{CPT}	40	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20	–	20	–	ns	
Access time from $\overline{OE}$	t_{OEA}	–	20	–	25	ns	
$\overline{OE}$ delay time	t_{OED}	20	–	25	–	ns	
$\overline{OE}$ to data output buffer turn-off delay	t_{OEZ}	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20	–	25	–	ns	

See next page for notes.

NOTES:

1. An initial pause of 100 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles. (Examples: $\overline{RAS}$ only Refresh cycle) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (MIN.) and V_{IL} (MAX.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (MAX.) limit insures that t_{RAC} (MAX.) can be met. t_{RCD} (MAX.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (MAX.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (MAX.) limit insures that t_{RAC} (MAX.) can be met. t_{RAD} (MAX.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (MAX.) limit, then access time is controlled exclusiviely by t_{AA}.
7. t_{WCS}, t_{CWL}, t_{RWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle in an early write cycle and the data out pin will remain open circuit (high-impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (MIN.), $t_{RWD} \geq t_{RWD}$ (MIN.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from data out (at access time) is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

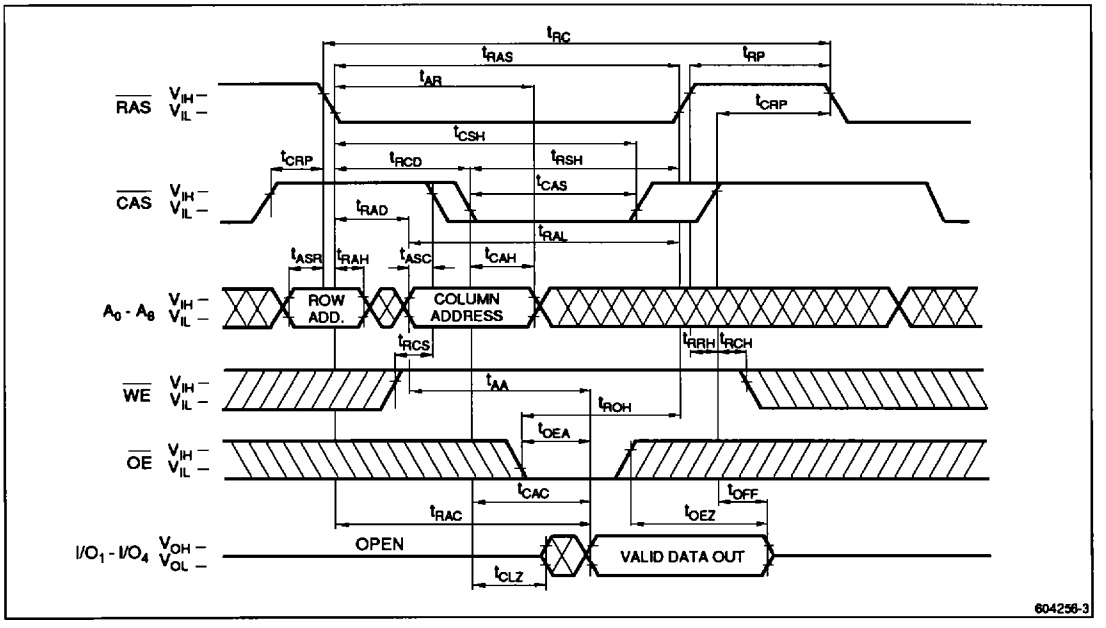

Figure 3. Read Cycle

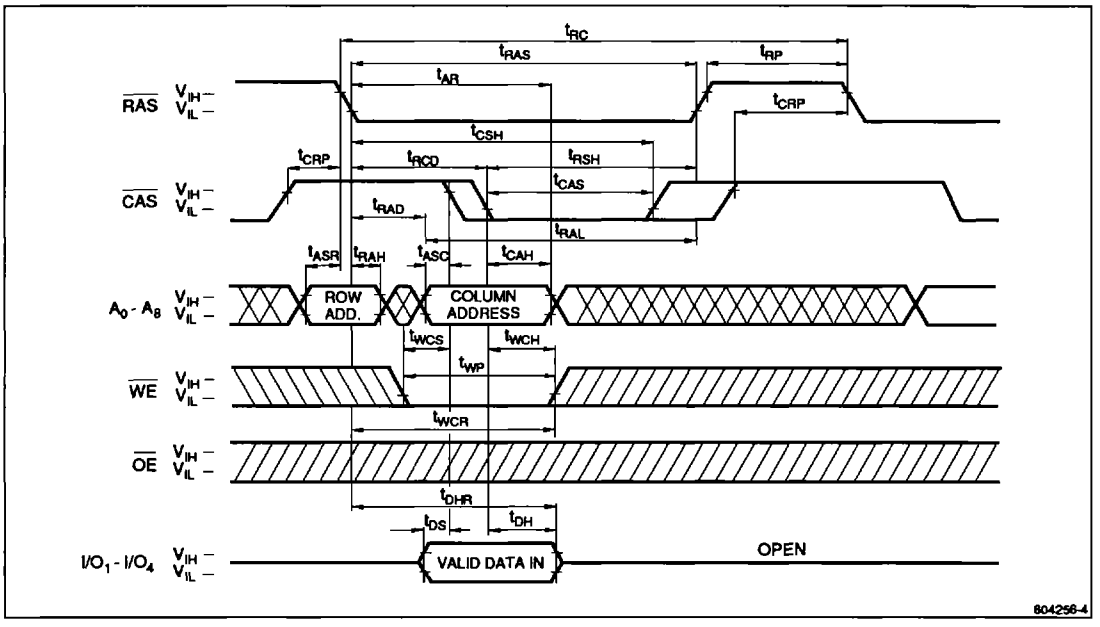

Figure 4. Write Cycle (Early Write)

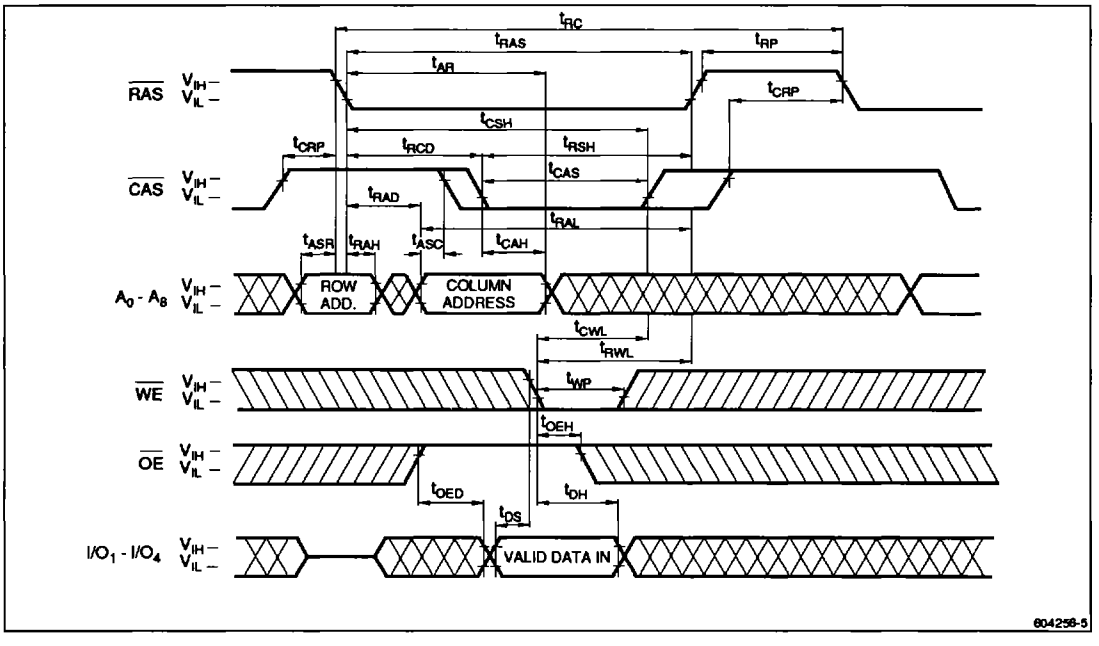

Figure 5. Write Cycle ($\overline{OE}$ Control)

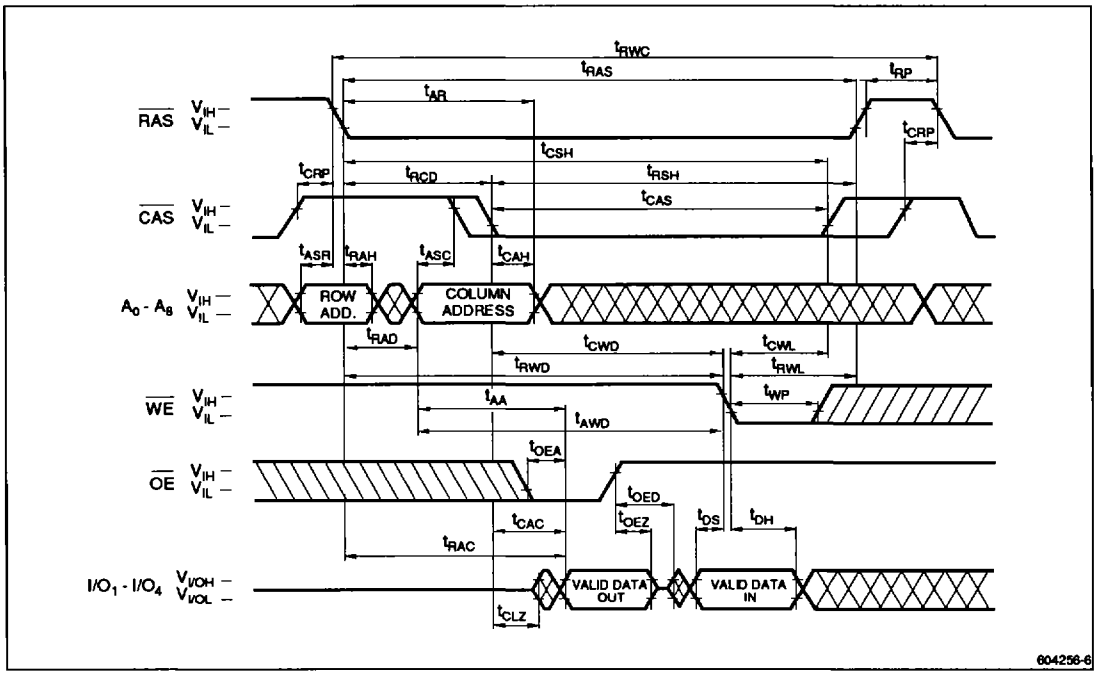

Figure 6. Read/Write, Read-Modify-Write Cycle

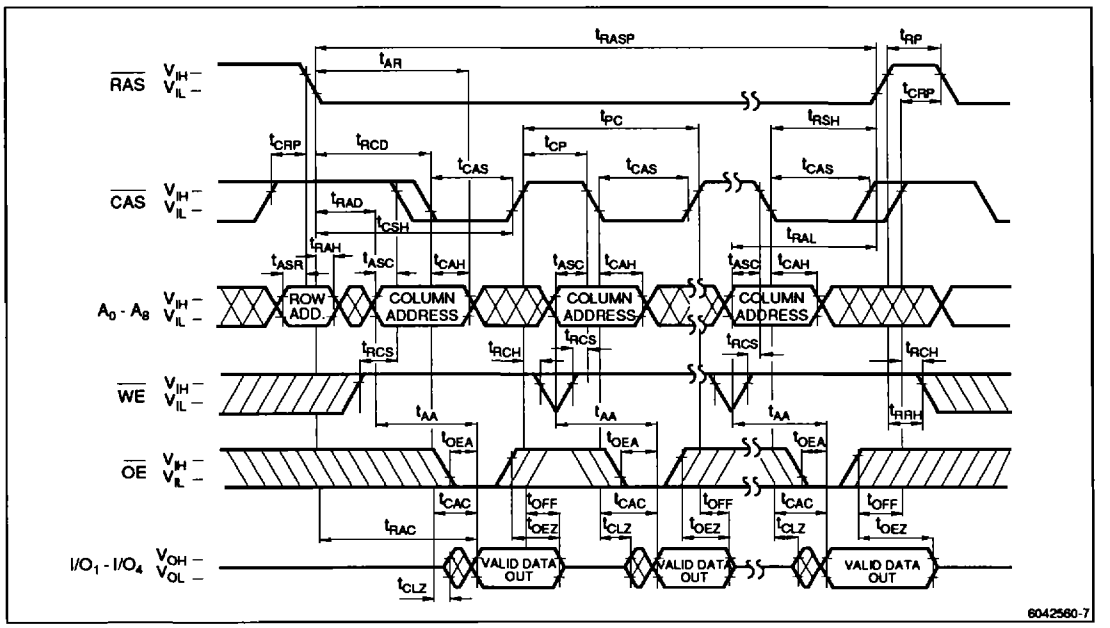

Figure 7. High Speed Page Mode Read Cycle

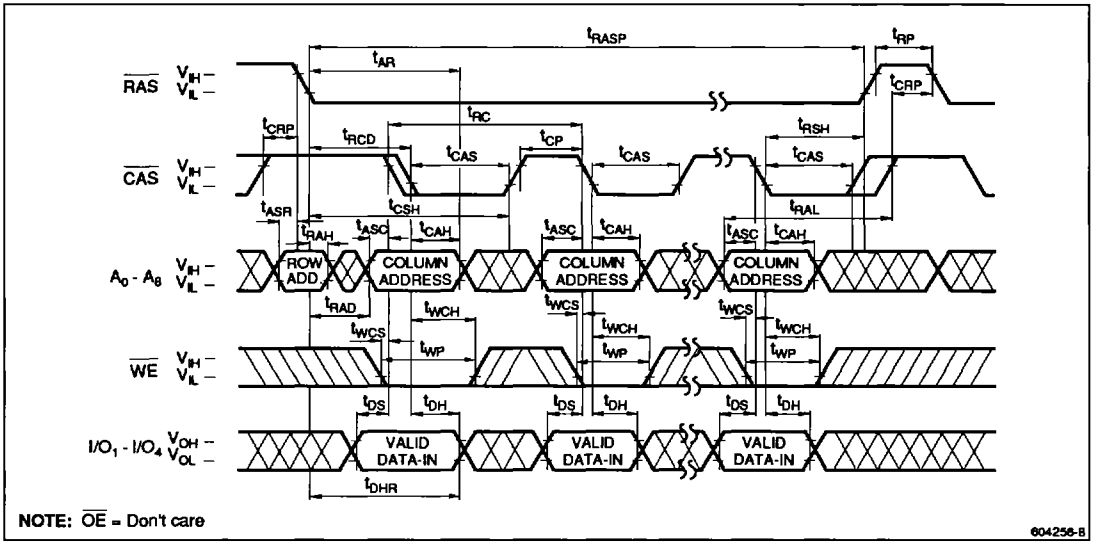

Figure 8. High Speed Page Mode Write Cycle (Early Write)

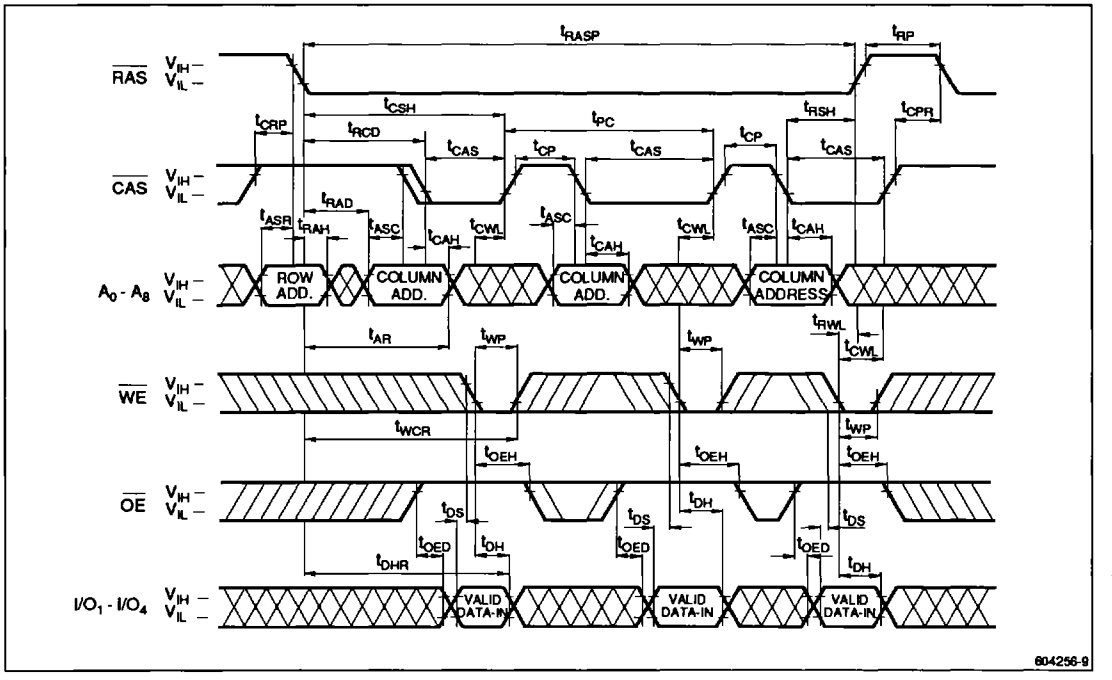

Figure 9. High Speed Page Mode Write Cycle (OE Control)

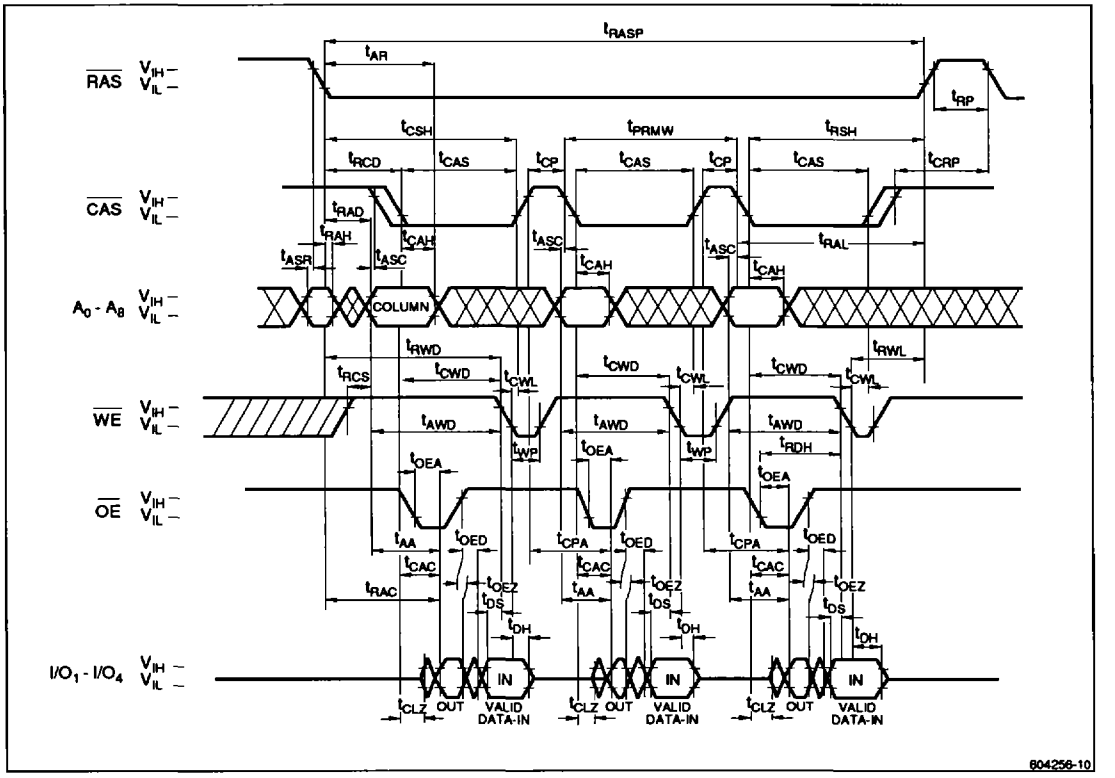

Figure 10. High Speed Page Mode Read/Write Cycle

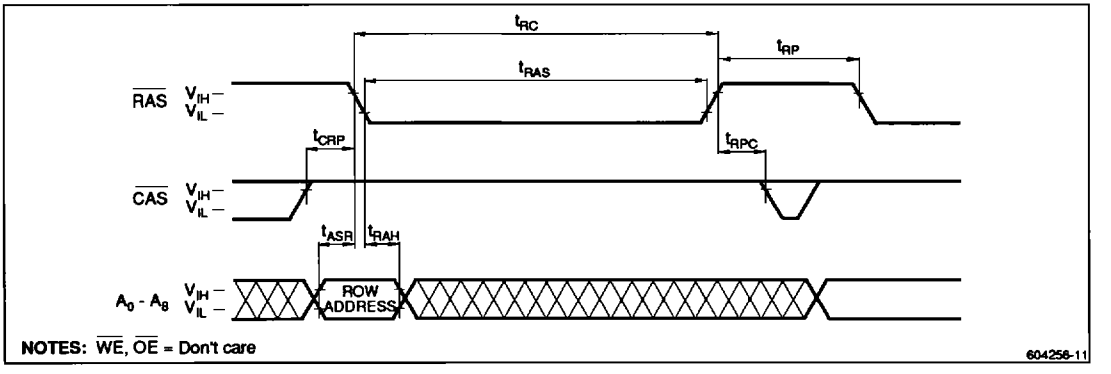

Figure 11. $\overline{RAS}$ Only Refresh Cycle

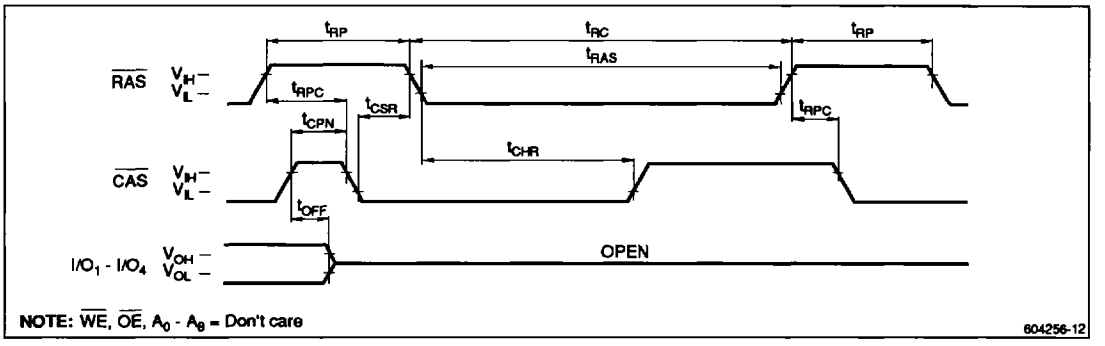

Figure 12. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

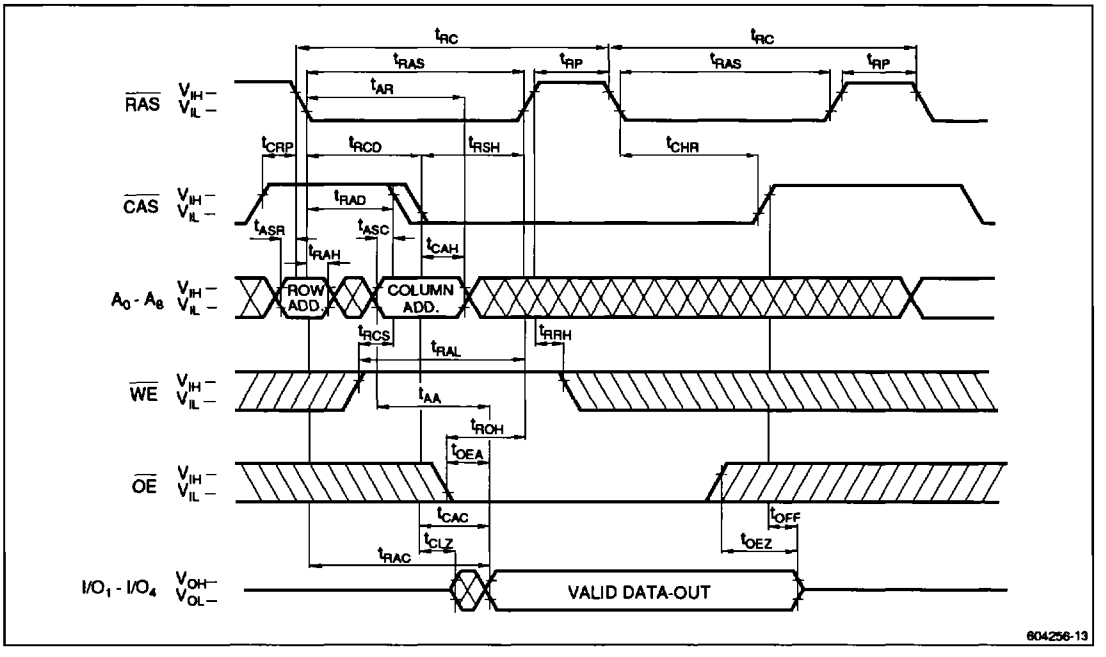

Figure 13. Hidden Refresh Read Cycle

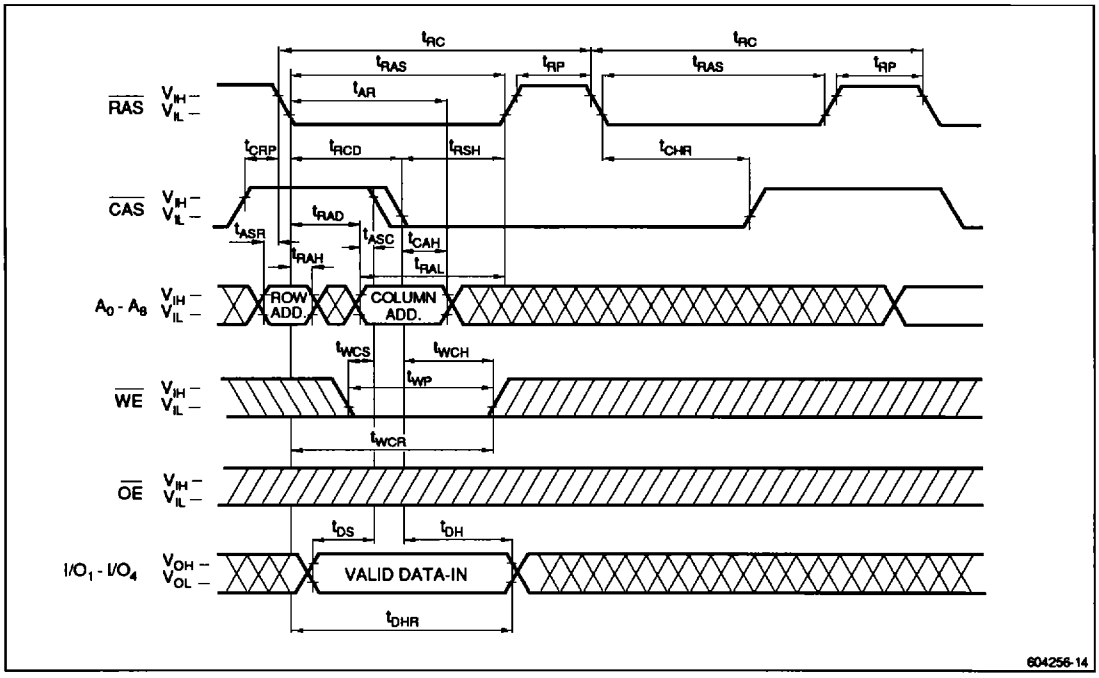

Figure 14. Hidden Refresh Write Cycle

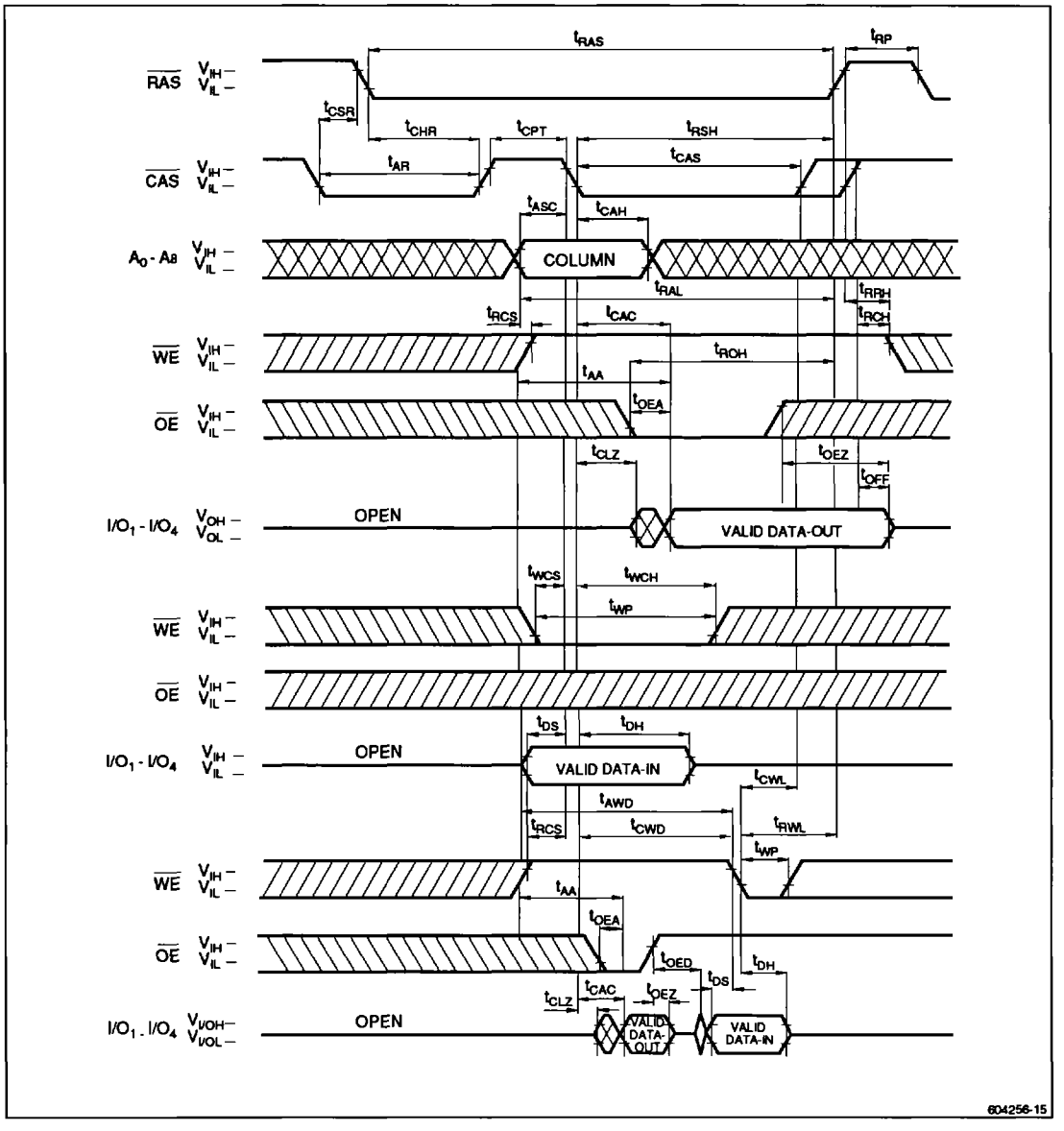

Figure 15. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle

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