PRELIMINARY PRODUCT SPECIFICATIONS

SHARP

Integrated Circuits Group

LH28F128SPHTD-PTL12

Flash Memory

128M (8M × 16/16M × 8)

(Model No.: LHF12P01)

Spec No.: FM033006

Issue Date: March 18, 2003

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To; _____

PRELIMINARY

SPECIFICATIONS

Product Type 128Mbit Flash Memory

LH28F128SPHTD—PTL12

Model No. (LHF12P01)

This device specification is subject to change without notice.

* This specifications contains 30 pages including the cover and appendix.

CUSTOMERS ACCEPTANCE

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  - Office electronics
  - Instrumentation and measuring equipment
  - Machine tools
  - Audiovisual equipment
  - Home appliance
  - Communication equipment other than for trunk lines

  (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

  - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
  - Mainframe computers
  - Traffic control systems
  - Gas leak detectors and automatic cutoff devices
  - Rescue and security equipment
  - Other safety devices and safety equipment, etc.

  (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

  - Aerospace equipment
  - Communications equipment for trunk lines
  - Control equipment for the nuclear power industry
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- Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

LH28F128SPHTD-PTL12
128Mbit (8Mbit×16/16Mbit×8)
Page Mode Flash MEMORY

■ 128-Mbit Density
- Bit Organization ×8/×16

■ High Performance Page Mode Reads for Memory Array
- 120/25ns 4-Word/ 8-Byte Page Mode

■ V_{CC}=2.7V-3.6V Operation
- V_{CCQ} for Input/Output Power Supply Isolation
- Automatic Power Savings Mode Reduces I_{CCR} in Static Mode

■ OTP (One Time Program) Block
- 4-Word/ 8-Byte Factory-Programmed Area
- 3963-Word/ 7926-Byte User-Programmable Area

■ High Performance Program with Page Buffer
- 16-Word/ 32-Byte Page Buffer
- Page Buffer Program Time 12.5µs/byte (Typ.)

■ Operating Temperature -40°C to +85°C

■ Symmetrically-Blocked Architecture
- One-hundred and twenty-eight 64-KWord/ 128-KByte Blocks

■ Enhanced Data Protection Features
- Individual Block Lock
- Absolute Protection with $V_{PEN} \leq V_{PENLK}$
- Block Erase, (Page Buffer) Program Lockout during Power Transitions

■ Automated Erase/Program Algorithms
- Program Time 210µs (Typ.)
- Block Erase Time 1s (Typ.)

■ Cross-Compatible Command Support
- Basic Command Set
- Common Flash Interface (CFI)

■ Extended Cycling Capability
- Minimum 100,000 Block Erase Cycles

■ 56-Lead TSOP (Normal Bend)

■ CMOS Process (P-type silicon substrate)

■ ETOX^{TM*} Flash Technology

■ Not designed or rated as radiation hardened

The product, which is Page Mode Flash memory, is a high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at V_{CC}=2.7V-3.6V and V_{PEN}=2.7V-3.6V

The product supports high performance page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states.

Fast program capability is provided through the use of high speed Page Buffer Program.

The block locking scheme is available for memory array and this scheme provides maximum flexibility for safe nonvolatile code and data storage.

OTP (One Time Program) block provides an area to store security code and to protect its code.

* ETOX is a trademark of Intel Corporation.

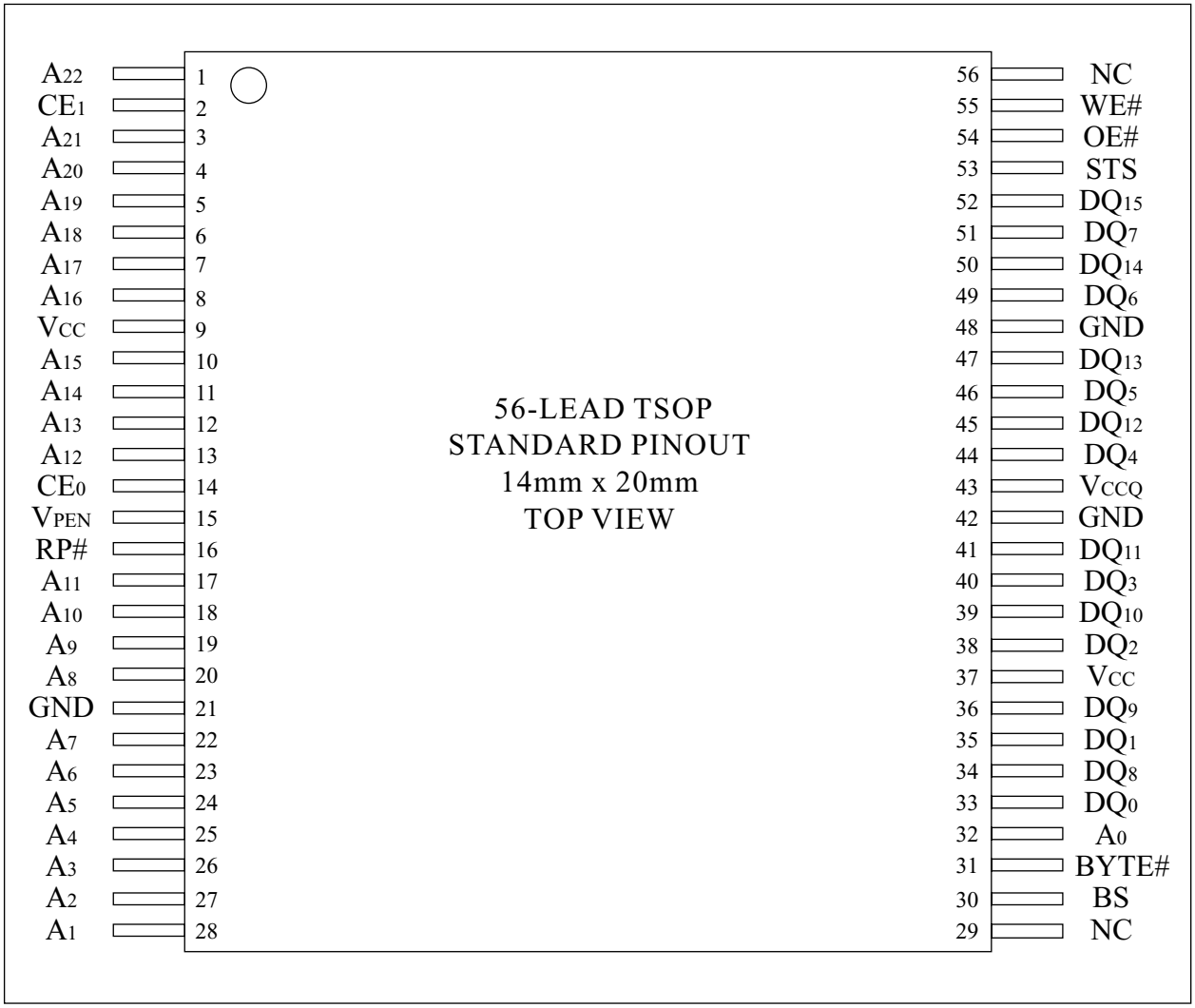


Figure 1. 56-Lead TSOP (Normal Bend) Pinout

Table 1. Pin Descriptions

Symbol	Type	Name and Function
A_0	INPUT	ADDRESS INPUTS: Lowest address input in byte mode (BYTE#=V_{IL} : ×8 bit). Address is internally latched during an erase or a program cycle. This pin is not used in word mode (BYTE#=V_{IH} : ×16 bit)
A_{22}-A_1	INPUT	ADDRESS INPUTS: Inputs for addresses during read, erase and program operations. Addresses are internally latched during an erase or a program cycle.
BS	INPUT	BANK SELECT: Bank 0 is selected by BS=V_{IL}. Bank 1 is selected by BS=V_{IH}.
DQ_{15}-DQ_0	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle. DQ_{15}-DQ_8 pins are not used in byte mode (BYTE#=V_{IL} : ×8 bit).
CE_0, CE_1	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. When the device is de-selected, power consumption reduces to standby levels. Refer to Table 2 to determine whether the device is selected or de-selected depending on the state of CE_0, CE_1 and BS.
RP#	INPUT	RESET: When low (V_{IL}), RP# resets internal automation and inhibits erase and program operations, which provides data protection. RP#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RP# must be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the first edge of CE_0 or CE_1 that disables the device or the rising edge of WE# (whichever occurs first). BS transitions must not occur when CE_0=CE_1=V_{IL} and WE#=V_{IL}.
STS	OPEN DRAIN OUTPUT	STATUS: Indicates the status of the internal WSM (Write State Machine). When configured in level mode (default mode), STS acts as a RY/BY# pin (STS is V_{OL} when the WSM is executing internal erase or program algorithms). When configured in one of its pulse modes, STS can pulse to indicate erase/program completion. Refer to Table 9 for STS configuration.
BYTE#	INPUT	BYTE ENABLE: BYTE# V_{IL} places the device in byte mode (×8). In this mode, DQ_{15}-DQ_8 is floated (High Z) and A_0 is the lowest address input. BYTE# V_{IH} places the device in word mode (×16) and A_1 is the lowest address input.
V_{PEN}	INPUT	MONITORING POWER SUPPLY VOLTAGE: V_{PEN} is not used for power supply pin. With V_{PEN}≤V_{PENLK}, block erase, (page buffer) program, block lock configuration and OTP program cannot be executed and should not be attempted.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY (2.7V-3.6V): With V_{CC}≤V_{LKO}, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (refer to DC Characteristics) produce spurious results and should not be attempted.
V_{CCQ}	SUPPLY	INPUT/OUTPUT POWER SUPPLY (2.7V-3.6V): Power supply for all input/output pins.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internally connected; it may be driven or floated.

Table 2. CE_0, CE_1, BS Truth Table (1), (2)

BS	CE_1	CE_0	Device
V_{IL}	V_{IL}	V_{IL}	Bank 0 Enabled
	V_{IL}	V_{IH}	Disabled
	V_{IH}	V_{IL}	Disabled
	V_{IH}	V_{IH}	Disabled
V_{IH}	V_{IL}	V_{IL}	Bank 1 Enabled
	V_{IL}	V_{IH}	Disabled
	V_{IH}	V_{IL}	Disabled
	V_{IH}	V_{IH}	Disabled

NOTE:
1. For single-chip applications, CE_1 can be connected to GND.
2. BS transitions must not occur when CE_0=CE_1=V_{IL} and WE#=V_{IL}.

Selected by $BS=V_{IL}$ (Bank 0)

$[A_{22}\text{-}A_1]$		$[A_{22}\text{-}A_0]$
3FFFFF	64-Kword/128-Kbyte Block 63	7FFFFF
3F0000 3EFFFF	64-Kword/128-Kbyte Block 62	7E0000 7DFFFF
3E0000 3DFFFF	64-Kword/128-Kbyte Block 61	7C0000 7BFFFF
3D0000 3CFFFF	64-Kword/128-Kbyte Block 60	7A0000 79FFFF
3C0000 3BFFFF	64-Kword/128-Kbyte Block 59	780000 77FFFF
3B0000 3AFFFF	64-Kword/128-Kbyte Block 58	760000 75FFFF
3A0000 39FFFF	64-Kword/128-Kbyte Block 57	740000 73FFFF
390000 38FFFF	64-Kword/128-Kbyte Block 56	720000 71FFFF
380000 37FFFF	64-Kword/128-Kbyte Block 55	700000 6FFFFF
370000 36FFFF	64-Kword/128-Kbyte Block 54	6E0000 6DFFFF
360000 35FFFF	64-Kword/128-Kbyte Block 53	6C0000 6BFFFF
350000 34FFFF	64-Kword/128-Kbyte Block 52	6A0000 69FFFF
340000 33FFFF	64-Kword/128-Kbyte Block 51	680000 67FFFF
330000 32FFFF	64-Kword/128-Kbyte Block 50	660000 65FFFF
320000 31FFFF	64-Kword/128-Kbyte Block 49	640000 63FFFF
310000 30FFFF	64-Kword/128-Kbyte Block 48	620000 61FFFF
300000 2FFFFF	64-Kword/128-Kbyte Block 47	600000 5FFFFF
2F0000 2EFFFF	64-Kword/128-Kbyte Block 46	5E0000 5DFFFF
2E0000 2DFFFF	64-Kword/128-Kbyte Block 45	5C0000 5BFFFF
2D0000 2CFFFF	64-Kword/128-Kbyte Block 44	5A0000 59FFFF
2C0000 2BFFFF	64-Kword/128-Kbyte Block 43	580000 57FFFF
2B0000 2AFFFF	64-Kword/128-Kbyte Block 42	560000 55FFFF
2A0000 29FFFF	64-Kword/128-Kbyte Block 41	540000 53FFFF
290000 28FFFF	64-Kword/128-Kbyte Block 40	520000 51FFFF
280000 27FFFF	64-Kword/128-Kbyte Block 39	500000 4FFFFF
270000 26FFFF	64-Kword/128-Kbyte Block 38	4E0000 4DFFFF
260000 25FFFF	64-Kword/128-Kbyte Block 37	4C0000 4BFFFF
250000 24FFFF	64-Kword/128-Kbyte Block 36	4A0000 49FFFF
240000 23FFFF	64-Kword/128-Kbyte Block 35	480000 47FFFF
230000 22FFFF	64-Kword/128-Kbyte Block 34	460000 45FFFF
220000 21FFFF	64-Kword/128-Kbyte Block 33	440000 43FFFF
210000 20FFFF	64-Kword/128-Kbyte Block 32	420000 41FFFF
200000		400000

$[A_{22}\text{-}A_1]$		$[A_{22}\text{-}A_0]$
1FFFFF	64-Kword/128-Kbyte Block 31	3FFFFF
1F0000 1EFFFF	64-Kword/128-Kbyte Block 30	3E0000 3DFFFF
1E0000 1DFFFF	64-Kword/128-Kbyte Block 29	3C0000 3BFFFF
1D0000 1CFFFF	64-Kword/128-Kbyte Block 28	3A0000 39FFFF
1C0000 1BFFFF	64-Kword/128-Kbyte Block 27	380000 37FFFF
1B0000 1AFFFF	64-Kword/128-Kbyte Block 26	360000 35FFFF
1A0000 19FFFF	64-Kword/128-Kbyte Block 25	340000 33FFFF
190000 18FFFF	64-Kword/128-Kbyte Block 24	320000 31FFFF
180000 17FFFF	64-Kword/128-Kbyte Block 23	300000 2FFFFF
170000 16FFFF	64-Kword/128-Kbyte Block 22	2E0000 2DFFFF
160000 15FFFF	64-Kword/128-Kbyte Block 21	2C0000 2BFFFF
150000 14FFFF	64-Kword/128-Kbyte Block 20	2A0000 29FFFF
140000 13FFFF	64-Kword/128-Kbyte Block 19	280000 27FFFF
130000 12FFFF	64-Kword/128-Kbyte Block 18	260000 25FFFF
120000 11FFFF	64-Kword/128-Kbyte Block 17	240000 23FFFF
110000 10FFFF	64-Kword/128-Kbyte Block 16	220000 21FFFF
100000 0FFFFF	64-Kword/128-Kbyte Block 15	200000 1FFFFF
0F0000 0EFFFF	64-Kword/128-Kbyte Block 14	1E0000 1DFFFF
0E0000 0DFFFF	64-Kword/128-Kbyte Block 13	1C0000 1BFFFF
0D0000 0CFFFF	64-Kword/128-Kbyte Block 12	1A0000 19FFFF
0C0000 0BFFFF	64-Kword/128-Kbyte Block 11	180000 17FFFF
0B0000 0AFFFF	64-Kword/128-Kbyte Block 10	160000 15FFFF
0A0000 09FFFF	64-Kword/128-Kbyte Block 9	140000 13FFFF
090000 08FFFF	64-Kword/128-Kbyte Block 8	120000 11FFFF
080000 07FFFF	64-Kword/128-Kbyte Block 7	100000 0FFFFF
070000 06FFFF	64-Kword/128-Kbyte Block 6	0E0000 0DFFFF
060000 05FFFF	64-Kword/128-Kbyte Block 5	0C0000 0BFFFF
050000 04FFFF	64-Kword/128-Kbyte Block 4	0A0000 09FFFF
040000 03FFFF	64-Kword/128-Kbyte Block 3	080000 07FFFF
030000 02FFFF	64-Kword/128-Kbyte Block 2	060000 05FFFF
020000 01FFFF	64-Kword/128-Kbyte Block 1	040000 03FFFF
010000 00FFFF	64-Kword/128-Kbyte Block 0	020000 01FFFF
000000		000000

Figure 2.1. Memory Map (Memory Area selected by $BS=V_{IL}$)

Selected by $BS=V_{IH}$ (Bank 1)

$[A_{22}\text{-}A_1]$		$[A_{22}\text{-}A_0]$
3FFFFF	64-Kword/128-Kbyte Block 63	7FFFFF
3F0000 3EFFFF	64-Kword/128-Kbyte Block 62	7E0000 7DFFFF
3E0000 3DFFFF	64-Kword/128-Kbyte Block 61	7C0000 7BFFFF
3D0000 3CFFFF	64-Kword/128-Kbyte Block 60	7A0000 79FFFF
3C0000 3BFFFF	64-Kword/128-Kbyte Block 59	780000 77FFFF
3B0000 3AFFFF	64-Kword/128-Kbyte Block 58	760000 75FFFF
3A0000 39FFFF	64-Kword/128-Kbyte Block 57	740000 73FFFF
390000 38FFFF	64-Kword/128-Kbyte Block 56	720000 71FFFF
380000 37FFFF	64-Kword/128-Kbyte Block 55	700000 6FFFFF
370000 36FFFF	64-Kword/128-Kbyte Block 54	6E0000 6DFFFF
360000 35FFFF	64-Kword/128-Kbyte Block 53	6C0000 6BFFFF
350000 34FFFF	64-Kword/128-Kbyte Block 52	6A0000 69FFFF
340000 33FFFF	64-Kword/128-Kbyte Block 51	680000 67FFFF
330000 32FFFF	64-Kword/128-Kbyte Block 50	660000 65FFFF
320000 31FFFF	64-Kword/128-Kbyte Block 49	640000 63FFFF
310000 30FFFF	64-Kword/128-Kbyte Block 48	620000 61FFFF
300000 2FFFFF	64-Kword/128-Kbyte Block 47	600000 5FFFFF
2F0000 2EFFFF	64-Kword/128-Kbyte Block 46	5E0000 5DFFFF
2E0000 2DFFFF	64-Kword/128-Kbyte Block 45	5C0000 5BFFFF
2D0000 2CFFFF	64-Kword/128-Kbyte Block 44	5A0000 59FFFF
2C0000 2BFFFF	64-Kword/128-Kbyte Block 43	580000 57FFFF
2B0000 2AFFFF	64-Kword/128-Kbyte Block 42	560000 55FFFF
2A0000 29FFFF	64-Kword/128-Kbyte Block 41	540000 53FFFF
290000 28FFFF	64-Kword/128-Kbyte Block 40	520000 51FFFF
280000 27FFFF	64-Kword/128-Kbyte Block 39	500000 4FFFFF
270000 26FFFF	64-Kword/128-Kbyte Block 38	4E0000 4DFFFF
260000 25FFFF	64-Kword/128-Kbyte Block 37	4C0000 4BFFFF
250000 24FFFF	64-Kword/128-Kbyte Block 36	4A0000 49FFFF
240000 23FFFF	64-Kword/128-Kbyte Block 35	480000 47FFFF
230000 22FFFF	64-Kword/128-Kbyte Block 34	460000 45FFFF
220000 21FFFF	64-Kword/128-Kbyte Block 33	440000 43FFFF
210000 20FFFF	64-Kword/128-Kbyte Block 32	420000 41FFFF
200000		400000

$[A_{22}\text{-}A_1]$		$[A_{22}\text{-}A_0]$
1FFFFF	64-Kword/128-Kbyte Block 31	3FFFFF
1F0000 1EFFFF	64-Kword/128-Kbyte Block 30	3E0000 3DFFFF
1E0000 1DFFFF	64-Kword/128-Kbyte Block 29	3C0000 3BFFFF
1D0000 1CFFFF	64-Kword/128-Kbyte Block 28	3A0000 39FFFF
1C0000 1BFFFF	64-Kword/128-Kbyte Block 27	380000 37FFFF
1B0000 1AFFFF	64-Kword/128-Kbyte Block 26	360000 35FFFF
1A0000 19FFFF	64-Kword/128-Kbyte Block 25	340000 33FFFF
190000 18FFFF	64-Kword/128-Kbyte Block 24	320000 31FFFF
180000 17FFFF	64-Kword/128-Kbyte Block 23	300000 2FFFFF
170000 16FFFF	64-Kword/128-Kbyte Block 22	2E0000 2DFFFF
160000 15FFFF	64-Kword/128-Kbyte Block 21	2C0000 2BFFFF
150000 14FFFF	64-Kword/128-Kbyte Block 20	2A0000 29FFFF
140000 13FFFF	64-Kword/128-Kbyte Block 19	280000 27FFFF
130000 12FFFF	64-Kword/128-Kbyte Block 18	260000 25FFFF
120000 11FFFF	64-Kword/128-Kbyte Block 17	240000 23FFFF
110000 10FFFF	64-Kword/128-Kbyte Block 16	220000 21FFFF
100000 0FFFFF	64-Kword/128-Kbyte Block 15	200000 1FFFFF
0F0000 0EFFFF	64-Kword/128-Kbyte Block 14	1E0000 1DFFFF
0E0000 0DFFFF	64-Kword/128-Kbyte Block 13	1C0000 1BFFFF
0D0000 0CFFFF	64-Kword/128-Kbyte Block 12	1A0000 19FFFF
0C0000 0BFFFF	64-Kword/128-Kbyte Block 11	180000 17FFFF
0B0000 0AFFFF	64-Kword/128-Kbyte Block 10	160000 15FFFF
0A0000 09FFFF	64-Kword/128-Kbyte Block 9	140000 13FFFF
090000 08FFFF	64-Kword/128-Kbyte Block 8	120000 11FFFF
080000 07FFFF	64-Kword/128-Kbyte Block 7	100000 0FFFFF
070000 06FFFF	64-Kword/128-Kbyte Block 6	0E0000 0DFFFF
060000 05FFFF	64-Kword/128-Kbyte Block 5	0C0000 0BFFFF
050000 04FFFF	64-Kword/128-Kbyte Block 4	0A0000 09FFFF
040000 03FFFF	64-Kword/128-Kbyte Block 3	080000 07FFFF
030000 02FFFF	64-Kword/128-Kbyte Block 2	060000 05FFFF
020000 01FFFF	64-Kword/128-Kbyte Block 1	040000 03FFFF
010000 00FFFF	64-Kword/128-Kbyte Block 0	020000 01FFFF
000000		000000

Figure 2.2. Memory Map (Memory Area selected by $BS=V_{IH}$)

Table 3. Identifier Codes Address

	Code	Address $[A_{22}\text{-}A_1]$ (1)	Data $[DQ_7\text{-}DQ_0]$	Notes
Manufacturer Code	Manufacturer Code	000000H	B0H	2
Device Code	Device Code	000001H	18H	2
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	$DQ_0 = 0$	3
	Block is Locked		$DQ_0 = 1$	3

NOTES:
1. The address A_0 and BS don't care.
2. "00H" is presented on DQ_{15}-DQ_8 in word mode (BYTE#=V_{IH} : ×16 bit).
3. Block Address = The beginning location of a block address. DQ_{15}-DQ_1 are reserved for future implementation.

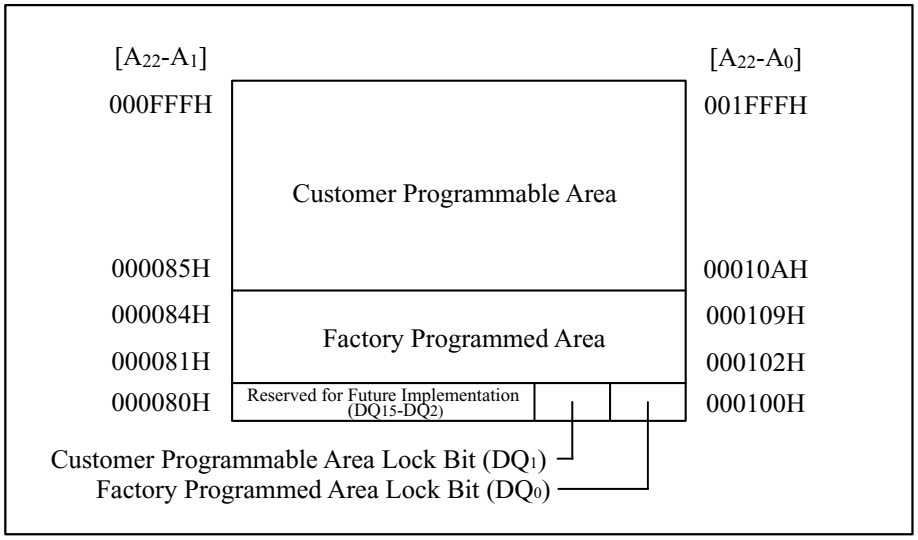


Figure 3. OTP Block Address Map
(The area not specified in the above figure cannot be used.)

NOTE:
1. BS must be V_{IL}, when using OTP block.

Table 4. Bus Operation[1, 2]

Mode	Notes	RP#	$CE_{0,1}$ [3]	OE#	WE#	Address	V_{PEN}	DQ [4]	STS [10]
Read Array	8	V_{IH}	Enabled	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable		V_{IH}	Enabled	V_{IH}	V_{IH}	X	X	High Z	X
Standby		V_{IH}	Disabled	X	X	X	X	High Z	X
Reset	5	V_{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes/OTP	8	V_{IH}	Enabled	V_{IL}	V_{IH}	Refer to Table 3	X	Refer to Table 3	X
Read Query	8,9	V_{IH}	Enabled	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Write	6,7,8	V_{IH}	Enabled	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES:
1. Refer to DC Characteristics. When $V_{PEN} \leq V_{PENLK}$, memory contents can be read, but cannot be altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PENLK} or V_{PENH} for V_{PEN}.
   Refer to DC Characteristics for V_{PENLK} and V_{PENH} voltages.
3. Refer to Table 2 to determine whether the device is selected or de-selected depending on the state of CE_0, CE_1 and BS.
4. DQ refers to DQ_{15}-DQ_0 in word mode (BYTE#=V_{IH} : ×16 bit) and DQ_7-DQ_0 in byte mode (BYTE#=V_{IL} : ×8 bit).
5. RP# at GND±0.2V ensures the lowest power consumption.
6. Command writes involving block erase, (page buffer) program, block lock configuration or OTP program are reliably executed when $V_{PEN}=V_{PENH}$ and V_{CC}=2.7V-3.6V.
7. Refer to Table 5 for valid D_{IN} during a write operation. BS transitions must not occur when $CE_0=CE_1=V_{IL}$ and WE#=V_{IL}.
8. Never hold OE# low and WE# low at the same timing.
9. Query code = Common Flash Interface (CFI) code.
10. STS is V_{OL} when the WSM (Write State Machine) is executing internal block erase, (page buffer) program or OTP program algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with program and page buffer program inactive), (page buffer) program suspend mode, or reset mode.

Table 5. Command Definitions (10)

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array	1		Write	Bnk	FFH			
Read Identifier Codes/OTP	≥ 2	4	Write	Bnk	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	4	Write	Bnk	98H	Read	QA	QD
Read Status Register	2		Write	Bnk	70H	Read	Bnk	SRD
Clear Status Register	1		Write	Bnk	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Program	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5,7	Write	BA	E8H	Write	BA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8	Write	Bnk	B0H			
Block Erase and (Page Buffer) Program Resume	1	8	Write	Bnk	D0H			
STS Configuration	2		Write	Bnk	B8H	Write	Bnk	CC
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bits	2	9	Write	Bnk	60H	Write	Bnk	D0H
OTP Program	2		Write	OA	C0H	Write	OA	OD

NOTES:

1. Bus operations are defined in Table 4. Each command is valid for the bank to which the command is written. BS transitions must not occur when CE_0=CE_1=V_{IL} and WE#=V_{IL}.
2. Bnk=Any valid address within the bank selected by BS.
   IA=Identifier codes address (Refer to Table 3).
   QA=Query codes address.
   BA=Address within the block for block erase, page buffer program or set block lock bit.
   WA=Address of memory location for the Program command.
   OA=Address of OTP block to be read or programmed (Refer to Figure 3).
3. The upper byte of the data bus (DQ_{15}-DQ_8) during command writes is ignored in word mode (BYTE#=V_{IH} : ×16 bit).
   ID=Data to be read from identifier codes. (Refer to Table 3).
   QD=Data to be read from query database.
   SRD=Data to be read from status register. Refer to Table 7 and Table 8 for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the first edge of CE_0 or CE_1 that disables the device or the rising edge of WE# (whichever occurs first) during command write cycles.
   N-1=N is the number of the words /bytes to be loaded into a page buffer.
   OD=Data within OTP block. Data is latched on the first edge of CE_0 or CE_1 that disables the device or the rising edge of WE# (whichever occurs first) during command write cycles.
   CC= STS configuration code (Refer to Table 9). STS configuration must be set for every bank.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code and the data within OTP block (Refer to Table 3).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RP# is V_{IH}.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, write the program sequential address and data of "N" times. Finally, write the any valid address within the block to be programmed and the confirm command (D0H).

8. If both block erase operation and (page buffer) program operation are suspended, the suspended (page buffer) program operation is resumed when writing the Block Erase and (Page Buffer) Program Resume (D0H) command.
9. Following the Clear Block Lock Bits command, all the blocks within the bank to which the command is written are unlocked at a time.
10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 6. Functions of Block Lock [1], [2]

DQ_0 [3]	State Name	Erase/Program Allowed [4]
0	Unlocked	Yes
1	Locked	No

NOTES:
1. Selected block is locked by the Set Block Lock Bit command. Following the Clear Block Lock Bits command, all the blocks within the bank to which the command is written are unlocked at a time.
2. Locked and unlocked states remain unchanged even after power-up/down and device reset.
3. After writing the Read Identifier Codes/OTP command, read operation outputs the block lock bit status on DQ_0 (refer to Table 3).
4. Erase and program are general terms, respectively, to express: block erase and (page buffer) program operations.

Table 7. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BECBLS	PBPOPSBLS	VPENS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)	
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check SR.7 or STS to determine block erase, (page buffer) program, block lock configuration or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0".
SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = BLOCK ERASE AND CLEAR BLOCK LOCK BITS STATUS (BECBLS) 1 = Error in Block Erase or Clear Block Lock Bits 0 = Successful Block Erase or Clear Block Lock Bits	If both SR.5 and SR.4 are "1"s after a block erase, page buffer program, block lock configuration, STS configuration attempt, an improper command sequence was entered.
SR.4 = (PAGE BUFFER) PROGRAM, OTP PROGRAM AND SET BLOCK LOCK BIT STATUS (PBPOPSBLS) 1 = Error in (Page Buffer) Program, OTP Program or Set Block Lock Bit 0 = Successful (Page Buffer) Program, OTP Program or Set Block Lock Bit	
SR.3 = V_{PEN} STATUS (VPENS) 1 = V_{PEN} LOW Detect, Operation Abort 0 = V_{PEN} OK	SR.3 does not provide a continuous indication of V_{PEN} level. The WSM interrogates and indicates the V_{PEN} level only after Block Erase, (Page Buffer) Program, Set Block Lock Bit, Clear Block Lock Bits or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PEN} \neq V_{PENH}$ or V_{PENLK}.
SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS) 1 = (Page Buffer) Program Suspended 0 = (Page Buffer) Program in Progress/Completed	SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/ OTP command indicates block lock bit status.
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Erase or Program Attempted on a Locked Block, Operation Abort 0 = Unlocked	
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

Table 8. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

XSR.7 = STATE MACHINE STATUS (SMS)
1 = Page Buffer Program available
0 = Page Buffer Program not available

XSR.6-0 =RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.

XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

Table 9. STS Configuration Definition (1), (2)

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
R	R	R	R	R	R	CC	CC
7	6	5	4	3	2	1	0

DQ_{15}-DQ_2 = RESERVED FOR FUTURE ENHANCEMENTS (R)

DQ_1-DQ_0 = STS CONFIGURATION CODE (CC)
- 00 = level mode: RY/BY# indication. (Default)
- 01 = pulse mode on erase complete.
- 10 = pulse mode on program complete.
- 11 = pulse mode on erase or program complete.

In STS configuration = "00", STS is V_{OL} when the WSM is executing internal erase or program algorithms.

STS configuration codes "01", "10" and "11" are all pulse modes such that the STS pin pulses low then high when the operation indicated by the configuration code is completed.

NOTES:

After power-up or device reset, STS configuration is set to "00".

STS configuration 00
The output of the STS pin is the control signal to prevent accessing a flash memory while the internal WSM is busy (SR.7="0").

STS configuration 01
The output of the STS pin is the control signal to indicate that the erase operation is completed and the flash memory is available for the next operation.

STS configuration 10
The output of the STS pin is the control signal to indicate that the program operation is completed and the flash memory is available for the next operation.

STS configuration 11
The output of the STS pin is the control signal to indicate that the erase or program operation is completed and the flash memory is available for the next operation.

NOTE:
1. When the device is configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250ns.
2. STS configuration must be set for every bank.

1 Electrical Specifications

1.1 Absolute Maximum Ratings*

Operating Temperature

During Read, Erase and Program ...-40°C to +85°C (1)

Storage Temperature

During under Bias..... -40°C to +85°C

During non Bias..... -65°C to +125°C

Voltage On Any Pin (except V_{CC}, V_{CCQ} and V_{PEN})

.....-0.5V to V_{CCQ}+0.5V (2)

V_{CC} and V_{CCQ} Supply Voltage ..... -0.2V to +3.9V (2)

V_{PEN} Supply Voltage..... -0.2V to +3.9V (2)

Output Short Circuit Current.....100mA (3)

**WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:

1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC}, V_{CCQ} and V_{PEN} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

1.2 Operating Conditions

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
T_A	Operating Temperature		-40	+25	+85	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage	1, 2	2.7	3.0	3.6	V	
V_{CCQ}	I/O Supply Voltage	1, 2	2.7	3.0	3.6	V	
V_{PENH}	V_{PEN} Voltage	1	2.7	3.0	3.6	V	
	Block Erase Cycling: V_{PEN}=V_{PENH}		100,000			Cycles	

NOTES:

1. Refer to DC Characteristics tables for voltage range-specific specification.
2. V_{CC} and V_{CCQ} should be the same voltage.

1.2.1 Capacitance (1) (T_A=+25°C, f=1MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
C_{IN}	Input Capacitance		12	16	pF	V_{IN}=0.0V
C_{OUT}	Output Capacitance		16	24	pF	V_{OUT}=0.0V

NOTE:
1. Sampled, not 100% tested.

1.2.2 AC Input/Output Test Conditions

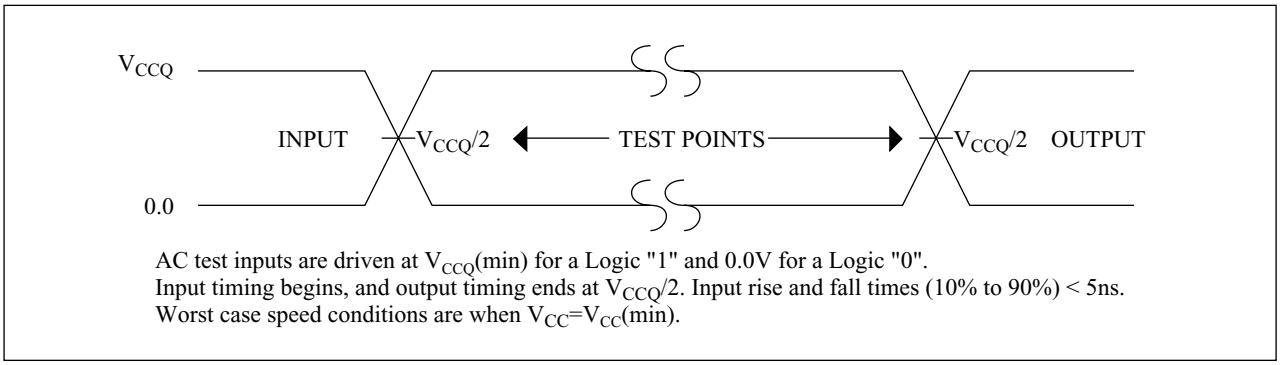


Figure 4. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V

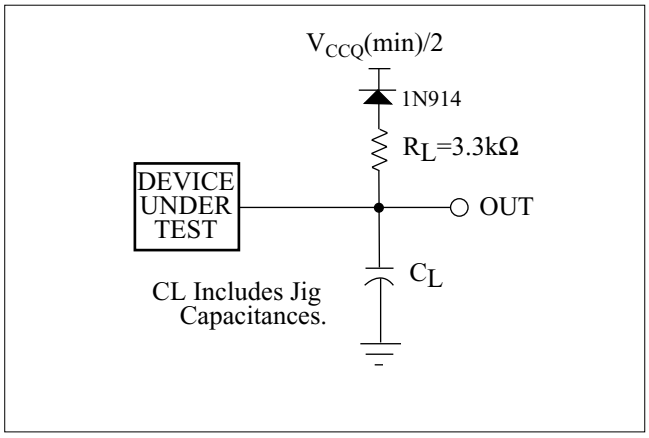


Figure 5. Transient Equivalent Testing Load Circuit

Table 10. Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC}=2.7V-3.6V	30

1.2.3 DC Characteristics

V_{CC}=2.7V-3.6V

Symbol	Parameter		Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	-2		+2	µA	V_{CC}=V_{CC}Max., V_{CCQ}=V_{CCQ}Max., V_{IN}/V_{OUT}=V_{CCQ} or GND
I_{LO}	Output Leakage Current		1	-10		+10	µA	
I_{CCS}	V_{CC} Standby Current		1, 2, 8		50	120	µA	CMOS Inputs, V_{CC}=V_{CC}Max., V_{CCQ}=V_{CCQ}Max., Device is disabled (refer to Table 2), RP#=V_{CCQ}±0.2V
					0.71	2	mA	TTL Inputs, V_{CC}=V_{CC}Max., V_{CCQ}=V_{CCQ}Max., Device is disabled (refer to Table 2), RP#=V_{IH}
I_{CCAS}	V_{CC} Automatic Power Savings Current		1, 2, 5		50	120	µA	CMOS Inputs, V_{CC}=V_{CC}Max., V_{CCQ}=V_{CCQ}Max., Device is enabled (refer to Table 2)
I_{CCD}	V_{CC} Reset Power-Down Current		1		50	120	µA	RP#=GND±0.2V I_{OUT} (STS)=0mA
I_{CCR}	Average V_{CC} Page Mode Read Current	4 word/ 8 byte read	1, 2		15	20	mA	CMOS Inputs, V_{CC}=V_{CC}Max., V_{CCQ}=V_{CCQ}Max., Device is enabled (refer to Table 2), f=5MHz, I_{OUT}=0mA
			1, 2		24	29	mA	CMOS Inputs, V_{CC}=V_{CC}Max., V_{CCQ}=V_{CCQ}Max., Device is enabled (refer to Table 2), f=33MHz, I_{OUT}=0mA
	Average V_{CC} Read Current	1 word/ 1 byte read	1, 2		40	50	mA	CMOS Inputs, V_{CC}=V_{CC}Max., V_{CCQ}=V_{CCQ}Max., Device is enabled (refer to Table 2), f=5MHz, I_{OUT}=0mA
I_{CCW}	V_{CC} (Page Buffer) Program, Set Block Lock Bit Current		1, 2, 6		35	60	mA	CMOS Inputs, V_{PEN}=V_{PENH}
			1, 2, 6		40	70	mA	TTL Inputs, V_{PEN}=V_{PENH}

DC Characteristics (Continued)

V_{CC}=2.7V-3.6V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{CCE}	V_{CC} Block Erase, Clear Block Lock Bits Current	1, 2, 6		35	70	mA	CMOS Inputs, $V_{PEN}=V_{PENH}$
		1, 2, 6		40	80	mA	TTL Inputs, $V_{PEN}=V_{PENH}$
I_{CCWS} I_{CCES}	V_{CC} (Page Buffer) Program or Block Erase Suspend Current	1, 3			10	mA	Device is disabled (refer to Table 2).
V_{IL}	Input Low Voltage	6	-0.5		0.8	V	
V_{IH}	Input High Voltage	6	2.0		V_{CCQ} + 0.5	V	
V_{OL}	Output Low Voltage	6, 8			0.4	V	$V_{CC}=V_{CC}$Min., $V_{CCQ}=V_{CCQ}$Min., I_{OL}=2mA
					0.2	V	$V_{CC}=V_{CC}$Min., $V_{CCQ}=V_{CCQ}$Min., I_{OL}=100µA
V_{OH}	Output High Voltage	6, 8	0.85× V_{CCQ}			V	$V_{CC}=V_{CC}$Min., $V_{CCQ}=V_{CCQ}$Min., I_{OH}=-1.5mA
			V_{CCQ} -0.2			V	$V_{CC}=V_{CC}$Min., $V_{CCQ}=V_{CCQ}$Min., I_{OH}=-100µA
V_{PENLK}	V_{PEN} Lockout Voltage during Normal Operations	4, 6, 7			1.0	V	
V_{PENH}	V_{PEN} Voltage during Block Erase, (Page Buffer) Program, Set Block Lock Bit, Clear Block Lock Bits or OTP Program Operations	4, 7	2.7	3.0	3.6	V	
V_{LKO}	V_{CC} Lockout Voltage	4	2.0			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC}=3.0V, V_{CCQ}=3.0V and T_A=+25°C unless V_{CC} is specified.
2. CMOS inputs are either V_{CCQ}±0.2V or GND±0.2V. TTL inputs are either V_{IL} or V_{IH}.
3. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW}. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR}.
4. Block erase, (page buffer) program, block lock configuration and OTP program operations are inhibited when $V_{PEN}\leq V_{PENLK}$ or $V_{CC}\leq V_{LKO}$. These operations are not guaranteed outside the specified voltage (V_{CC}=2.7V-3.6V and V_{PEN}=2.7V-3.6V).
5. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
6. Sampled, not 100% tested.
7. V_{PEN} is not used for power supply pin. With $V_{PEN}\leq V_{PENLK}$, block erase, (page buffer) program, block lock configuration and OTP program operations are inhibited.
8. Includes STS.

1.2.4 AC Characteristics - Read-Only Operations (1)

T_A=-40°C to +85°C

		V_{CC}	3.0V-3.6V		2.7V-3.6V		
		V_{CCQ}	3.0V-3.6V		2.7V-3.6V		
Symbol	Parameter	Notes	Min.	Max.	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		120		120		ns
t_{AVQV}	Address to Output Delay			120		120	ns
t_{ELQV}	CE_X to Output Delay	3, 4		120		120	ns
t_{APA}	Page Address Access Time			25		30	ns
t_{GLQV}	OE# to Output Delay	3		25		30	ns
t_{PHQV}	RP# High to Output Delay			180		180	ns
t_{ELQX}	CE_X to Output in Low Z	2, 4	0		0		ns
t_{GLQX}	OE# to Output in Low Z	2	0		0		ns
t_{EHQZ}	CE_X to Output in High Z	2, 5		35		35	ns
t_{GHQZ}	OE# to Output in High Z	2		15		15	ns
t_{OH}	Output Hold from First Occurring Address, CE_X or OE# change	2, 5	0		0		ns
t_{ELFL}/t_{ELFH}	CEx Setup to BYTE# Going Low or High	2, 4		10		10	ns
t_{FLQV}/t_{FHQV}	BYTE# to Output Delay			1000		1000	ns
t_{FLQZ}/t_{FHQZ}	BYTE# to Output in High Z	2		1000		1000	ns

NOTES:
1. Refer to AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the first edge of CE_0, CE_1 or BS that enables the device (refer to Table 2) without impact to t_{ELQV}.
4. The timing is defined from the first edge of CE_0, CE_1 or BS that enables the device.
5. The timing is defined from the first edge of CE_0, CE_1 or BS that disables the device.

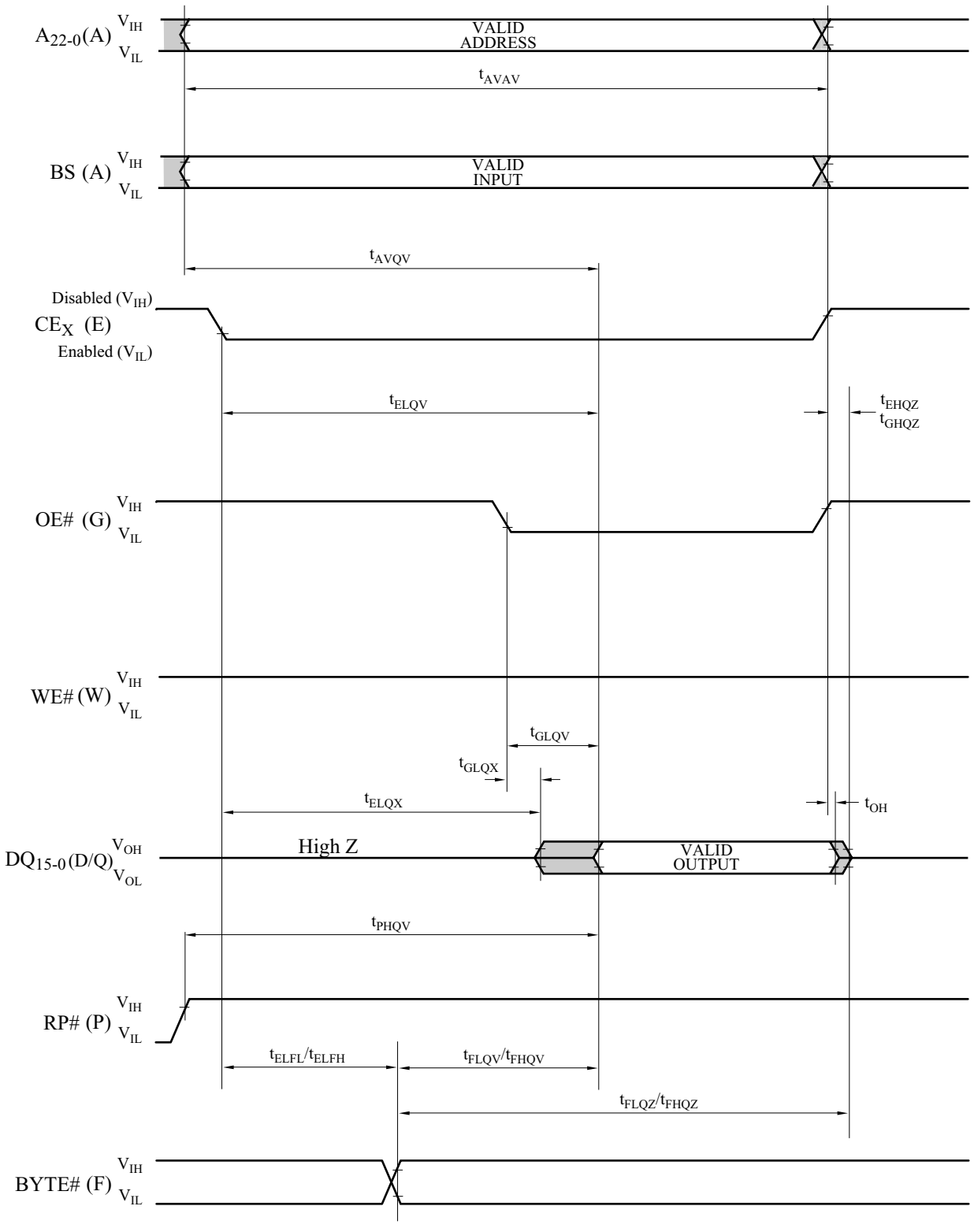


Figure 6. AC Waveform for 1-Word/ 1-Byte Read Operations
(Status Register, Identifier Codes, OTP Block or Query Code)

NOTE:

1. Status register, identifier codes, OTP block and query code can only be read in 1 word/ 1 byte read operations.

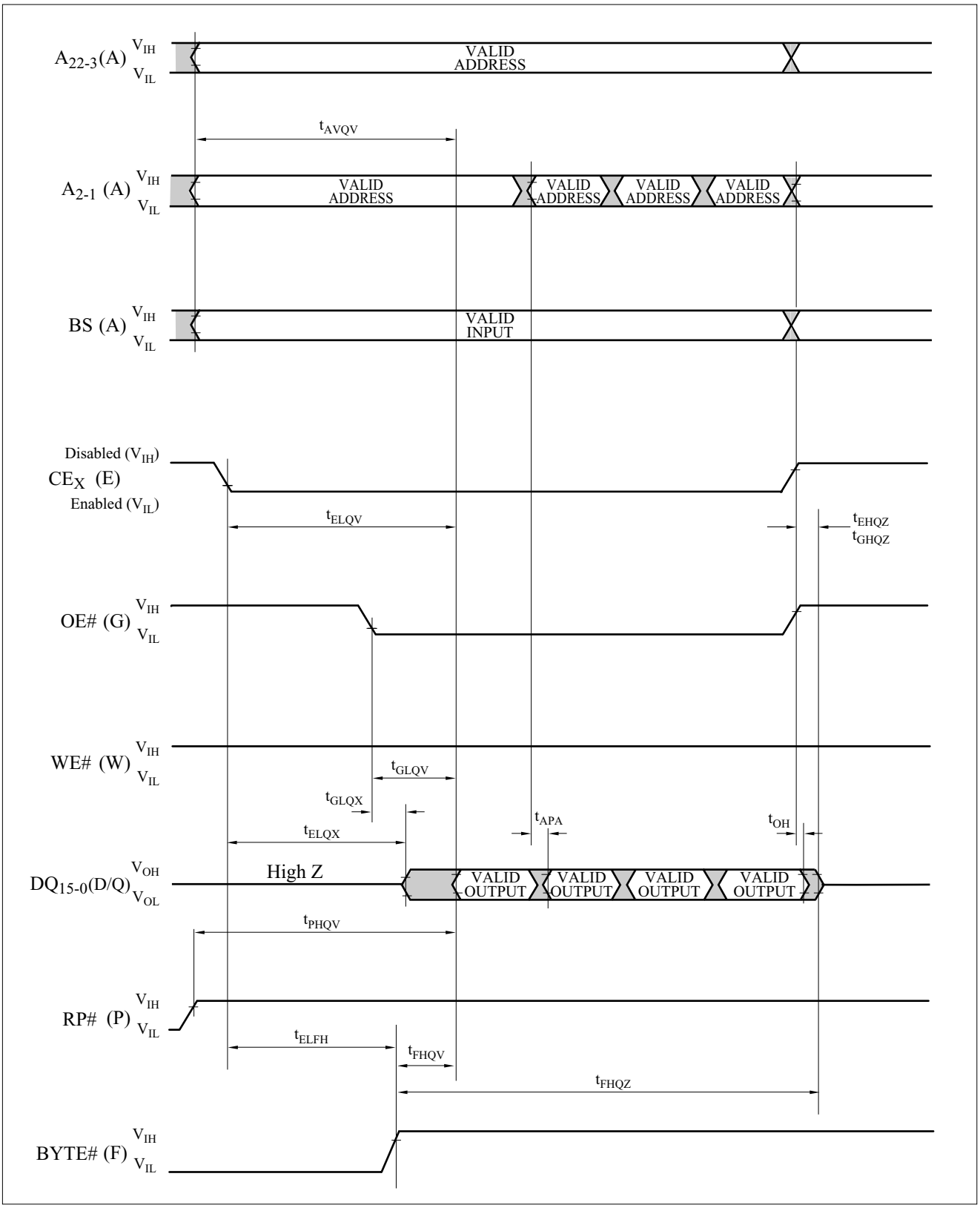


Figure 7. AC Waveform for 4-Word Page Mode Read Operations
(Memory Array)

NOTE:
1. Memory array supports page mode read operations.

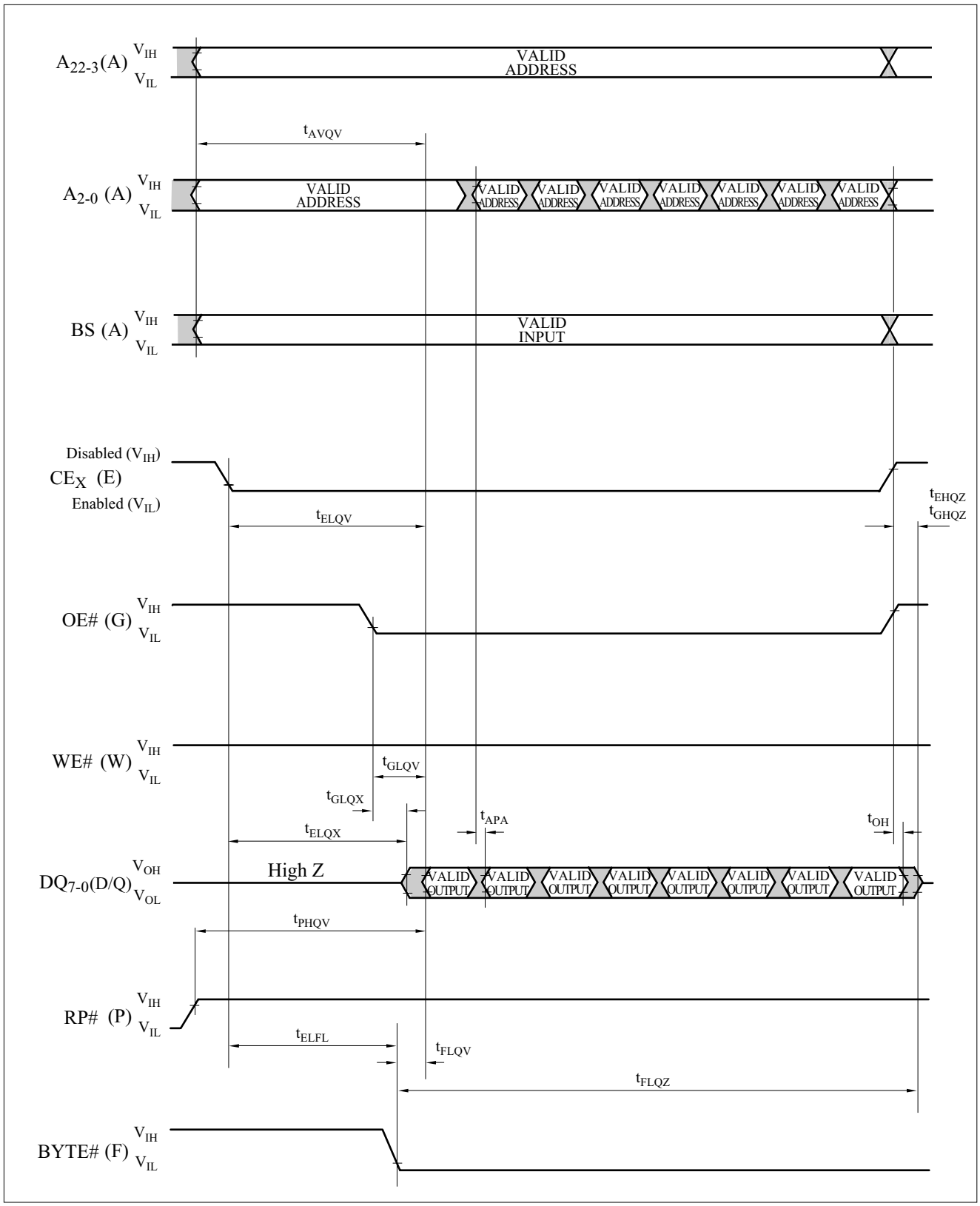


Figure 8. AC Waveform for 8-Byte Page Mode Read Operations (Memory Array)

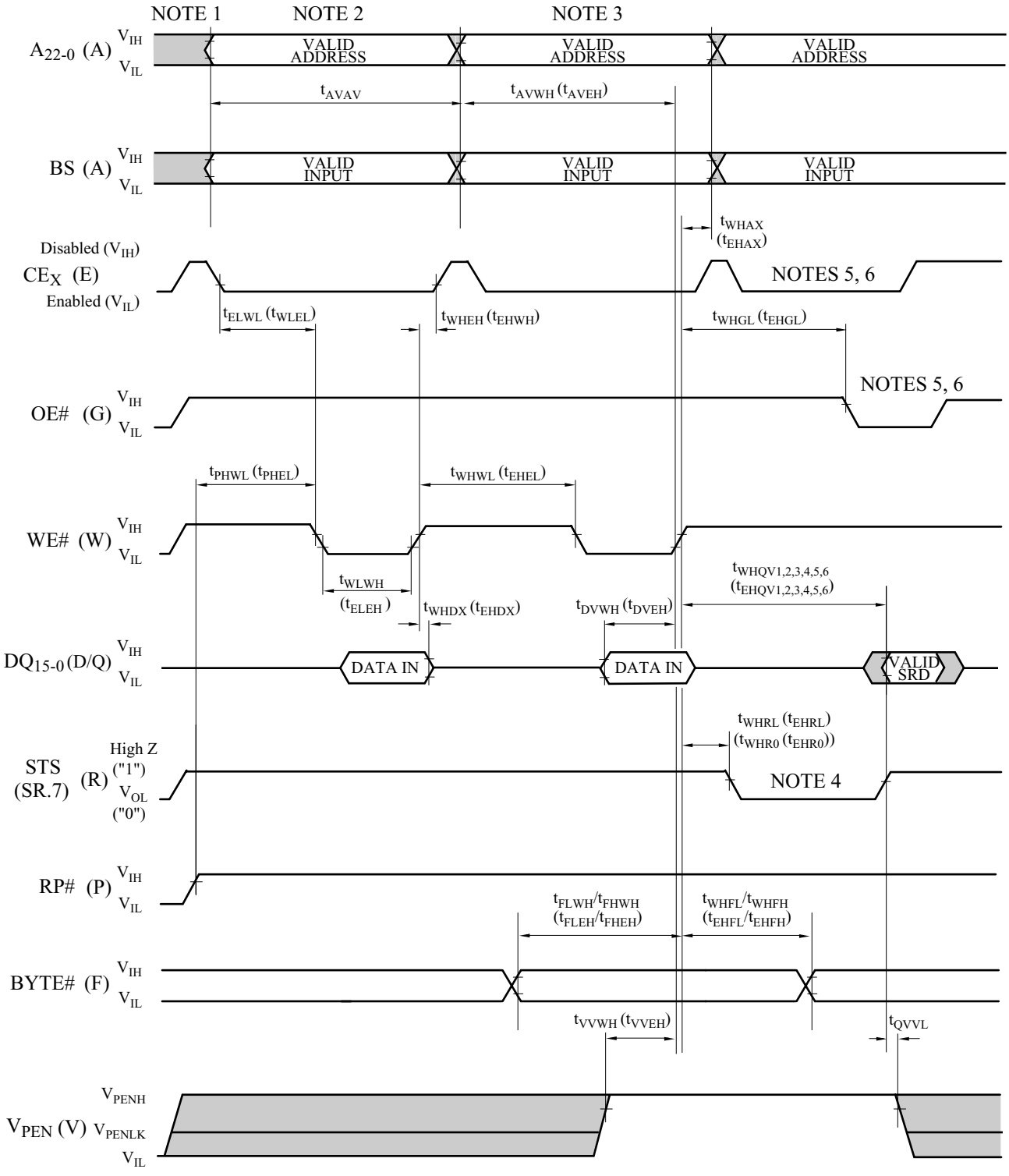
NOTE:
1. Memory array supports page mode read operations.

1.2.5 AC Characteristics - Write Operations [1], [2]

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		120		ns
t_{PHWL} (t_{PHEL})	RP# High Recovery to WE# (CE_X) Going Low	3, 9	1		µs
t_{ELWL} (t_{WLEL})	CE_X (WE#) Setup to WE# (CE_X) Going Low	9	0		ns
t_{WLWH} (t_{ELEH})	WE# (CE_X) Pulse Width Low	4, 9, 10	70		ns
t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE_X) Going High	7, 10	50		ns
t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE_X) Going High	7, 10	55		ns
t_{WHEH} (t_{EHWH})	CE_X (WE#) Hold from WE# (CE_X) High	10	0		ns
t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE_X) High	10	0		ns
t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE_X) High	10	0		ns
t_{WHWL} (t_{EHEL})	WE# (CE_X) Pulse Width High	5, 9, 10	30		ns
t_{VVWH} (t_{VVEH})	V_{PEN} Setup to WE# (CE_X) Going High	3, 10	0		ns
t_{WHGL} (t_{EHGL})	Write Recovery before Read	8	35		ns
t_{WHR0} (t_{EHR0}) t_{WHRL} (t_{EHRL})	WE# (CE_X) High to SR.7 Going "0", STS Going Low	10, 11		500	ns
t_{QVVL}	V_{PEN} Hold from Valid SRD, STS High Z	3, 6, 11	0		ns
t_{FLWH}/t_{FHWH} (t_{FLEH}/t_{FHEH})	BYTE# Setup to WE# (CE_X) Going High	10	50		ns
t_{WHFL}/t_{WHFH} (t_{EHFL}/t_{EHFH})	BYTE# Hold from WE# (CE_X) High	10	90		ns

NOTES:
1. The timing characteristics for reading the status register during block erase, (page buffer) program, block lock configuration and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either CE_0, CE_1 or WE#.
   BS transitions must not occur when CE_0=CE_1=V_{IL} and WE#=V_{IL}.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WP}) is defined from the first edge of CE_0 or CE_1 that enables the device or the falling edge of WE# (whichever occurs last) to the first edge of CE_0 or CE_1 that disables the device or the rising edge of WE# (whichever occurs first). Hence, t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}.
5. Write pulse width high (t_{WPH}) is defined from the first edge of CE_0 or CE_1 that disables the device or the rising edge of WE# (whichever occurs first) to the first edge of CE_0 or CE_1 that enables the device or the falling edge of WE# (whichever occurs last). Hence, t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}.
6. V_{PEN} should be held at V_{PEN}=V_{PENH} until determination of block erase, (page buffer) program, block lock configuration or OTP program success (SR.1/3/4/5=0).
7. Refer to Table 5 for valid address and data for block erase, (page buffer) program, block lock configuration and OTP program.
8. The output delay time t_{AVQV} or t_{ELQV} is required in addition to t_{WHGL} (t_{EHGL}) for read operations after command writes.
9. The timing is defined from the first edge of CE_0 or CE_1 that enables the device.
10. The timing is defined from the first edge of CE_0 or CE_1 that disables the device.
11. STS timings depend on STS configuration.



NOTES:
1. V_{CC} power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay. This waveform illustrates the case when STS is in level mode (RY/BY#).
5. Read status register data.
6. For read operation, OE# and CE_X must be driven active, and WE# de-asserted.

Figure 9. AC Waveform for Write Operations

1.2.6 Reset Operations

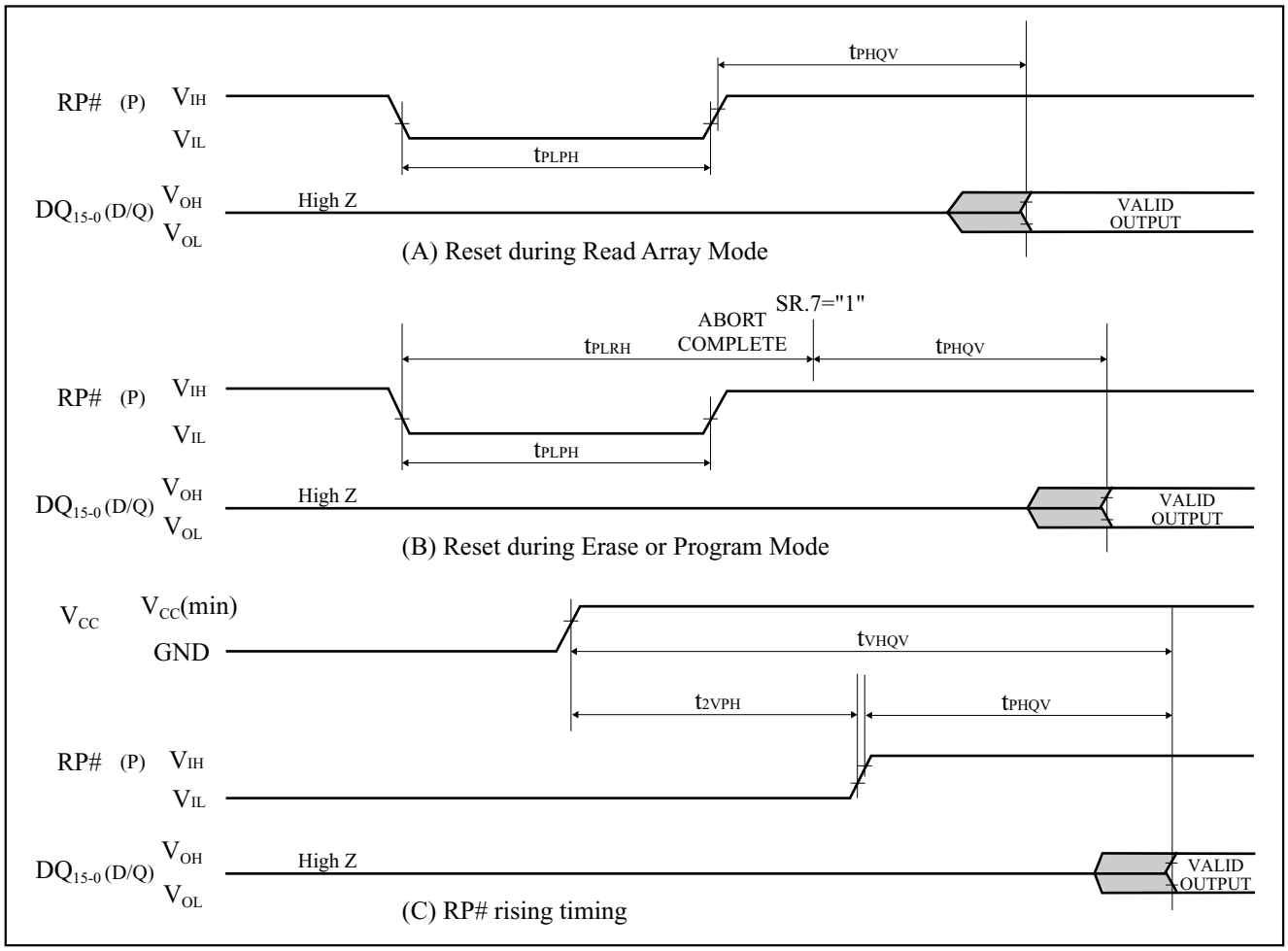


Figure 10. AC Waveform for Reset Operations

Reset AC Specifications (V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	RP# Low to Reset during Read (RP# must be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	RP# Low to Reset during Erase or Program	1, 3, 4		30	µs
t_{2VPH}	V_{CC} 2.7V to RP# High	1, 3, 5	100		ns
t_{VHQV}	V_{CC} 2.7V to Output Delay	3		1	ms

NOTES:
1. A reset time, t_{PHQV}, is required from the later of SR.7 (STS) going "1" (High Z) or RP# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.
2. The device may reset if t_{PLPH} is <100ns, but this is not guaranteed.
3. Sampled, not 100% tested.
4. If RP# asserted while a block erase, (page buffer) program, block lock configuration or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding RP# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

1.2.7 Block Erase, (Page Buffer) Program and Block Lock Configuration Performance(3)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

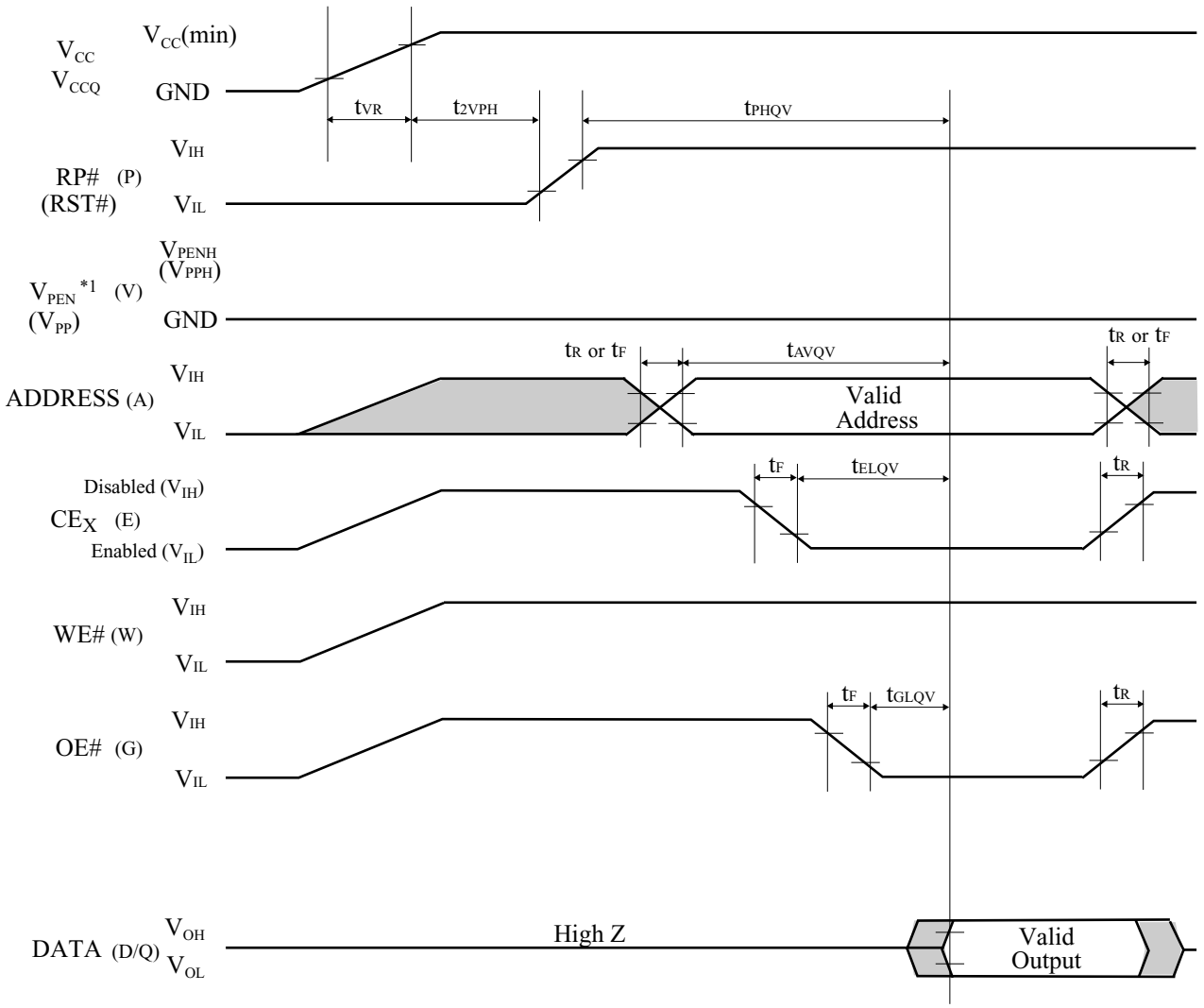
Symbol	Parameter	Notes	$V_{PEN}=V_{PENH}$			Unit
			Min.	Typ.(1)	Max.	
	Page Buffer Program Time (Time to Program 16 words/ 32 bytes)	2, 6, 7		400	1200	µs
t_{WHQV3}/ t_{EHQV3}	Program Time	2		210	630	µs
	Block Program Time (Using Page Buffer Program Command)	2		1.6	4.8	s
t_{WHQV4}/ t_{EHQV4}	Block Erase Time	2		1	5	s
t_{WHQV5}/ t_{EHQV5}	Set Block Lock Bit Time	2		64	85	µs
t_{WHQV6}/ t_{EHQV6}	Clear Block Lock Bits Time	2		0.5	0.7	s
t_{WHRH1}/ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4		25	90	µs
t_{WHRH2}/ t_{EHRH2}	Block Erase Suspend Latency Time to Read	4		26	40	µs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	600			µs

NOTES:
1. Typical values measured at V_{CC}=3.0V, V_{PEN}=3.0V and T_A=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (the first edge of CE_0 or CE_1 that disables the device or the rising edge of WE#) until SR.7 going "1" or STS going High Z.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.
6. These values are valid when the page buffer is full, and the start address is aligned on a 16-word/ 32-byte boundary.
7. Program time per byte (t_{WHQV1}/ t_{EHQV1}) is 12.5µs/byte (typical).
   Program time per word (t_{WHQV2}/ t_{EHQV2}) is 25.0µs/word (typical).

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 To prevent the unwanted writes, system designers should consider the design, which applies V_{PEN} (V_{PP}) to 0V during read operations and V_{PENH} (V_{PPH}) during write or erase operations.
See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		1	µs/V
t_F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

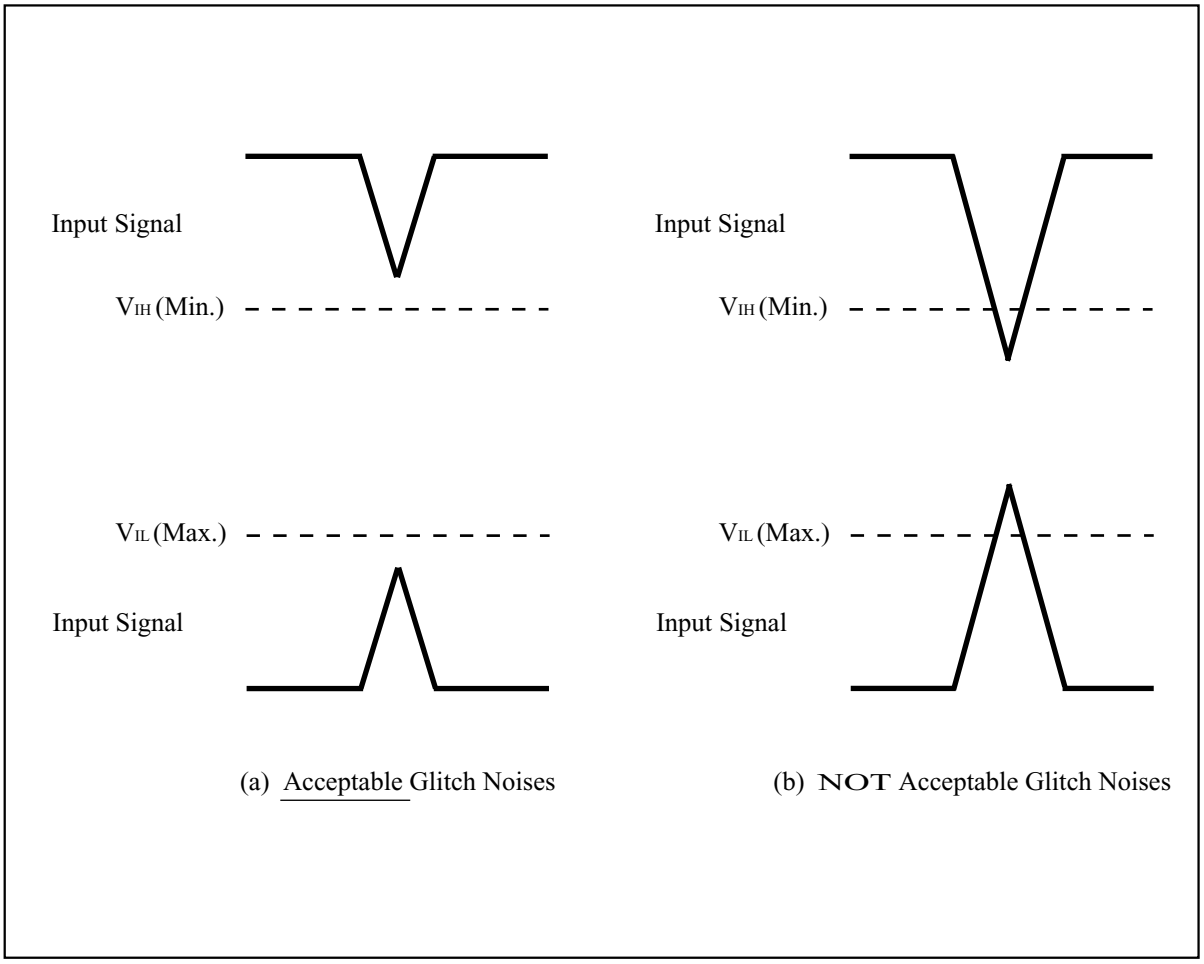


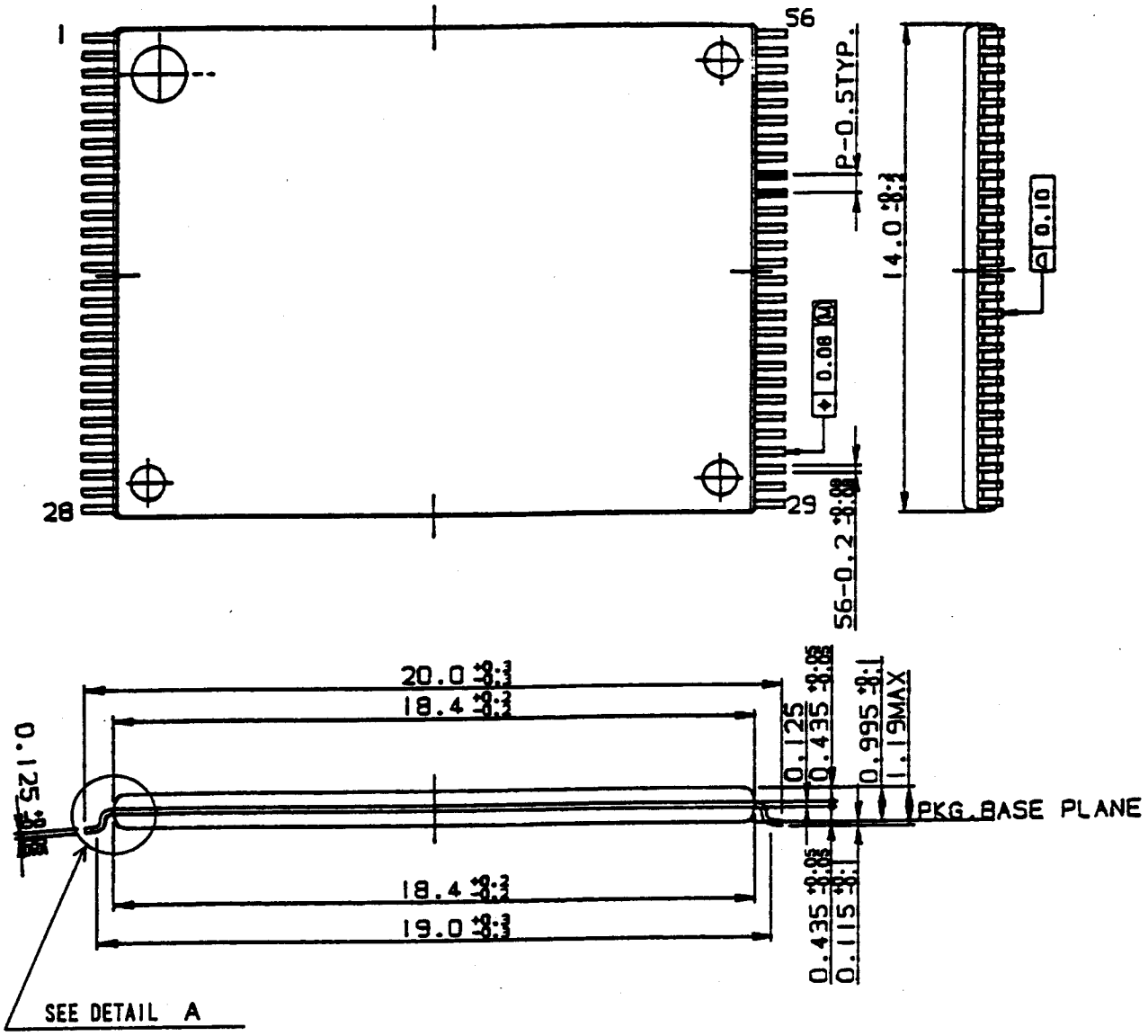
Figure A-2. Waveform for Glitch Noises

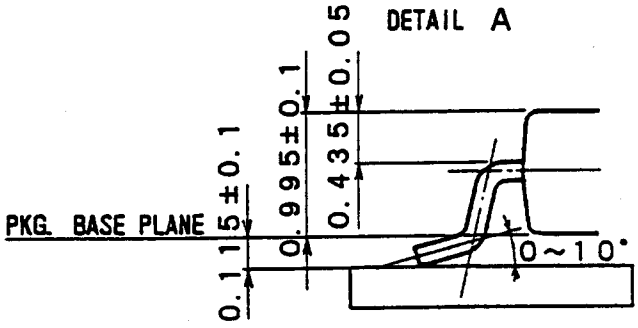
See the “DC CHARACTERISTICS“ described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION(1)

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:
1. International customers should contact their local SHARP or distribution sales office.





名称 NAME	TSOP56-P-1420	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。 NOTE Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1115	単位 UNIT	mm	

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