National Semiconductor

LH0053/LH0053C High Speed Sample and Hold Amplifier

General Description

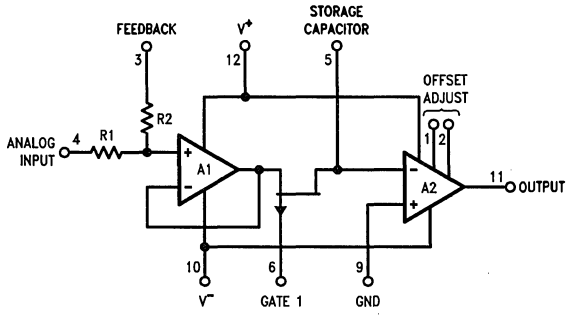
The LH0053/LH0053C is a high speed sample and hold circuit capable of acquiring a 20V step signal in under 5.0 μs.

The device is ideally suited for a variety of high speed data acquisition applications including analog buffer memories for A to D conversion and synchronous demodulation.

Features

- Sample acquisition time 10 μs max. for 20V signal
- FET switch for preset or reset function
- Sample accuracy null
- Offset adjust to 0V
- DTL/TTL compatible FET gate
- Single storage capacitor

Schematic and Connection Diagrams



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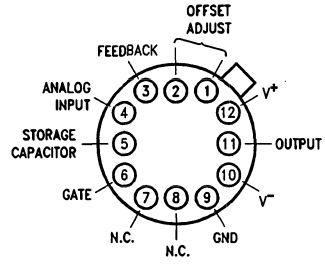
Metal Can Package



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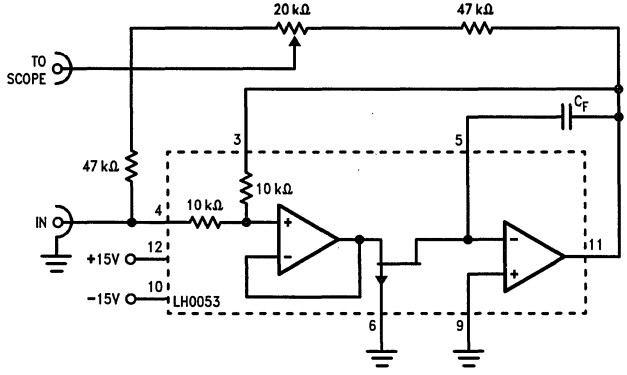
Top View

Order Number LH0053G or LH0053CG
See NS Package Number G12B

AC Test Circuit

Acquisition Time Test Circuit



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V^+ and V^-)	±18V
Gate Input Voltage (V_6)	±20V
Analog Input Voltage (V_4)	±15V
Input Current (I_8 and I_5)	±10 mA
Power Dissipation	See graph
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH0053	−55°C to +125°C
LH0053C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (Note 1)

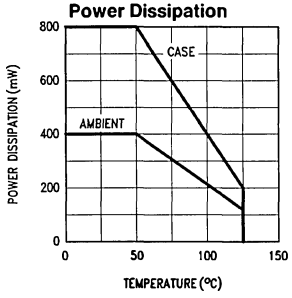
Parameter	Conditions	Limits						Units
		LH0053			LH0053C			
		Min	Typ	Max	Min	Typ	Max	
Sample (Gate "0") Input Voltage				0.5			0.5	V
Sample (Gate "0") Input Current	V_6 = 0.5V, T_A = 25°C V_6 = 0.5V			−5.0 −100			−5.0 −100	μA μA
Hold (Gate "1") Input Voltage		4.5			4.5			V
Hold (Gate "1") Input Current	V_6 = 4.5V, T_A = 25°C V_6 = 4.5V			1.0 1.0				nA μA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	V_4 = 0V, V_6 = 0.5V		13	18		13	18	mA
Input Bias Current (I_4)	V_4 = 0V, T_A = 25°C		120	250		150	500	nA
Input Resistance		5.0	10	15	5.0	10	15	kΩ
Analog Output Voltage Range	R_L = 2.0 kΩ	±10	±12		±10	±12		V
Output Offset Voltage	V_4 = 0V, V_6 = 0.5V, T_A = 25°C V_4 = 0V, V_6 = 0.5V		5.0	7.0 10		5.0	10 15	mV mV
Sample Accuracy (Note 2)	V_4 = ±10V, V_6 = 0.5V, T_A = 25°C		0.1	0.2		0.1	0.3	%
Aperture Time	ΔV_6 = 4.5V, T_A = 25°C		10	25		10	25	ns
Sample Acquisition Time	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF, V_6 = 0V		5.0	10		8.0	15	μs
Sample Acquisition Time	V_4 = ±10V, T_A = 25°C, C_F = 100 pF, V_6 = 0V		4.0			4.0		μs
Output Slew Rate	ΔV_{IN} = ±10V, T_A = 25°C, C_F = 100 pF, V_6 = 0V		20			20		V/μs
Large Signal Bandwidth	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF		200			200		kHz
Large Current (Pin 5)	V_4 = ±10V, T_A = 25°C, V_4 = ±10V		6.0	50 30		10	100 30	pA nA
Drift Rate	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF		6.0	50		10	100	mV/s
Drift Rate	V_4 = ±10V, C_F = 1000 pF			30			30	V/s

Note 1: Unless otherwise noted, these specifications apply for V_S = ±15V, pin 9 grounded, a 1000 pF capacitor between pin 5 and pin 11, pin 3 shorted to pin 11, over the temperature range −55°C to +125°C for the LH0053 and −25°C to +85°C for the LH0053C. All typical values are for T_A = 25°C.

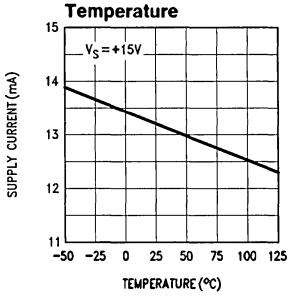
Note 2: Sample accuracy may be nulled by inserting a potentiometer in the feedback loop. This compensates for source impedance and feedback resistor tolerances.

Typical Performance Characteristics

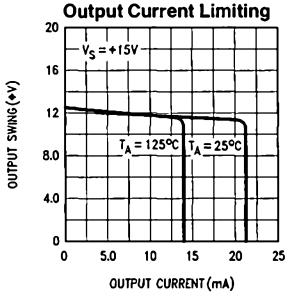
Power Dissipation



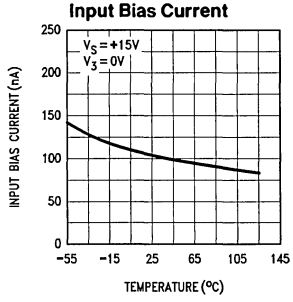
Supply Current vs Temperature



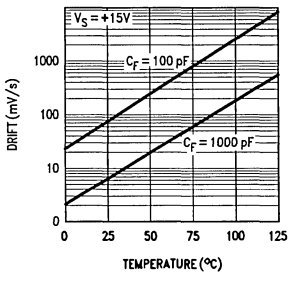
Output Current Limiting



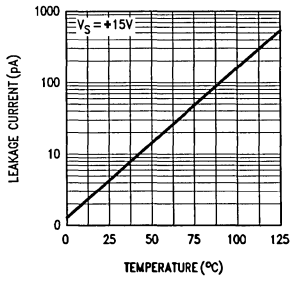
Input Bias Current



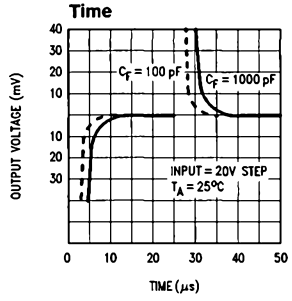
Drift



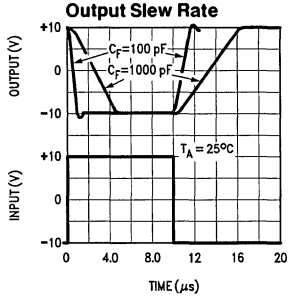
Leakage Current at Pin 5



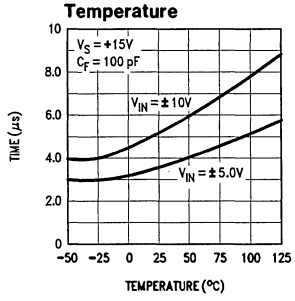
Sample Acquisition Time



Output Slew Rate



Acquisition Time vs Temperature



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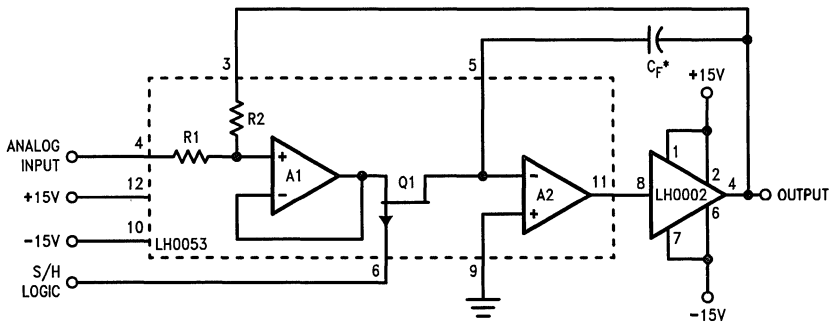
Typical Applications

Increasing Output Drive Capability



*Polystyrene construction.

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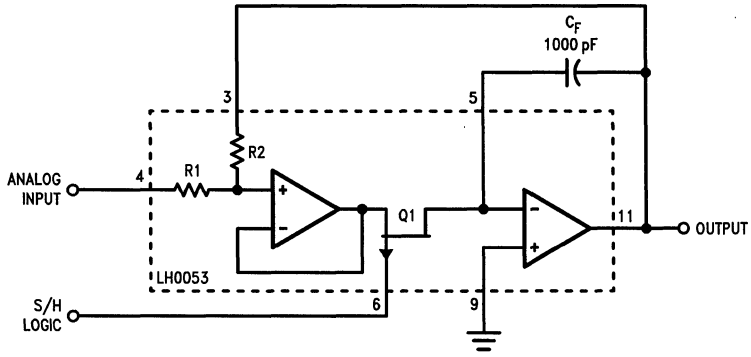
Typical Applications (Continued)

Sample and Hold



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Applications Information

SOURCE IMPEDANCE COMPENSATION

The gain accuracy (linearity) of the LH0053/LH0053C is set by two internal precision resistors. Circuit applications in which the source impedance is non-zero will result in a closed loop gain error, e.g. if $R_S = 10\Omega$, a gain error of 0.1% results. *Figures 1* and *2* show methods for accommodating non-zero source impedance.

DRIFT ERROR MINIMIZATION

In order to minimize drift error, care in selecting C_F and layout of the printed circuit board are required. The capacitor should be of high quality teflon, polycarbonate, or polystyrene construction. Board layout and clean lines are critical particularly at elevated temperature.

A ground guard (shield) surrounding pin 5 will minimize leakage currents to and from the summing junction, arising from extraneous signals. See AN-63 for detailed recommendations.

CAPACITOR SELECTION

The size of the capacitor is determined by the required drift rate usually at the expense of acquisition time.

The drift is dictated by leakage current at pin 5 and is given by:

$$\frac{dv}{dt} = \frac{I_L}{C_F}$$

Where I_L is the leakage current at pin 5 and C_F is the value of the capacitance. The room temperature leakage of the LH0053 is typically 6.0 pA, and a 1000 pF capacitor will yield a drift rate of 6.0 mV per second.

For values of C_F below 1000 pF, acquisition for the LH0053 is primarily governed by the slew rate of the input amplifier (20 V/μs) and the setting time of the output amplifier ($\cong$1.0 μs). For values above C_F = 1000 pF, acquisition time is given by:

$$t_a = \frac{C_F \Delta V}{I_{DSS}} + t_{S2}$$

Where:

C_F = The value of the capacitor

ΔV = The magnitude of the input step, e.g. 20V

I_{DSS} = The ON current of switch Q1 $\cong$ 5.0 mA

t_{S2} = The setting time of output amplifier $\cong$ 1.0 μs

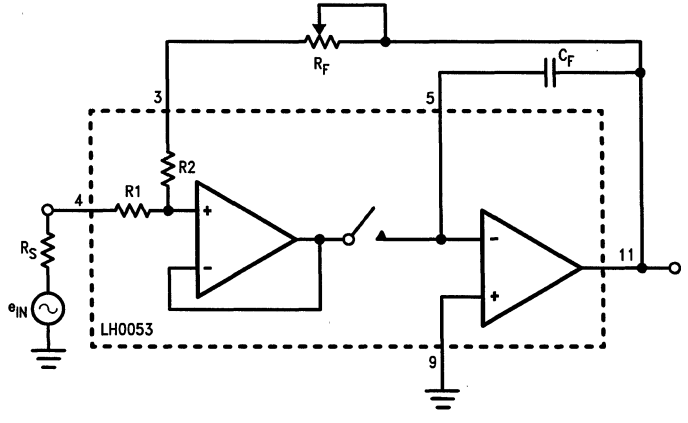

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FIGURE 1. Non-Zero Source Impedance Compensation

Applications Information (Continued)

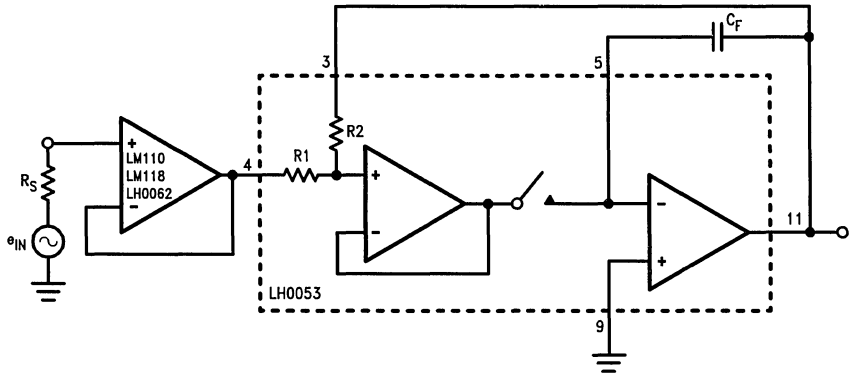

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FIGURE 2. Non-Zero Source Impedance Buffering

GATE INPUT CONSIDERATIONS

5.0V TTL Applications

The LH0053 Gate input (pin 6) will interface directly with 5.0V TTL. However, TTL gates typically pull up to 2.5V in the logic "1" state. It is therefore advisable to use a 10 kΩ pull-up resistor between the 5.0V, V_{CC}, and the output of the gate as shown in *Figure 3*.

To obtain the highest speed and fastest acquisition time, the gate drive shown in *Figure 6* is recommended.

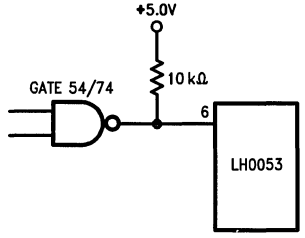

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FIGURE 3. TTL Logic Compatibility

CMOS APPLICATIONS

The LH0053 gate input may be interfaced directly with 74C, CMOS operating off of V_{CC}'s from 5.0V to 15V. However, transient currents of several milliamps can flow on the rising and falling edges of the input signal. It is, therefore, advisable to parallel the outputs of two 54C/74C gates as shown in *Figure 4*.

It should be noted that leakage at pin 5 in the hold mode will be increased by a factor of 2 to 3 when operating into 15V logic levels.

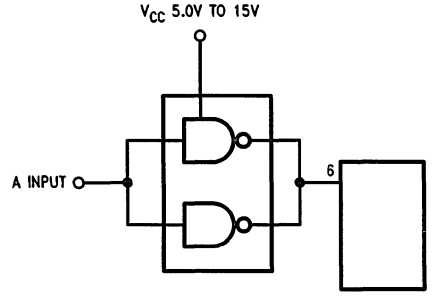

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FIGURE 4. CMOS Logic Compatibility

HEAT SINKING

The LH0053 may be operated over the military temperature range, −55°C to +125°C, without incurring damage to the device. However, a clip on heat sink such as the Wakefield 215 Series or Thermalloy 2240 will reduce the internal temperature rise by about 20°C. The result is two-fold improvement in drift rate at an ambient temperature of 25°C.

Since the case of the device is electrically isolated from the circuit, the LH0053 may be mounted directly to a grounded heat sink.

POWER SUPPLY DECOUPLING

Amplifiers A1 and A2 within the LH0053 are very wide band devices and are sensitive to power supply inductance. It is advisable to bypass V^+ (pin 12) and V^- (pin 10) to ground with 0.1 μF disc capacitors in order to prevent oscillation.

Applications Information (Continued)

Should this procedure prove inadequate, the disc capacitors should be paralleled with 4.7 μF solid tantalum electrolytic capacitors.

DC OFFSET ADJUST

Output offset error may be adjusted to zero using the circuit shown in *Figure 5.* Offset null should be accomplished in the sample mode ($V_6 \leq 0.5V$) and analog input (pin 4) equal to zero volts.

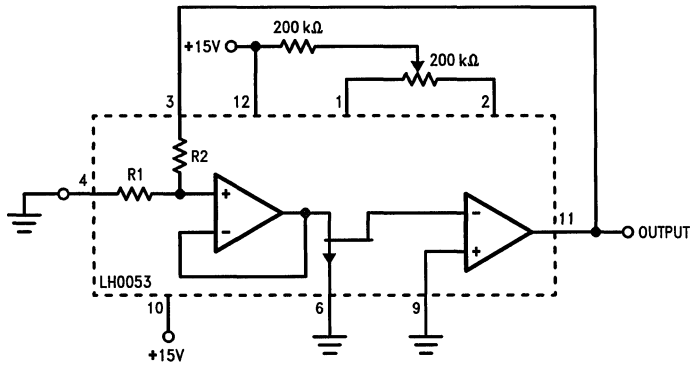

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FIGURE 5. Offset Null Circuit

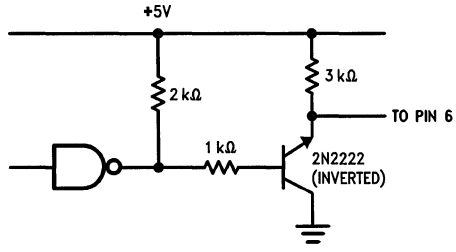

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FIGURE 6. High Speed Gate Drive Circuit

Definition of Terms

Voltage V_4: The voltage at pin 4, i.e., the analog input voltage.

Voltage V_6: The voltage at pin 6, i.e., the logic control signal. A logic "1" input, $V_6 \leq 4.5V$, places the LH0053 in the HOLD mode; a logic "0" input ($V_6 \leq 0.5V$) places the device in sample mode.

Acquisition Time: The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to Analog Input 1 (pin 4) with logic input, (pin 6) in the logic "0" state.

Aperture Time: The time indeterminacy when switching from the "sample" mode to the HOLD mode measured from the time the logic input passes through its threshold (2.0V) to the time the device actually enters the HOLD mode.

Sample Accuracy: Difference between input voltage and output voltage while in the sample mode, expressed as a percent of the input voltage.