

LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

Check for Samples: [LF412-N](#)

FEATURES

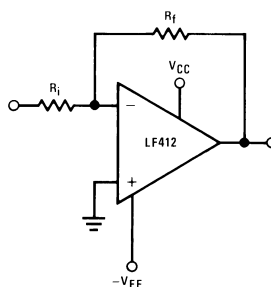
- Internally Trimmed Offset Voltage: 1 mV (max)
- Input Offset Voltage Drift: 10 $\mu\text{V}/^\circ\text{C}$ (max)
- Low Input Bias Current: 50 pA
- Low Input Noise Current: 0.01 pA / $\sqrt{\text{Hz}}$
- Wide Gain Bandwidth: 3 MHz (min)
- High Slew Rate: 10V/ μs (min)
- Low Supply Current: 1.8 mA/Amplifier
- High Input Impedance: $10^{12}\Omega$
- Low Total Harmonic Distortion: $\leq 0.02\%$
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 μs

DESCRIPTION

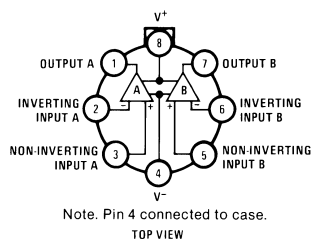
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Typical Connection


Figure 1.

Connection Diagram


**Figure 2. TO Package – Top View
See Package Number NEV0008A**


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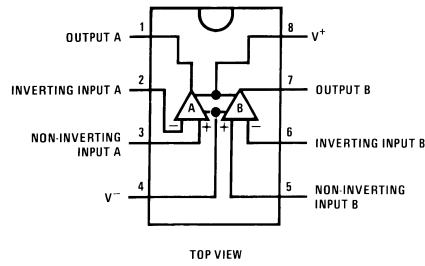
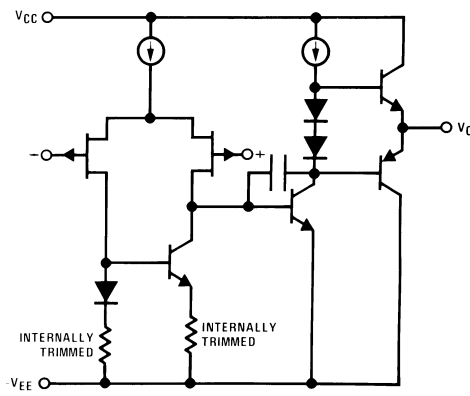


Figure 3. PDIP/CDIP Package – Top View
See Package Number P0008E or NAB0008A

Simplified Schematic



(1) Available per JM38510/11905

Figure 4. 1/2 Dual

Detailed Schematic

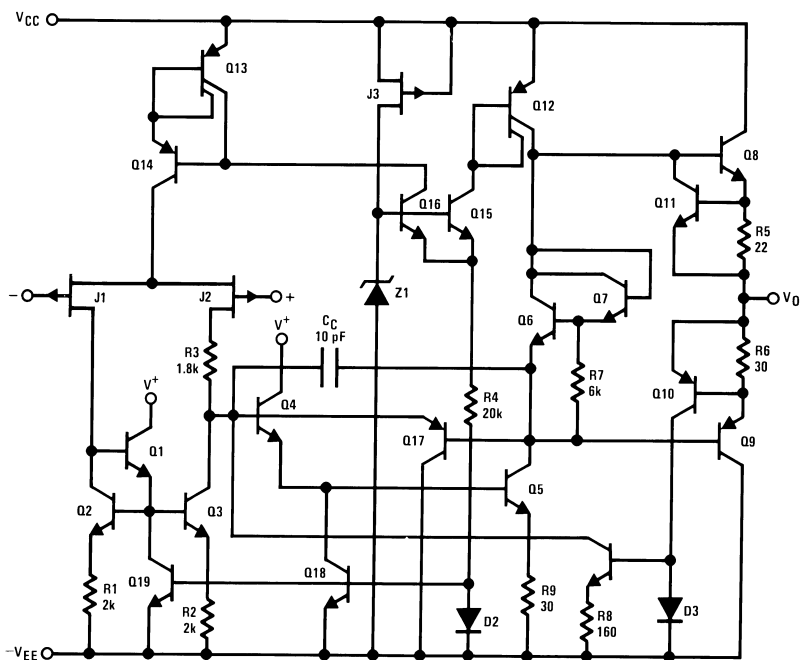


Figure 5.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾ ⁽²⁾

| | LF412A | LF412 |
|--|--------------------------------|--------------------------------|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input voltage Range ⁽³⁾ | | |
| Output Short Circuit Duration ⁽⁴⁾ | Continuous | Continuous |
| | TO Package | PDIP Package |
| Power Dissipation ⁽⁵⁾ | See ⁽⁶⁾ | 670 mW |
| T _j max | 150°C | 115°C |
| θ _{JA} (Typical) | 152°C/W | 115°C/W |
| Operating Temp. Range | See ⁽⁷⁾ | See ⁽⁷⁾ |
| Storage Temp. Range | -65°C ≤ T _A ≤ 150°C | -65°C ≤ T _A ≤ 150°C |
| Lead Temp. (Soldering, 10 sec.) | 260°C | 260°C |
| ESD Tolerance ⁽⁸⁾ | 1700V | 1700V |

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.
- (2) Refer to RETS412X for LF412MH and LF412MJ military specifications.
- (3) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
- (4) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
- (5) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.
- (6) For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA}.
- (7) These devices are available in both the commercial temperature range 0°C ≤ T_A ≤ 70°C and the military temperature range -55°C ≤ T_A ≤ 125°C. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in TO package only. In all cases the maximum operating temperature is limited by internal junction temperature T_j max.
- (8) Human body model, 1.5 kΩ in series with 100 pF.

DC Electrical Characteristics

| Symbol | Parameter | Conditions | LF412A ⁽¹⁾ | | | LF412 ⁽¹⁾ | | | Units |
|----------------------|------------------------------------|---|-----------------------|------------------|-----|----------------------|-------|-----|-------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{OS} | Input Offset Voltage | R _S =10 kΩ, T _A =25°C | | 0.5 | 1.0 | | 1.0 | 3.0 | mV |
| ΔV _{OS} /ΔT | Average TC of Input Offset Voltage | R _S =10 kΩ ⁽²⁾ | | 7 | 10 | | 7 | 20 | μV/°C |
| I _{OS} | Input Offset Current | V _S =±15V ^{(1) (3)} | T _J =25°C | 25 | 100 | | 25 | 100 | pA |
| | | | T _J =70°C | | | 2 | | 2 | nA |
| | | | T _J =125°C | | | 25 | | 25 | nA |
| I _B | Input Bias Current | V _S =±15V ^{(1) (3)} | T _J =25°C | 50 | 200 | | 50 | 200 | pA |
| | | | T _J =70°C | | | 4 | | 4 | nA |
| | | | T _J =125°C | | | 50 | | 50 | nA |
| R _{IN} | Input Resistance | T _J =25°C | | 10 ¹² | | 10 ¹² | | Ω | |
| A _{VOL} | Large Signal Voltage Gain | R _L =2k, T _A =25°C | 50 | 200 | | 25 | 200 | | V/mV |
| | | V _S =±15V, V _O =±10V, Over Temperature | 25 | 200 | | 15 | 200 | | V/mV |
| | | | | | | | | | |
| V _O | Output Voltage Swing | V _S =±15V, R _L =10k | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| V _{CM} | Input Common-Mode Voltage Range | | ±16 | +19.5 | | ±11 | +14.5 | | V |
| | | | | -16.5 | | | -11.5 | | V |
| CMRR | Common-Mode Rejection Ratio | R _S ≤10k | 80 | 100 | | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | | ⁽⁴⁾ 80 | 100 | | 70 | 100 | | dB |
| I _S | Supply Current | V _O = 0V, R _L = ∞ | | 3.6 | 5.6 | | 3.6 | 6.5 | mA |

- (1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S=±20V for the LF412A and for V_S=±15V for the LF412. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.
- (2) The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 85% of the amplifiers meet this specification.
- (3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_J=T_A+θ_JA P_D where θ_JA is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
- (4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

AC Electrical Characteristics

| Symbol | Parameter | Conditions | LF412A ⁽¹⁾ | | | LF412 ⁽¹⁾ | | | Units |
|----------------|---------------------------------|--|-----------------------|-------|-----|----------------------|-------|-----|----------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | T _A =25°C, f=1 Hz-20 kHz (Input Referred) | | -120 | | | -120 | | dB |
| SR | Slew Rate | V _S =±15V, T _A =25°C | 10 | 15 | | 8 | 15 | | V/μs |
| GBW | Gain-Bandwidth Product | V _S =±15V, T _A =25°C | 3 | 4 | | 2.7 | 4 | | MHz |
| THD | Total Harmonic Dist | A _V =+10, R _L =10k, V _O =20 Vp-p, BW=20 Hz-20 kHz | | ≤0.02 | | | ≤0.02 | | % |
| e _n | Equivalent Input Noise Voltage | T _A =25°C, R _S =100Ω, f=1 kHz | | 25 | | | 25 | | nV / √Hz |
| i _n | Equivalent Input Noise Current | T _A =25°C, f=1 kHz | | 0.01 | | | 0.01 | | pA / √Hz |

- (1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S=±20V for the LF412A and for V_S=±15V for the LF412. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.

Typical Performance Characteristics

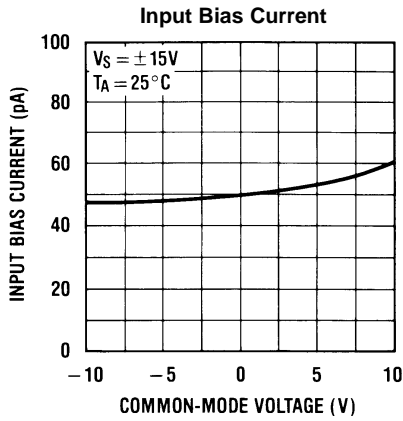


Figure 6.

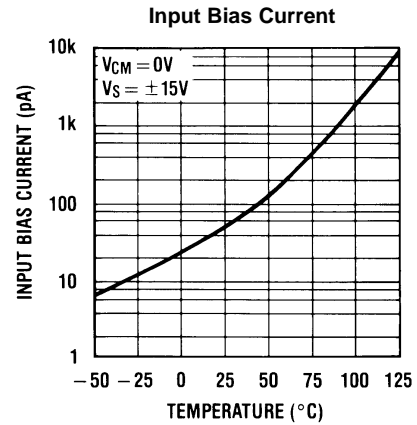


Figure 7.

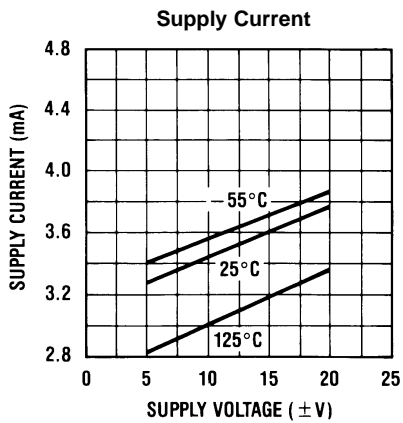


Figure 8.

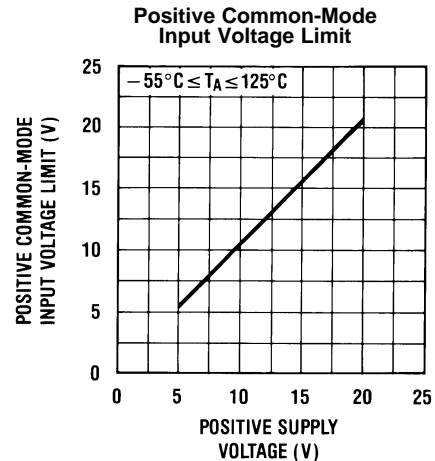


Figure 9.

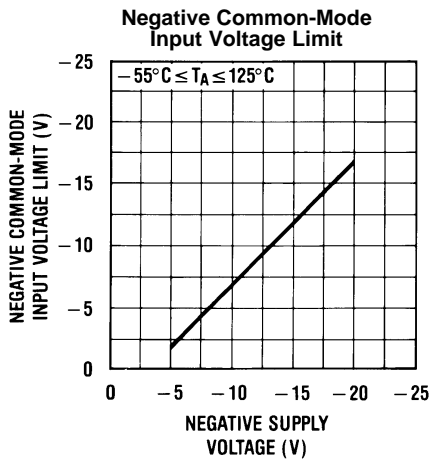


Figure 10.

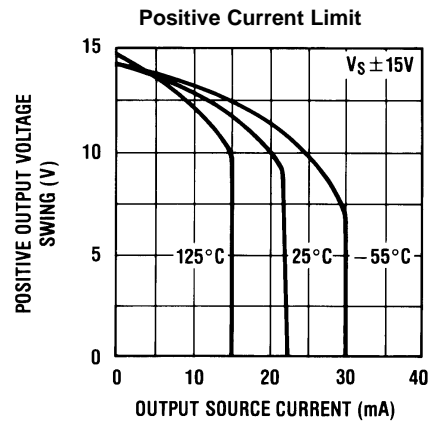


Figure 11.

Typical Performance Characteristics (continued)

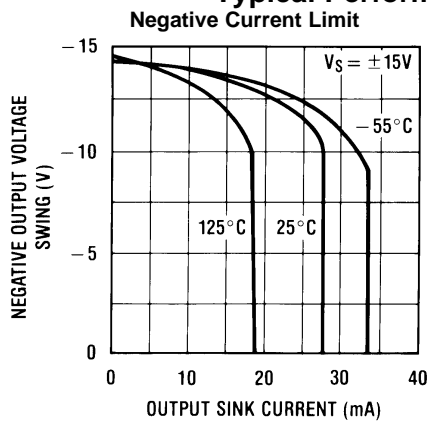


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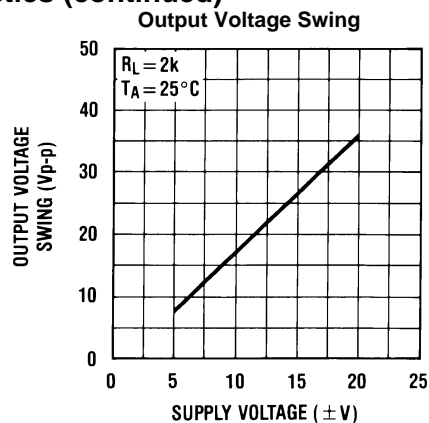


Figure 13.

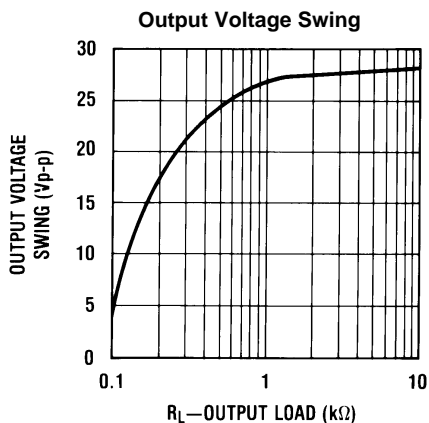


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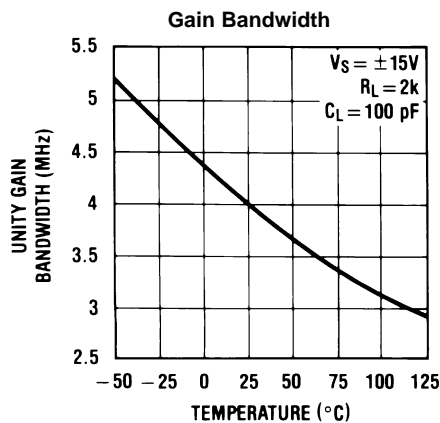


Figure 15.

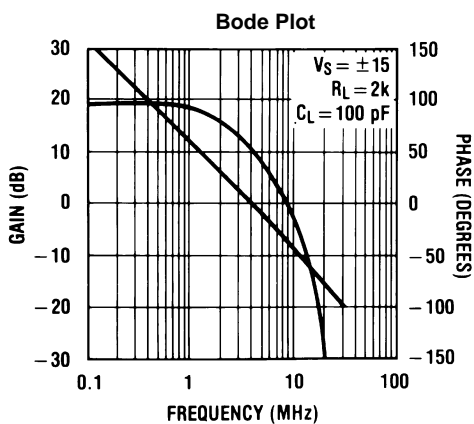


Figure 16.

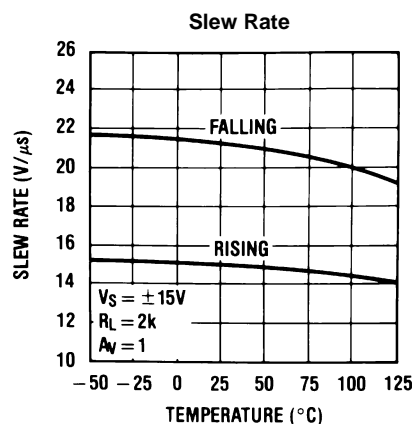
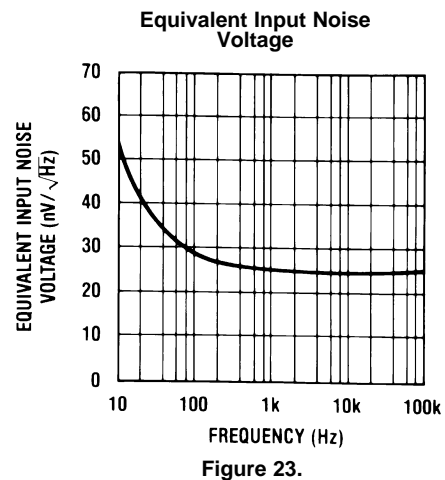
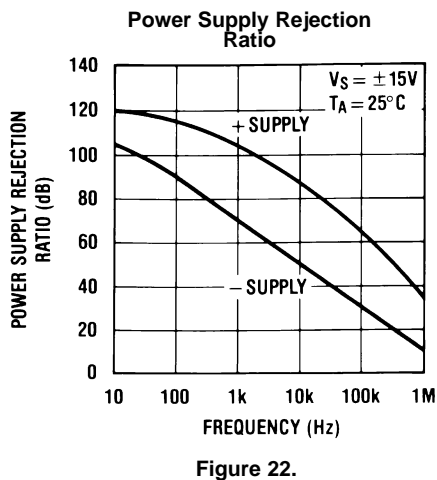
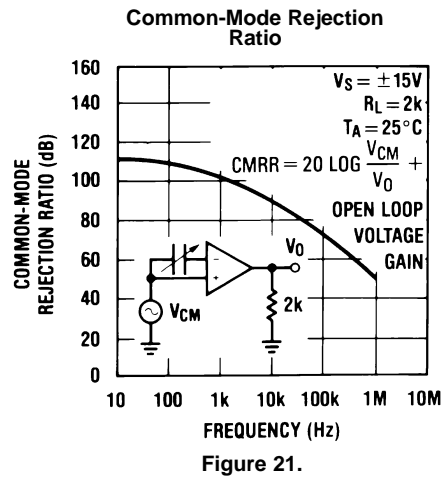
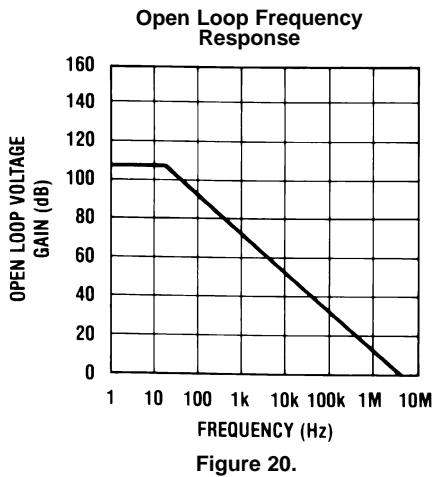
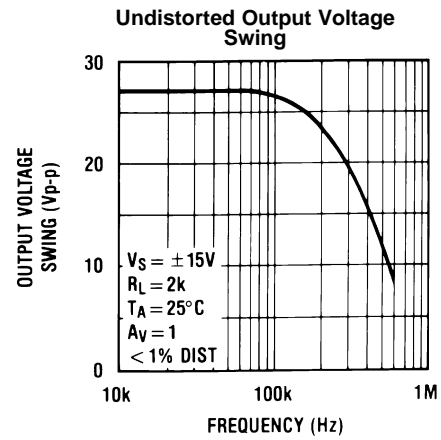
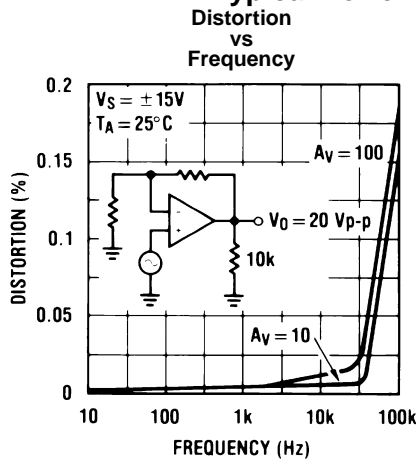


Figure 17.

Typical Performance Characteristics (continued)



Typical Performance Characteristics (continued)

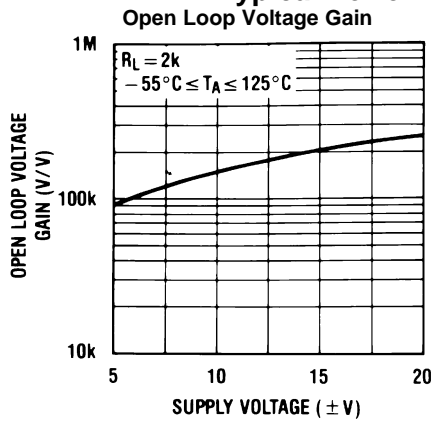


Figure 24.

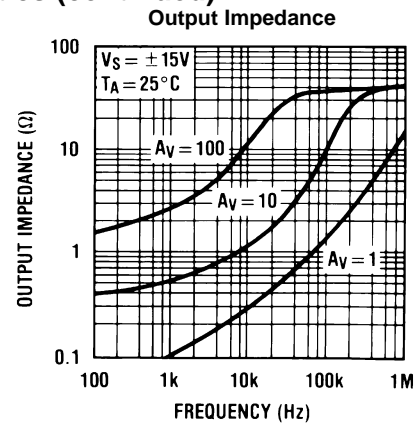


Figure 25.

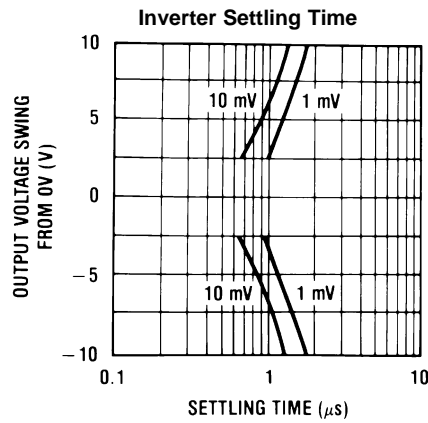


Figure 26.

PULSE RESPONSE

$R_L=2\text{ k}\Omega$, $C_L=10\text{ pF}$

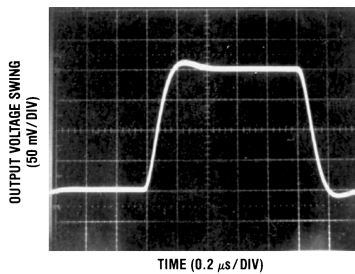


Figure 27. Small Signal Inverting

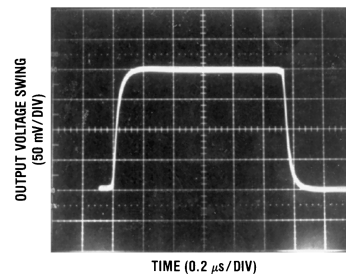


Figure 28. Small Signal Non-Inverting

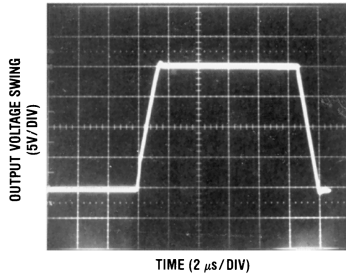


Figure 29. Large Signal Inverting

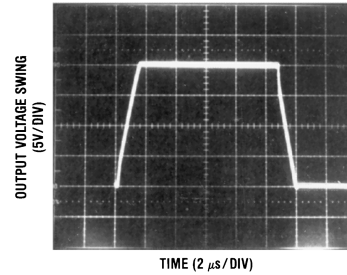


Figure 30. Large Signal Non-Inverting

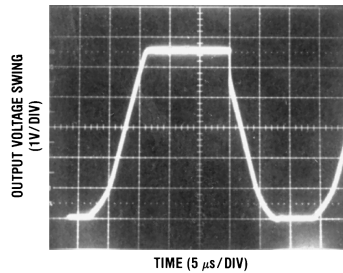


Figure 31. Current Limit ($R_L=100\Omega$)

APPLICATION HINTS

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 6.0V$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 k Ω load resistance to $\pm 10V$ over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

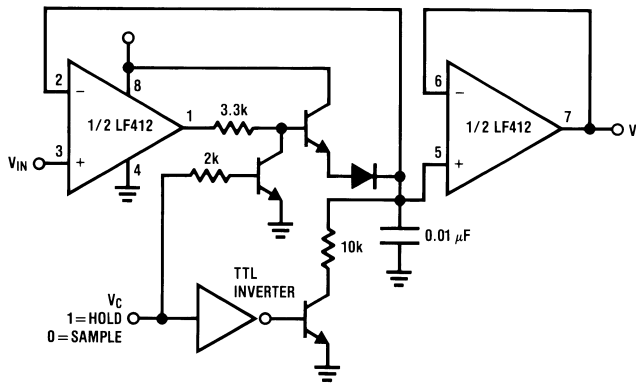
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

TYPICAL APPLICATION

Figure 32. Single Supply Sample and Hold



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| LF412ACN | ACTIVE | PDIP | P | 8 | 40 | TBD | Call TI | Level-1-NA-UNLIM | 0 to 70 | LF 412ACN | Samples |
| LF412ACN/NOPB | ACTIVE | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | Call TI | Level-1-NA-UNLIM | 0 to 70 | LF 412ACN | Samples |
| LF412CN | ACTIVE | PDIP | P | 8 | 40 | TBD | Call TI | Level-1-NA-UNLIM | 0 to 70 | LF 412CN | Samples |
| LF412CN/NOPB | ACTIVE | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | Call TI | Level-1-NA-UNLIM | 0 to 70 | LF 412CN | Samples |
| LF412MH | ACTIVE | TO | NEV | 8 | 500 | TBD | POST-PLATE | Level-1-NA-UNLIM | -55 to 125 | LF412MH | Samples |
| LF412MH/NOPB | ACTIVE | TO | NEV | 8 | 500 | Green (RoHS & no Sb/Br) | POST-PLATE | Level-1-NA-UNLIM | -55 to 125 | LF412MH | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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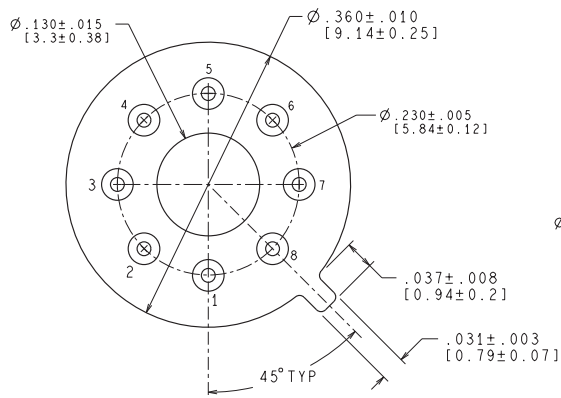
P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



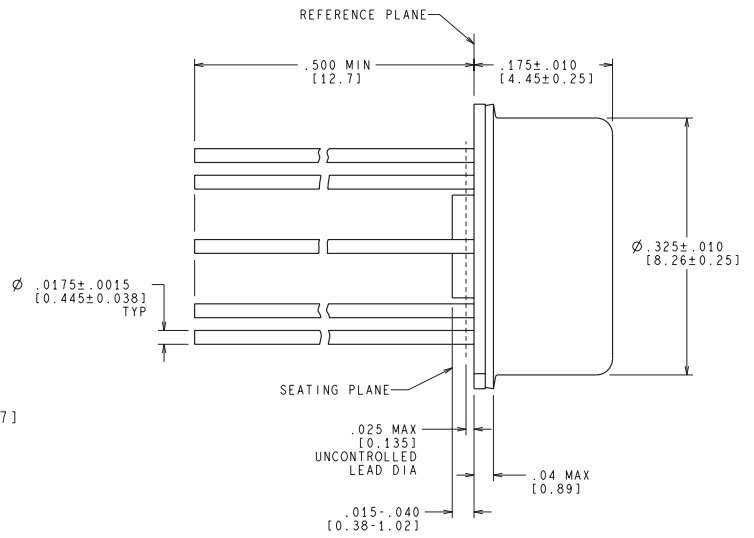
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

NEV0008A



MIL-PRF-38535
CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE IN MILLIMETERS



H08A (REV C)

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