Ordering number : EN*5391

NMOS + CCD

LC89975M

PAL-Format Delay Line

Preliminary

Overview

The LC89975M is a lower-cost PAL-Format CCD delay line based on the LC89970M, with the sizes of chip and package miniaturized and the external parts count reduced.

Features

- 5 V single-voltage power supply
- On-chip 3× PLL circuit for 3·fsc operation from an fsc (4.43 MHz) input
- Supports PAL/GBI and 4.43 NTSC systems, selected by a control pin input
- Includes an on-chip comb filter for chrominance signal crosstalk exclusion. This adjustment-free circuit provides high-precision comb characteristics.
- Peripheral circuits included on chip to allow operation with minimal external circuits.
- Positive-phase signal input, positive phase signal output (luminance signal)

Functions

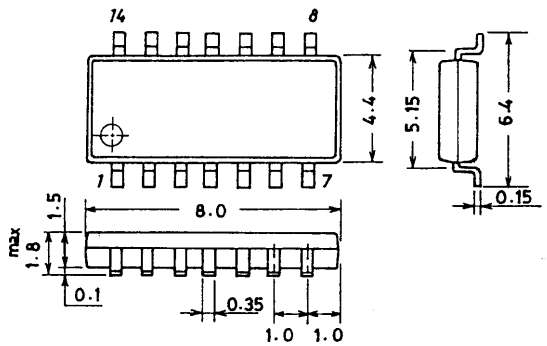
- CCD shift register (for chrominance and luminance signals)
- CCD drive circuit
- Circuit for switching the number of CCD stages
- CCD signal addition circuit
- Auto-bias circuit
- Sync tip clamping circuit (luminance signal)
- Center bias circuit (chrominance signal)
- Sample-and-hold circuit
- PLL 3× circuit
- 3·fsc clock output circuit
- RD voltage generation step-up circuit

Package Dimensions

unit: mm

3111-MFP14S

[LC89975M]



SANYO: MFP14S

Specifications

Absolute Maximum Ratings at Ta = 25°C

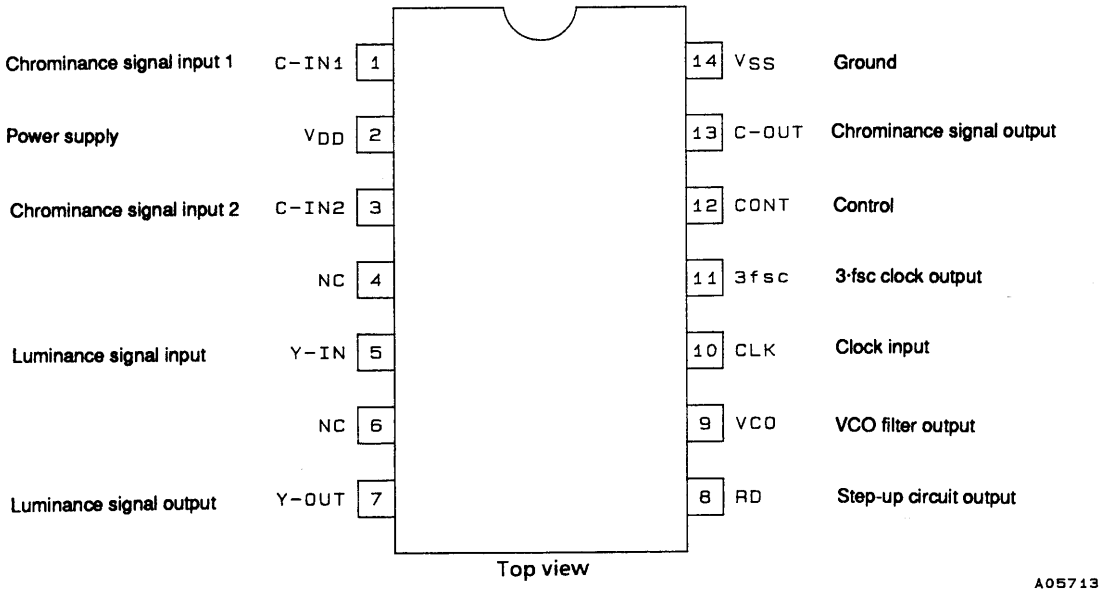
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.0	V
Allowable power dissipation	Pdmax		250	mW
Operating temperature	Topr		–10 to +60	°C
Storage temperature	Tstg		–55 to +150	°C

Recommended Conditions at Ta = 25°C

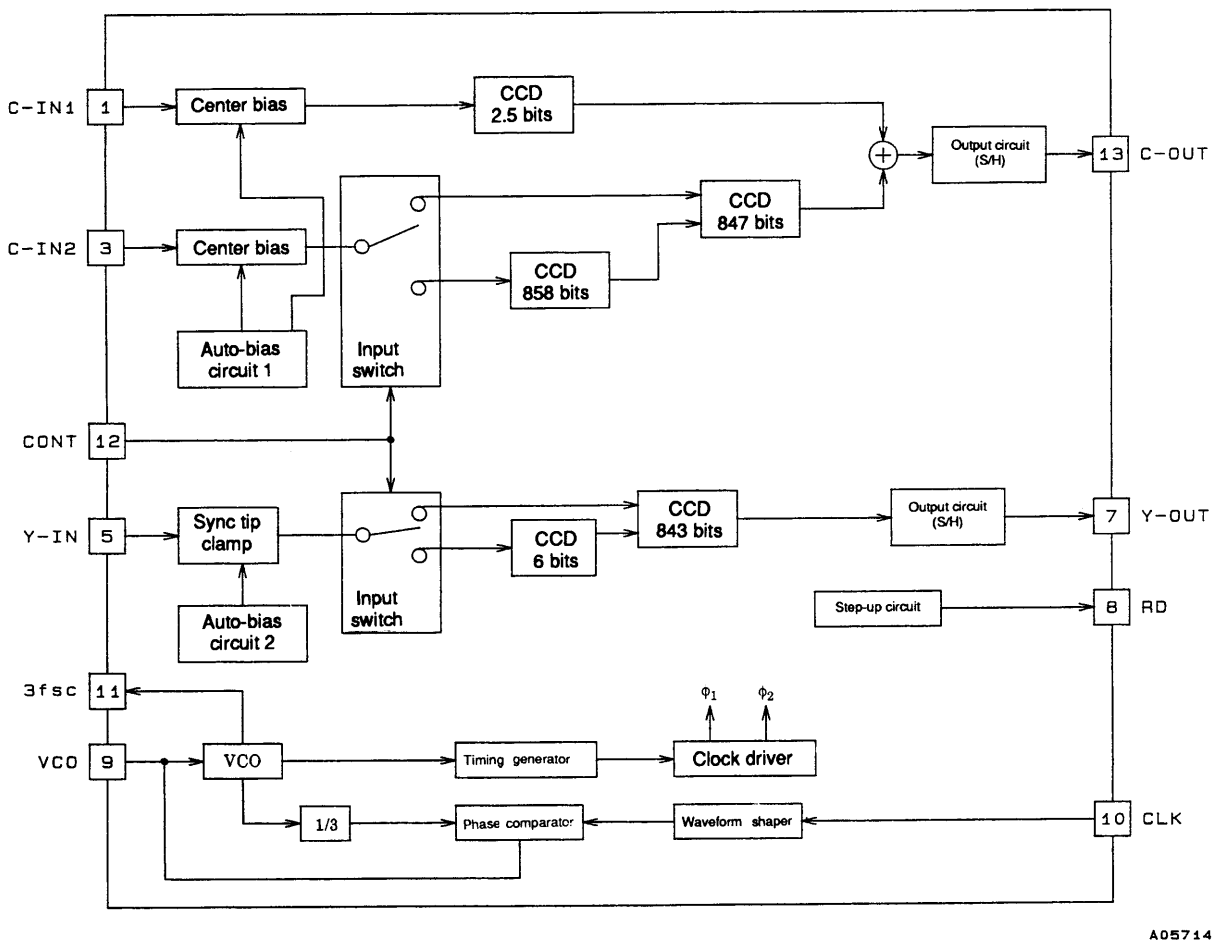
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Clock input amplitude	V_{CLK}		300	500	1000	mVp-p
Clock frequency	F_{CLK}	Sine wave	—	4.43361875	—	MHz
Chrominance signal input amplitude	V_{IN-C}		—	350	500	mVp-p
Luminance signal input amplitude	V_{IN-Y}		—	400	572	mVp-p

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-0005 JAPAN

Pin Assignment



Block Diagram



Control Pin

CONT	Mode (typical example)	Chrominance signal delay (number of CCD stages)	Luminance signal delay (number of CCD stages)
Low	PAL/GBI	2H (1705) + 0H (2.5)	1H (849)
High	4.43 NTSC	1H (847) + 0H (2.5)	1H (843)

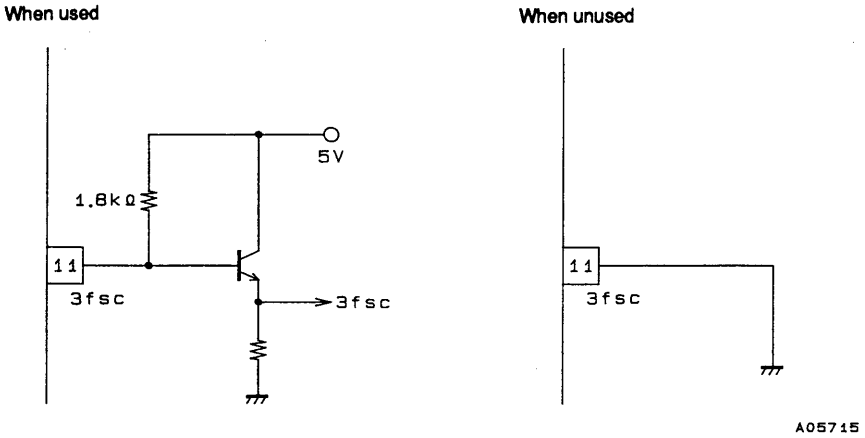
Switching levels

Low/High	Symbol	min	typ	max	Unit
Low	V_L	–0.3	0.0	+0.5	V
High	V_H	2.0	5.0	6.0	V

Note: Since a pull-down resistor of about 70 kΩ is built in the control pin circuit, it will remain fixed at the low level if left open.

3fsc Pin

This pin outputs the 3·fsc clock signal generated by the PLL 3× circuit.



Electrical Characteristics at V_{DD} = 5.0 V, Ta = 25°C, F_{CLK} = 4.43361875 MHz, V_{CLK} = 500 mVp-p

Parameter	Symbol	Test conditions	Switch states			min	typ	max	Unit
			SW1	SW2	SW3				
Power-supply current	I_{DD-1}	1	a	a	b	27	32	37	mA
	I_{DD-2}		b	a	b				

Chrominance System Characteristics (with no signal applied to the Y-IN pin)

Parameter	Symbol	Test conditions	Switch states			min	typ	max	Unit
			SW1	SW2	SW3				
Pin voltage (input)	V_{INC-1}	2	a	a	b	2.2	2.7	3.2	V
	V_{INC-2}		b	a	b				
Pin voltage (output)	V_{OUTC-1}		a	a	b	1.5	2.0	2.5	V
	V_{OUTC-2}		b	a	b				
Voltage gain	G_{VC-1}	3	a	a	b	0	2	4	dB
	G_{VC-2}		b	a	b				
Comb depth	C_{D-1}	4	a	a	b	—	–40	–35	dB
	C_{D-2}		b	a	b				
Linearity	L_{NC-1}	5	a	a	b	–0.3	0.0	+0.3	dB
	L_{NC-2}		b	a	b				
Clock leakage (3·fsc)	L_{CK3C-1}	6	a	a	b	—	10	50	mVrms
	L_{CK3C-2}		b	a	b				
Clock leakage fsc)	L_{CK1C-1}		a	a	b	—	0.5	1.5	mVrms
	L_{CK1C-2}		b	a	b				
Noise	N_{C-1}	7	a	a	b	—	0.5	2.0	mVrms
	N_{C-2}		b	a	b				
Output impedance	Z_{OC-1}	8	a	a	a, b	200	350	500	Ω
	Z_{OC-2}		b	a	a, b				
0H delay time	T_{DC-1}	9	a	a	b	—	245	—	ns
	T_{DC-2}		b	a	b				

Luminance System Characteristics (with no signals applied to the C-IN1 and C-IN2 pins)

Parameter	Symbol	Test conditions	Switch states			min	typ	max	Unit
			SW1	SW2	SW3				
Pin voltage (input)	V_{INY-1}	10	a	a	b	1.7	2.2	2.7	V
	V_{INY-2}		b	a	b				
Pin voltage (output)	V_{OUTY-1}		a	a	b	0.8	1.3	1.8	V
	V_{OUTY-2}		b	a	b				
Voltage gain	G_{VY-1}	11	a	a	b	0	2	4	dB
	G_{VY-2}		b	a	b				
Frequency response	G_{FY-1}	12	a	b	b	–2	0	2	dB
	G_{FY-2}		b	b	b				
Differential gain	D_{GY-1}	13	a	a	b	0	5	7	%
	D_{GY-2}		b	a	b				
Differential phase	D_{PY-1}		a	a	b	0	5	7	deg
	D_{PY-2}		b	a	b				
Linearity	L_{SY-1}	14	a	a	b	37	40	43	%
	L_{SY-2}		b	a	b				
Clock leakage (3·fsc)	L_{CK3Y-1}	15	a	a	b	—	10	50	mVrms
	L_{CK3Y-2}		b	a	b				
Clock leakage (fsc)	L_{CK1Y-1}		a	a	b	—	0.5	1.5	mVrms
	L_{CK1Y-2}		b	a	b				
Noise	N_{Y-1}	16	a	a	b	—	0.5	2.0	mVrms
	N_{Y-2}		b	a	b				
Output impedance	Z_{OY-1}	17	a	a	c, b	250	400	550	Ω
	Z_{OY-2}		b	a	c, b				
Delay time	T_{DY-1}	18	a	a	b	—	63.88	—	µs
	T_{DY-2}		b	a	b	—	63.43	—	

Test Conditions

1. Power-supply current with no input signal applied

2. Pin output voltage with no input signal applied (center bias voltage)

3. Measure the C-OUT output when 350-mVp-p sine wave signals are input to C-IN1 and C-IN2.

$$G_{VC} = 20 \log \frac{\text{C-OUT output [mVp-p]}}{350\ \text{[mVp-p]}}\ \text{[dB]}$$

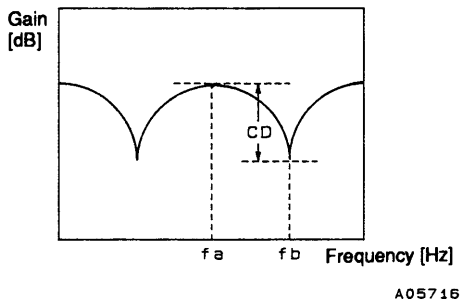
Measured frequencies

G_{VC-1}	4.429662 MHz	(PAL/GBI)
G_{VC-2}	4.425694 MHz	(4.43 NTSC)

4. Measure the comb depth from the C-OUT output when 350-mVp-p sine wave signals of frequency fa are input to C-IN1 and C-IN2 and when signals of frequency fb are input.

$$C_D = 20 \log \frac{\text{The C-OUT output for an fb input [mVp-p]}}{\text{The C-OUT output for an fa input [mVp-p]}}\ \text{[dB]}$$

Measured frequencies	fa	fb	
C_{D-1}	4.429662 MHz	4.425756 MHz	(PAL/GBI)
C_{D-2}	4.425694 MHz	4.417819 MHz	(4.43 NTSC)



5. Measure the C-OUT output when 200-mVp-p sine wave signals are input to C-IN1 and C-IN2 and when 500-mVp-p sine wave signals are input and calculate the gain difference.

$$L_{NC} = 20 \log \left(\frac{\text{Output for a 500-mVp-p input [mVp-p]}}{500\ \text{[mVp-p]}} \Big/ \frac{\text{Output for a 200-mVp-p input [mVp-p]}}{200\ \text{[mVp-p]}} \right)\ \text{[dB]}$$

Measured frequencies

L_{NC-1}	4.429662 MHz	(PAL/GBI)
L_{NC-2}	4.425694 MHz	(4.43 NTSC)

6. Measure the 3·fsc (13.3 MHz) and fsc (4.43 MHz) components in the C-OUT output with no input signal applied.

7. Measure the noise in the C-OUT output with no input signal applied.
Set up the noise meter with a 200-kHz high-pass filter and a 5-MHz low-pass filter.

8. Let V1 be the C-OUT output when 350-mVp-p sine wave signals are input to C-IN1 and C-IN2 with SW3 in the a position, and V2 be the C-OUT output with SW3 in the b position.

$$Z_{OC} = \frac{\text{V2 [mVp-p]} - \text{V1 [mVp-p]}}{\text{V1 [mVp-p]}} \times 500\ [\Omega]$$

Measured frequencies

Z_{OC-1}	4.429662 MHz	(PAL/GBI)
Z_{OC-2}	4.425694 MHz	(4.43 NTSC)

9. The C-OUT output delay time with respect to a C-IN1 input (the 2.5-bit CCD delay)

10. The pin output voltage when no input signal is applied (the clamp voltage)

11. Measure the Y-OUT output when a 200-kHz 400-mVp-p sine wave is input to Y-IN.

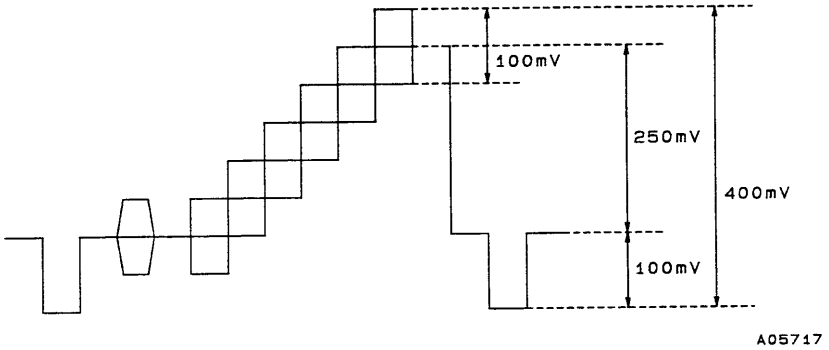
$$G_{VY} = 20 \log \frac{\text{Y-OUT output [mVp-p]}}{400 \text{ [mVp-p]}} \text{ [dB]}$$

12. Measure the Y-OUT output when a 200-kHz 200-mVp-p sine wave is input to Y-IN and when 3.3-MHz 200-mVp-p sine wave is input.

$$G_{FY} = 20 \log \frac{\text{The Y-OUT output for a 3.3-MHz input [mVp-p]}}{\text{The Y-OUT output for a 200-kHz input [mVp-p]}} \text{ [dB]}$$

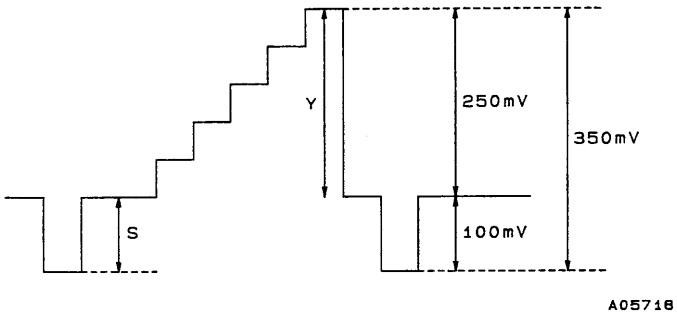
Adjust Vbias to set the bias to the clamp level plus 250 mV.

13. Apply a 5-step waveform (see the figure) to Y-IN and measure the Y-OUT output differential gain and differential phase with a vectorscope.



14. Apply a 5-step waveform (see the figure) to Y-IN and measure the Y-OUT output luminance signal level (Y) and sync level (S).

$$L_{SY} = \frac{S \text{ [mV]}}{Y \text{ [mV]}} \times 100 \text{ [\%]}$$



15. Measure the 3·fsc (13.3 MHz) and fsc (4.43 MHz) components in the Y-OUT output with no input signal applied.

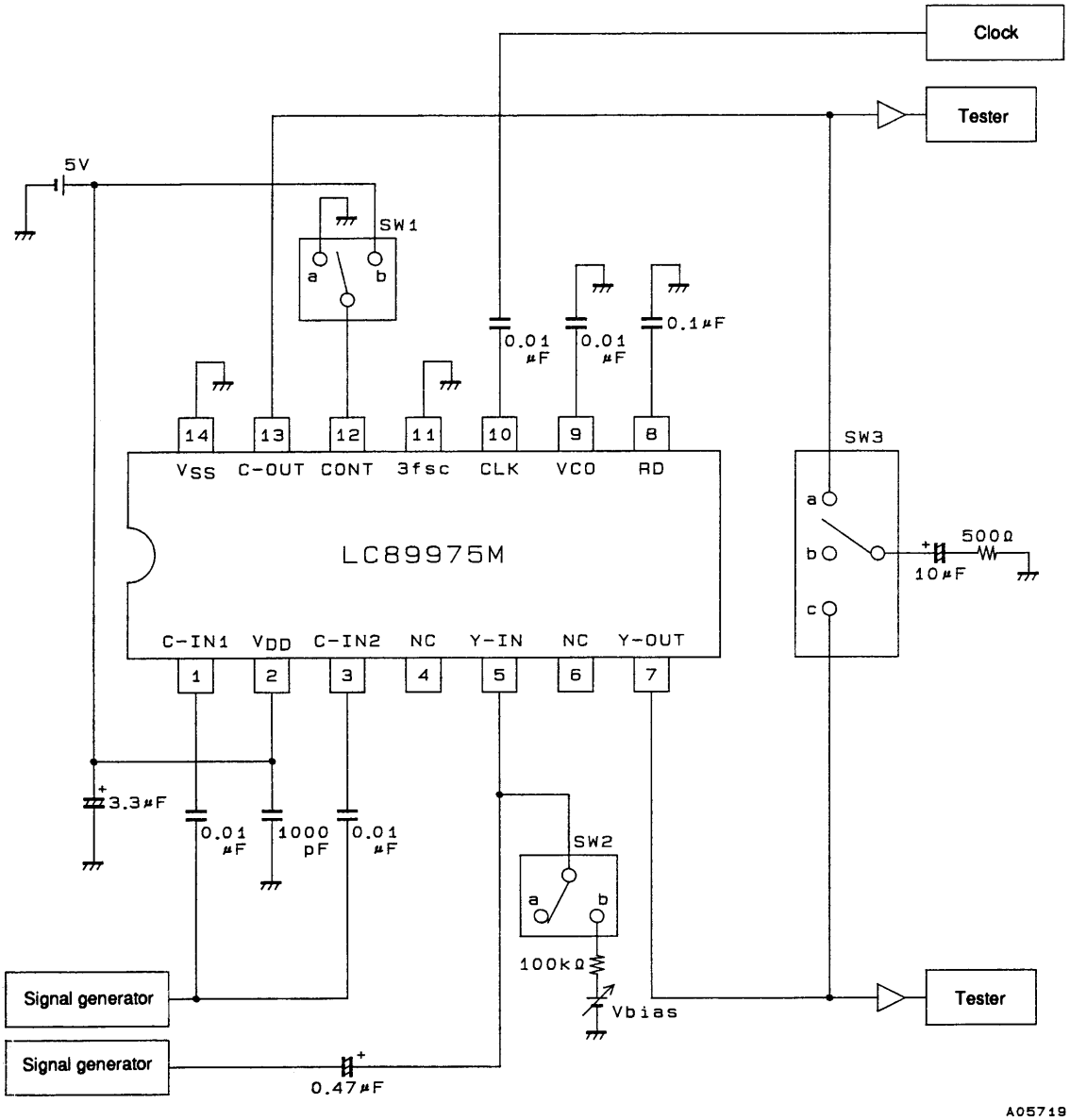
16. Measure the noise in the Y-OUT output with no input signal applied.
Set up the noise meter with a 200-kHz high-pass filter, a 5-MHz low-pass filter, and a 4.43-MHz trap filter.

17. Let V1 be the Y-OUT output when a 200-kHz 400-mVp-p sine wave signal is input to Y-IN and with SW3 in the c position, and V2 be the Y-OUT output with SW3 in the b position.

$$Z_{OY} = \frac{\text{V2 [mVp-p]} - \text{V1 [mVp-p]}}{\text{V1 [mVp-p]}} \times 500 \text{ [}\Omega\text{]}$$

18. The Y-OUT output delay time with respect to inputs to Y-IN.

Test Circuit



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