Ordering number : EN*4852B

CMOS LSI

LC89512W

CD-ROM Error Correction LSI with Built-In SCSI Interface

Preliminary

Overview

The LC89512W integrates a real-time error correction circuit and a SCSI interface in a single chip.

Functions

- CD-ROM error correction function, subcode readout function, SCSI interface

Features

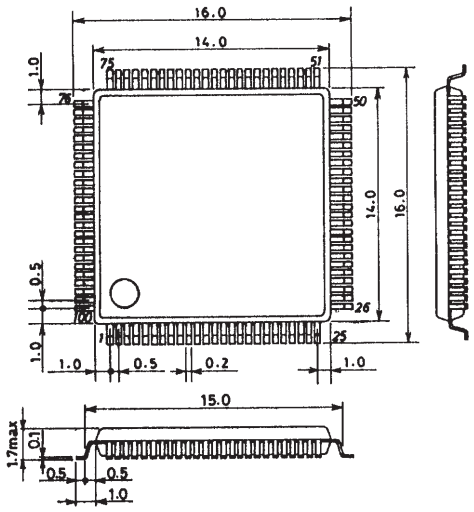
- Support for double-speed drives at an operating frequency of 16.9344 MHz
  Either SRAM (120 ns), DRAM (80 ns) or pseudo SRAM (85 ns) can be used.
- Support for quad-speed drives at an operating frequency of 33.8688 MHz
  SRAM (70 ns) must be used.
- Built-in SCSI interface with built-in 48 mA sink buffer (Only the TARGET function is supported.)
- Built-in 12-byte output FIFO for sub-CPU to host computer data transmission
- Built-in 12-byte input FIFO for host computer to sub-CPU data transmission
- Subcode data can be written to buffer RAM and the sub-CPU can read the subcode values by connecting the LC89512 to the CD-DSP subcode pin.
- Sub-CPU access of buffer RAM through the LC89512
- Built-in function for buffer RAM internal data transfer
- Pseudo-SRAM (128-kword × 8-bit and smaller) can be used.
- DRAM (two 256-kword × 4-bit chips or two 1-Mword × 4-bit chips) can be used.
- Transfer speeds:
  2.8 MB/second (asynchronous mode) (for CD-ROM decode only operation)
  4.2 MB/second (synchronous mode) (CD-ROM decode operation is not supported in synchronous mode)
  Both of these transfer modes use a 16.9344 MHz clock. (The transfer speed depends on the frequency used.)
- Operating frequencies: 16.9344 MHz (up to double speed), 33.8688 (quad speed)

Package Dimensions

unit: mm

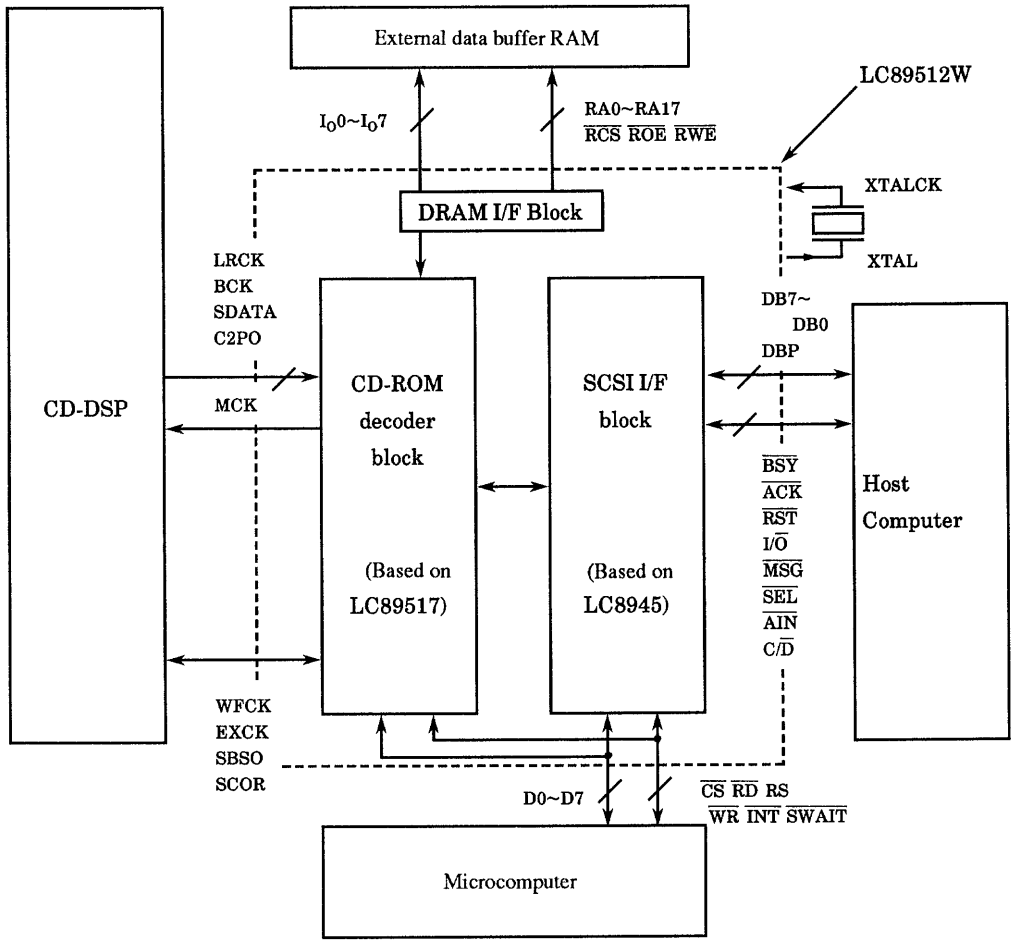
3181A-SQFP100

[LC89512W]



SANYO: SQFP100

Block Diagram



Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Pin	Type	Function
1	$\overline{DB7}$	B	SCSI connection
2	$V_{SS}1$	P	
3	$\overline{DBP}$	B	SCSI connection
4	$\overline{ATN}$	B	SCSI connection
5	$V_{SS}1$	P	
6	$\overline{BSY}$	B	SCSI connection
7	$\overline{ACK}$	B	SCSI connection
8	$V_{SS}1$	P	
9	$\overline{RST}$	B	SCSI connection
10	$\overline{MSG}$	B	SCSI connection
11	$V_{SS}1$	P	
12	$\overline{SEL}$	B	SCSI connection
13	C/D	B	SCSI connection
14	$V_{SS}1$	P	
15	$\overline{REQ}$	B	SCSI connection
16	I/O	B	SCSI connection
17	$V_{SS}0$	P	
18	I_O0	B	Data buffer RAM data signals These pins have built-in pull-up resistors.
19	I_O1	B	
20	I_O2	B	
21	I_O3	B	
22	I_O4	B	
23	I_O5	B	
24	I_O6	B	
25	I_O7	B	
26	$\overline{INT1}$	O	SCSI block interrupt request signal output (set using a register)
27	$V_{SS}0$	P	
28	$V_{SS}0$	P	
29	D0	B	Microprocessor data signals These pins have built-in pull-up resistors.
30	D1	B	
31	D2	B	
32	D3	B	
33	D4	B	
34	D5	B	
35	D6	B	
36	D7	B	
37	$\overline{INT0}$	O	Microprocessor interrupt request signal output
38	XTALCK	I	Crystal oscillator circuit input
39	XTAL	O	Crystal oscillator circuit output
40	$V_{SS}0$	P	
41	V_{DD}	P	
42	RA0	O	
43	RA1	O	Data buffer RAM address signal outputs
44	RA2	O	
45	RA3	O	
46	RA4	O	
47	RA5	O	
48	RA6	O	
49	RA7	O	
50	RA8	O	
51	RA9	O	
52	RA10	O	
53	RA11	O	

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Pin No.	Pin	Type	Function
54	RA12	O	Data buffer RAM address signal outputs
55	RA13	O	
56	RA14	O	
57	RA15	O	
58	RA16	O	
59	RA17	O	
60	V_{DD}	P	
61	$V_{SS}0$	P	
62	$\overline{RESET}$	I	Reset
63	TEST1	I	Test inputs. These pins should be tied low in normal operation.
64	TEST2	I	
65	TEST3	I	
66	WFCK	I	Subcode I/O
67	SBSO	I	
68	SCOR	I	
69	SDATA	I	Serial data input
70	BCK	I	Serial data input clock
71	LRCK	I	44.1 kHz strobe signal input
72	C2PO	I	C2 pointer input
73	$\overline{RD}$	I	Microprocessor data read signal input
74	$\overline{WR}$	I	Microprocessor data write signal input
75	$\overline{CS}$	I	Chip select signal input (from the microprocessor)
76	RS	I	Register selection signal input
77	$V_{SS}0$	P	
78	$\overline{SWAIT}$	O	Sub-CPU wait signal
79	EXCK	O	Sub code I/O
80	MCK	O	Crystal oscillator frequency output
81	TEST0	I	Test inputs. These pins should be tied low in normal operation
82	$\overline{RCS}$	O	RAM chip select
83	$\overline{RWE}$	O	RAM data write signal output
84	$\overline{ROE}$	O	RAM data read signal output
85		NC	
86		NC	
87		NC	
88		NC	
89	V_{DD}	P	
90	$V_{SS}1$	P	
91	$\overline{DB0}$	B	SCSI connection
92	$\overline{DB1}$	B	SCSI connection
93	$V_{SS}1$	P	
94	$\overline{DB2}$	B	SCSI connection
95	$\overline{DB3}$	B	SCSI connection
96	$V_{SS}1$	P	
97	$\overline{DB4}$	B	SCSI connection
98	$\overline{DB5}$	B	SCSI connection
99	$V_{SS}1$	P	
100	$\overline{DB6}$	B	SCSI connection

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Note: 1. NC must be left open. Do not connect any signals to these pins.
2. $V_{SS}0$ is the logic system ground and $V_{SS}1$ is the SCSI interface ground. (from the standard cell version)

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Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	–0.3 to +7.0	V
I/O voltages	V_I V_O	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	350	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering thermal stress limit (pins only)		10 seconds	260	°C

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	$V_{IH}1$	All input pins other than (1), (3), and XTALCK	2.2			V
Input low level voltage	$V_{IL}1$				0.8	V
Input high level voltage	$V_{IH}2$	$\overline{\text{RESET}}$, I_O0 to I_O7, D0 to D7, $\overline{\text{RD}}$, $\overline{\text{CS}}$, $\overline{\text{WR}}$, WFCK, SBSO and SCOR(1)	2.5			V
Input low level voltage	$V_{IL}2$				0.6	V
Input high level voltage	$V_{IH}3$	$\overline{\text{ACK}}$, $\overline{\text{ATN}}$ and the input pins (3)	2.0			V
Input low level voltage	$V_{IL}3$				0.8	V
Output high level voltage	$V_{OH}1$	$I_{OH}1$ = –3 mA: I_O0 to I_O7, D0 to D7 and all output pins other than (2), (3) and XTALCK	2.4			V
Output low level voltage	$V_{OL}1$	$I_{OL}1$ = 3 mA: I_O0 to I_O7, D0 to D7 and all output pins other than (2), (3) and XTALCK			0.4	V
Output low level voltage	$V_{OL}2$	$I_{OL}2$ = 3 mA: $\overline{\text{INT1}}$ and $\overline{\text{INT0}}$ (pull-up resistor open drain) (2)			0.4	V
Output low level voltage	$V_{OL}3$	$I_{OL}3$ = 48 mA: $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBP}}$, $\overline{\text{BSY}}$, I/O, $\overline{\text{MSG}}$, $\overline{\text{SEL}}$, $\overline{\text{RST}}$, $\overline{\text{REQ}}$, C/D (2)			0.4	V
Input leakage current	I_L	V_I = V_{SS}, V_{DD}: All input pins	–25		+25	µA
Pull-up resistance	R_{UP}	I_O0 to I_O7, D0 to D7, $\overline{\text{INT1}}$ and $\overline{\text{INT0}}$	40	80	160	kΩ