CMOS LSI

# LC895126

## CD-ROM Decoder with Built-in SCSI Interface

**Preliminary**

## Overview

The LC895126 is a CD-ROM decoder that in addition to CD-ROM functions also provides a built-in SCSI interface.

## Functions

• CD-ROM ECC functions, subcode read function, SCSI interface, CAV audio functions

## Features

• Built-in SCSI interface (Includes a SCAM selection register)
• Supports 24× playback and a 10MB/sec data transfer rate (when 16-bit data path 70-ns EDO DRAM is used).
• Supports the use of up to 4 Mbit of buffer RAM.
• Users can freely set up the CD main channel, C2 flag, and other areas in buffer RAM.
• Batch transfer function (Function that transfers the CD main channel, C2 flag, and other data in a single operation)
• Multiblock transfer function (Function that transfers multiple blocks automatically in a single operation)
• Subcode ECC functions and CD-Text support
• CAV audio functions
• Intelligent functions (Including auto buffering, auto decoding, and CD-R support)

• Supports 20MB/s transfers (This capability is currently under evaluation (July 1997) and cannot be guaranteed at present.)

## Package Dimensions

unit: mm

**3214-SQFP144**



SANYO: SQFP144
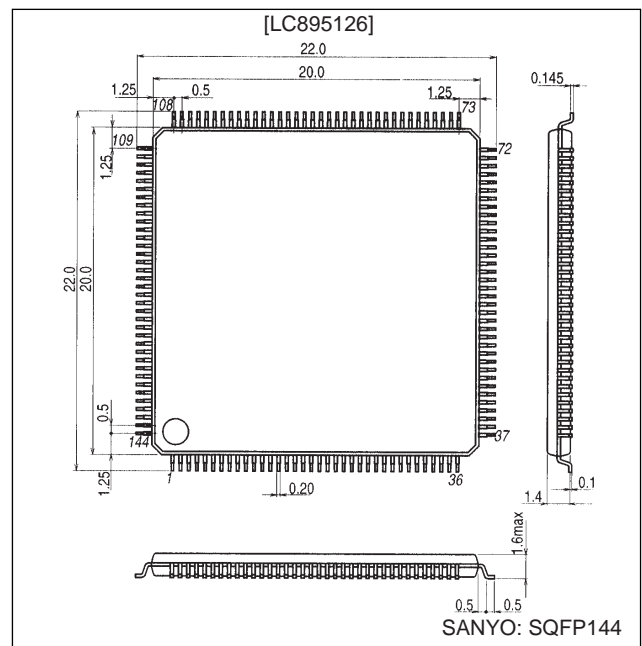
## Specifications

### Absolute Maximum Ratings at $Ta = 25°C$, $V_{SS} = 0$ V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | | −0.3 to +7.0 | V |
| Input and output voltage | $V_I$, $V_O$ | | −0.3 to $V_{DD}$ +0.3 | V |
| Allowable power dissipation | Pd max | $Ta \leq 70°C$ | 550 | mW |
| Operating temperature | Topr | | −30 to +70 | °C |
| Storage temperature | Tstg | | −55 to +125 | °C |
| Soldering conditions (pins only) | | 10 seconds | 260 | °C |

### Allowable Operating Ranges at $Ta = -30$ to $+70°C$, $V_{SS} = 0$ V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply voltage | $V_{DD}$ | | 4.5 | 5.0 | 5.5 | V |
| Input voltage range | $V_{IN}$ | | 0 | | $V_{DD}$ | V |

# LC895126

## Electrical Characteristics at Ta = –30 to +70°C, $V_{SS}$ = 0 V, $V_{DD}$ = 4.5 to 5.5 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Input high-level voltage | $V_{IH}1$ | TTL level pins: (1) | 2.2 | | | V |
| Input low-level voltage | $V_{IL}1$ | | | | 0.8 | V |
| Input high-level voltage | $V_{IH}2$ | TTL level pins: (9) | 2.2 | | | V |
| Input low-level voltage | $V_{IL}2$ | Pins with built-in pull-up resistors. | | | 0.8 | V |
| Input high-level voltage | $V_{IH}3$ | TTL level pins: (2) | 2.2 | | | V |
| Input low-level voltage | $V_{IL}3$ | Schmitt input pins | | | 0.8 | V |
| Input high-level voltage | $V_{IH}4$ | CMOS level pins: (3) | $0.8\ V_{DD}$ | | | V |
| Input low-level voltage | $V_{IL}4$ | Schmitt input pins | | | $0.2\ V_{DD}$ | V |
| Input high-level voltage | $V_{IH}5$ | (4), (8), (10) | 2.0 | | | V |
| Input low-level voltage | $V_{IL}5$ | | | | 0.8 | V |
| Output high-level voltage | $V_{OH}1$ | $I_{OH}1 = -12$ mA : (6) | $V_{DD} - 2.1$ | | | V |
| Output low-level voltage | $V_{OL}1$ | $I_{OL}1 = 12$ mA : (6) | | | 0.4 | V |
| Output high-level voltage | $V_{OH}2$ | $I_{OH}2 = -8$ mA : (7) | 2.4 | | | V |
| Output low-level voltage | $V_{OL}2$ | $I_{OL}2 = 8$ mA : (7) | | | 0.4 | V |
| Output high-level voltage | $V_{OH}2$ | $I_{OH}2 = -2$ mA : (9), (5) | 2.4 | | | V |
| Output low-level voltage | $V_{OL}2$ | $I_{OL}2 = 2$ mA : (9), (5) | | | 0.4 | V |
| Output low-level voltage | $V_{OL}4$ | $I_{OL}4 = 48$ mA : (10) | | | 0.4 | V |
| Input leakage current | $I_{IL}$ | $V_I = V_{SS}$ or $V_{DD}$: All input pins. | –25 | | +25 | µA |
| Pull-up resistance | $R_{UP}$ | (5), (9) | 60 | 120 | 240 | kΩ |

The pin sets referred to above are as follows:
INPUT
(1)    TEST0 to TEST4, CSCTRL, SUA0 to SUA6, X1EN, WFCK, SBS0
(2)    C2PO, SDATA, BCK, LRCK, SCOR, ZRESET
(3)    ZCS, ZRD, ZWR
(4)    SCSISEL, XTALSEL
OUTPUT
(5)    ZINT0, ZINT1, ZSWAIT
(6)    MCK, MCK2, MCK3
(7)    EXCK, DSDATA, DLRCK, DBCK, ZRAS0, ZRAS1, ZCAS0, ZCAS1, ZOE, ZUWE, ZLWE, RA0 to RA8
INOUT
(8)    ACK̄, ATN̄
(9)    D0 to D7, IO0 to IO15, IOP0 to IOP4
(10)   DB0 to DB7, DBP, BSY, I/O, MSG, SEL, RST, REQ, C/D
Note: The XTAL0, XTALCK0, XTAL1, and XTALCK1 pins are not covered by the electrical characteristics.

## SCSI Interface Pin Input Characteristics

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Input threshold voltage | $V_{t+t1}$ | $V_{DD}$ = 4.50 to 5.50 V | | 1.60 | 2.00 | V |
| | $V_{t-t1}$ | | 0.80 | 1.10 | | V |
| Hysteresis | $\Delta V_{tt1}$ | $V_{DD}$ = 5.0 V | 0.41 | 0.5 | | V |

## Active Negation Output Characteristics

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Output high-level voltage | $V_{OH}$ | $I_{OH} = -24$ mA | 2.5 | | | V |
| Output low-level voltage | $V_{OL}$ | $I_{OL} = 48$ mA | | | 0.4 | V |

Note: Active negation refers to the D̄B̄0̄ to D̄B̄7̄, R̄ĒQ̄, and D̄B̄P̄B̄ outputs.
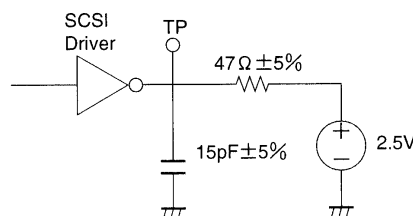


**Figure 1**

## LC895126

### Pin Functions

| Pin No. | Symbol | Type | Function |
|---------|--------|------|----------|
| 1 | $V_{SS0}$ | P | |
| 2 | IO2 | B | Buffer RAM data I/O pins. |
| 3 | IO1 | B | |
| 4 | IO0 | B | Built in pull-up resistors. |
| 5 | MCK2SEL | I | Provided for switching between MCK2 (22 MHz, 20 MHz) and MCK3 (27 MHz, 25 MHz) in PLL mode.<br>Currently, must be connected to $V_{DD}$. |
| 6 | | NC | |
| 7 | $V_{SS0}$ | P | |
| 8 | $V_{SS0}$ | P | |
| 9 | $V_{SS0}$ | P | |
| 10 | | NC | |
| 11 | | NC | |
| 12 | C2PO | I | CD DSP interface |
| 13 | SDATA | I | |
| 14 | BCK | I | |
| 15 | LRCK | I | |
| 16 | EXCK | O | Subcode I/O |
| 17 | WFCK | I | |
| 18 | $V_{DD}$ | P | |
| 19 | $V_{SS0}$ | P | |
| 20 | SBSO | I | Subcode I/O |
| 21 | SCOR | I | |
| 22 | DSDATA | O | D/A converter outputs |
| 23 | DLRCK | O | |
| 24 | DBCK | O | |
| 25 | MCK | O | Outputs the XTALCK1 state (1/1, 1/2, or stopped) |
| 26 | $V_{SS0}$ | P | |
| 27 | XTALCK0 | I | Crystal oscillator circuit input |
| 28 | XTAL0 | O | Crystal oscillator circuit input |
| 29 | TEST0 | I | |
| 30 | TEST1 | I | |
| 31 | TEST2 | I | Test pins. These pins must be connected to $V_{SS0}$. |
| 32 | TEST3 | I | |
| 33 | TEST4 | I | |
| 34 | MCK2 | O | Outputs the XTALCK0 state (1/1, 1/2, 1/512, or stopped) |
| 35 | MCK3 | O | |
| 36 | $V_{SS0}$ | P | |
| 37 | $V_{DD}$ | P | |
| 38 | ZRESET | I | Chip reset. The system is reset by a low-level input. |
| 39 | ZRD | I | Microcontroller data read signal input |
| 40 | ZWR | I | Microcontroller data write signal input |

Continued from preceding page.

| Pin No. | Symbol | Type | Function |
|---|---|---|---|
| 41 | ZCS | I | Register chip select signal input from the microcontroller |
| 42 | CSCTRL | I | CS active low/active high selection input from the microcontroller |
| 43 | SUA0 | I | Microcontroller register selection signals |
| 44 | SUA1 | I | |
| 45 | SUA2 | I | |
| 46 | SUA3 | I | |
| 47 | SUA4 | I | |
| 48 | SUA5 | I | |
| 49 | SUA6 | I | |
| 50 | D0 | B | Microcontroller data signals |
| 51 | D1 | B | |
| 52 | D2 | B | |
| 53 | D3 | B | |
| 54 | $V_{DD}$ | P | |
| 55 | $V_{SS0}$ | P | |
| 56 | D4 | B | |
| 57 | D5 | B | |
| 58 | D6 | B | |
| 59 | D7 | B | |
| 60 | ZINT0 | O | Interrupt request signal output to the microcontroller (ECC side. Set up by register settings.) |
| 61 | ZINT1 | O | Interrupt request signal output to the microcontroller (SCSI side. Set up by register settings.) |
| 62 | ZSWAIT | O | Wait signal output to the microcontroller |
| 63 | $V_{SS0}$ | P | |
| 64 | IOP0 | B | General-purpose I/O |
| 65 | IOP1 | B | |
| 66 | IOP2 | B | |
| 67 | IOP3 | B | |
| 68 | IOP4 | B | |
| 69 | X1EN | I | Must be tied low in versions without a PLL circuit. Must be connected to $V_{DD}$ through a resistor in versions that use the PLL circuit. |
| 70 | ZTALCK1 | I | Shock proof function oscillator circuit input. Used by the PLL circuit in PLL versions. |
| 71 | XTAL1 | O | Shock proof function oscillator circuit output. Used by the PLL circuit in PLL versions. |
| 72 | $V_{SS0}$ | P | Analog system ground in PLL versions |
| 73 | $V_{DD}$ | P | Analog system power supply in PLL versions |
| 74 | $V_{SS1}$ | P | |
| 75 | I/O | B | SCSI interface connections |
| 76 | $\overline{REQ}$ | B | |
| 77 | $V_{SS1}$ | P | |
| 78 | C/D | B | SCSI interface connections |
| 79 | $\overline{SEL}$ | B | |
| 80 | | NC | |
| 81 | $V_{DD}$ | P | |
| 82 | $V_{SS1}$ | P | |
| 83 | $\overline{MSG}$ | B | SCSI interface connections |
| 84 | $\overline{RST}$ | B | |
| 85 | $V_{SS1}$ | P | |
| 86 | $\overline{ACK}$ | B | SCSI interface connections |
| 87 | $\overline{BSY}$ | B | |
| 88 | $V_{SS1}$ | P | |

Continued from preceding page.

| Pin No. | Symbol | Type | Function |
|---|---|---|---|
| 89 | $\overline{ATN}$ | B | SCSI interface connections |
| 90 | $V_{DD}$ | P | |
| 91 | $V_{SS1}$ | P | |
| 92 | | NC | |
| 93 | $\overline{DBP}$ | B | SCSI interface connections |
| 94 | $V_{DD}$ | P | |
| 95 | $\overline{DB7}$ | B | SCSI interface connections |
| 96 | $\overline{DB6}$ | B | |
| 97 | $V_{SS1}$ | P | |
| 98 | $\overline{DB5}$ | B | SCSI interface connections |
| 99 | $\overline{DB4}$ | B | |
| 100 | $V_{DD}$ | P | |
| 101 | $\overline{DB3}$ | B | SCSI interface connections |
| 102 | $\overline{DB2}$ | B | |
| 103 | $V_{SS1}$ | P | |
| 104 | $\overline{DB1}$ | B | SCSI interface connections |
| 105 | $\overline{DB0}$ | B | |
| 106 | SCSISEL | I | SCSI pin assignment selection (No change when held low.) |
| 107 | XTALSEL | I | XATL oscillator selection in PLL mode |
| 108 | $V_{SS1}$ | P | |
| 109 | $V_{DD}$ | P | |
| 110 | $V_{SS0}$ | P | |
| 111 | ZRAS0 | O | RAS output 0 for buffer RAM (Normally, RAS 0 is used.) |
| 112 | ZRAS1 | O | RAS output 1 for buffer RAM |
| 113 | ZCAS0 | O | CAS output 0 for buffer RAM (Normally, CAS 0 is used.) |
| 114 | ZCAS1 | O | CAS output 1 for buffer RAM |
| 115 | ZOE | O | Buffer RAM output enable |
| 116 | ZUWE | O | Buffer RAM upper write enable |
| 117 | ZLWE | O | Buffer RAM lower write enable |
| 118 | $V_{SS0}$ | P | |
| 119 | RA0 | O | Buffer RAM address outputs |
| 120 | RA1 | O | |
| 121 | RA2 | O | |
| 122 | RA3 | O | |
| 123 | RA4 | O | |
| 124 | RA5 | O | |
| 125 | RA6 | O | |
| 126 | $V_{DD}$ | P | |
| 127 | $V_{SS0}$ | P | |
| 128 | RA7 | O | Buffer RAM address outputs |
| 129 | RA8 | O | |
| 130 | RA9 (IO15) | B | Buffer RAM address and data outputs. |
| 131 | RA10 (IO14) | B | Built in pull-up resistors. |

Continued from preceding page.

| Pin No. | Symbol | Type | Function |
|---------|--------|------|----------|
| 132 | IO13 | B | |
| 133 | IO12 | B | |
| 134 | IO11 | B | Buffer RAM data I/O. |
| 135 | IO10 | B | Built in pull-up resistors. |
| 136 | IO9 | B | |
| 137 | IO8 | B | |
| 138 | $V_{SS0}$ | P | |
| 139 | IO7 | B | |
| 140 | IO6 | B | |
| 141 | IO5 | B | Buffer RAM data I/O. |
| 142 | IO4 | B | Built in pull-up resistors. |
| 143 | IO3 | B | |
| 144 | $V_{DD}$ | P | |

NC pins must be left open.

Pin names that start with a 'Z' are negative logic (i.e. active low) pins.

$V_{SS0}$ is the logic system ground, and $V_{SS1}$ is the SCSI interface system ground.

If DRAM is used, undershoot prevention measures, such as inserting resistors in the RAS and CAS lines and inserting capacitors to ground, must be taken.

Since this IC includes buffers that sink 48 mA, applications must take adequate noise reduction measures.

## Block Diagram



A09480
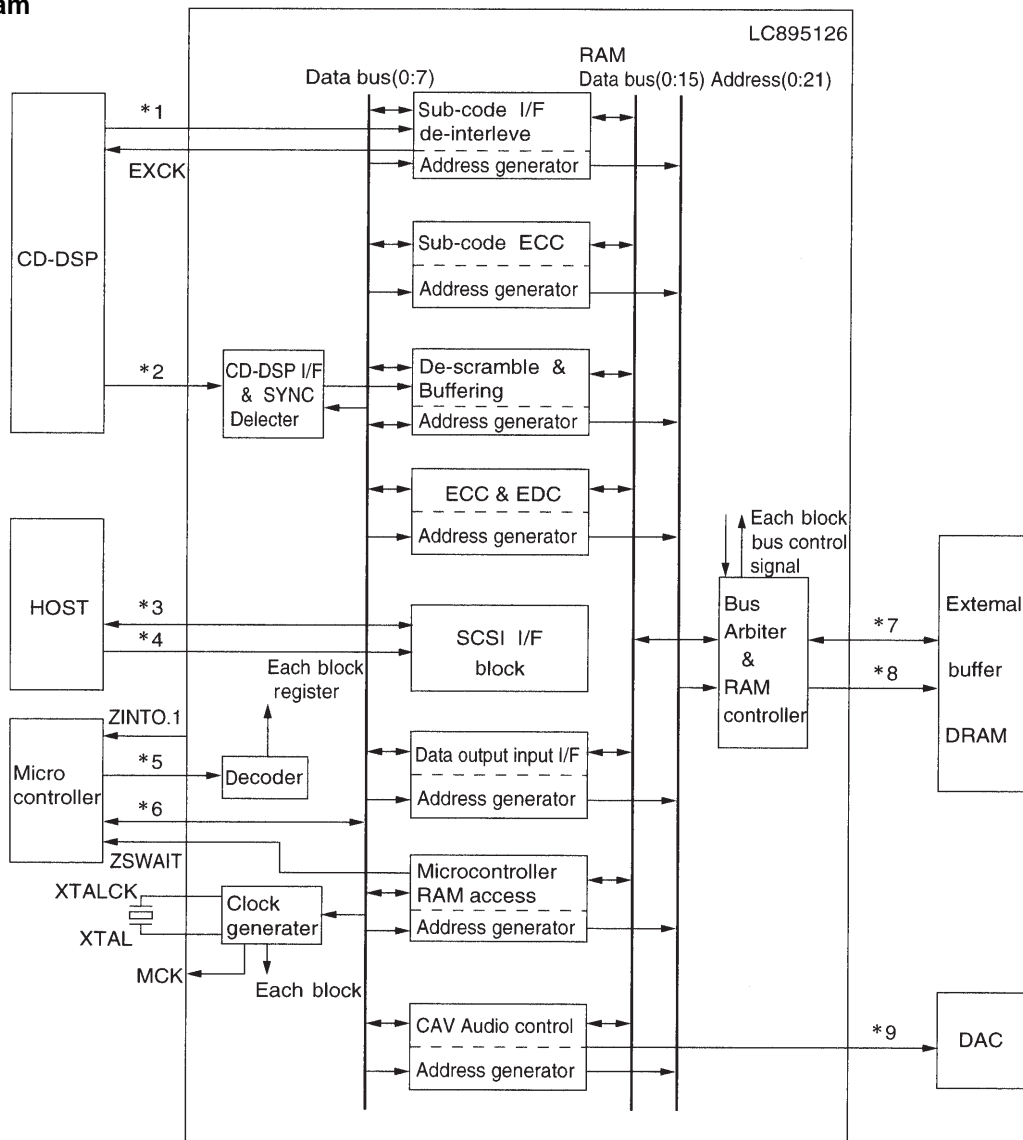
*1　WFCK, SBSO, SCOR
*2　BCK, SDATA, LRCK, C2PO
*3　DB0 to DB7, DBP, BSY, MSG, SEL, RST, REQ, I/O, C/D
*4　ACK, ATN
*5　ZRD, ZWR, SUA0 to AUA6, ZCS, CSCTRL
*6　D0 to D7
*7　IO0 to IO15
*8　RA0 to RA10, ZRAS0, ZRAS1, ZCAS0, ZCAS1, ZOE, ZUWE, ZLWE
*9　DBCK, DLRCK, DSDATA
Note: The pins IO15 and RA9 share pin 130, and the pins IO14 and RA10 share pin 131.

This catalog provides information as of January, 1998. Specifications and information herein are subject to change without notice.