Ordering number : ENA1954A

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LC88F85D0A — CMOS IC FROM 256K byte, RAM 8K byte on-chip 16-bit 1-chip Microcontroller

Overview

The LC88F85D0A is a 16-bit microcomputer that, centered around an Xstormy16 CPU core, integrates on a single chip a number of hardware features such as 256K bytes of flash ROM (onboard programmable), 8K bytes of RAM, five 16-bit timers, a time base timer, a synchronous SIO interface with automatic transfer function, a single-master I^2C/synchronous SIO interface, two asynchronous SIO (UART) interfaces, a remote control receiver, LCD dedicated RAM, an LCD dot-matrix driver, a 12-bit-resolution 8-channel AD converter, a watchdog timer, a system clock frequency divider, and a 35-source 10-vector interrupt feature.

Features

■Xstromy16 CPU
- 4G-byte address space
- General-purpose registers: 16 bits × 16

■Flash ROM
- Onboard programmable with a wide range of supply voltages: 3.0 to 5.5V
- Block erasable in 512-byte/1K-byte units
- Data writing in 2-byte units
- 262144 × 8 bits

■RAM
- Data: 8192 × 8 bits
- LCD display: 128 × 16 bits

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

■Minimum instruction cycle time (tCYC)
- 100ns (10MHz) V_{DD} = 4.5 to 5.5V
- 125ns (8MHz) V_{DD} = 3.0 to 5.5V
- 500ns (2MHz) V_{DD} = 2.0 to 5.5V

■Ports
- Normal withstand voltage I/O ports
  Ports whose I/O direction specifiable in 1-bit units: 20 (P0n, P1n, P20 to P23)
- LCD (Pins COM16/SEG0 to COM31/SEG15 are multiplexed with COM and SEG.)
  LCD driver bias power supply pins 4 ($V_{LCD}1$ to $V_{LCD}4$)
  Step-up capacitor pins 2 (CUP00, CUP01)
  16 common mode
  Segment output 64 (SEG0 to SEG63)
  Common output 16 (COM0 to COM15)
  32 common mode
  Segment output 48 (SEG16 to SEG63)
  Common output 32 (COM0 to COM31)
- Oscillation dedicated ports 4 (XT1, XT2, CF1, CF2)
- Reset pin 1 (RESB)
- TEST pin 1 (TEST)
- LCD port power pins 2 ($LCDV_{SS}0$, $LCDV_{SS}1$)
- Power pins 2 (V_{DD}, V_{SS})

■LCD
- LCD power supply : Capacitor step-up type
- Number of dots : 1024 (64 segments × 16 commons) / 1536 (48 segments × 32 commons)
- Contrast : Selectable from 16 levels
- LCD frame frequency : Selectable from 4 frequencies

■Timers
- Timer 0: 16-bit timer that supports PWM/toggle outputs
  <1> With 5-bit prescaler
  <2> 8-bit PWM × 2 / 8-bit timer + 8-bit PWM split mode selectable
  <3> Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 1: 16-bit timer with a capture register
  <1> With 5-bit prescaler
  <2> Can be divided into 8-bit timer × 2 channels
  <3> Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 3: 16-bit timer that supports PWM/toggle outputs
  <1> With 8-bit prescaler
  <2> 8-bit timer × 2 channels / 8-bit timer + 8-bit PWM split mode selectable
  <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 4: 16-bit timer that supports toggle output
  <1> Clock source selectable from system clock and prescaler 0
- Timer 5: 16-bit timer that supports toggle output
  <1> Clock source selectable from system clock and prescaler 0
  * The prescaler 0 consists of 4 bits and its clock source is selectable from the system clock, OSC0, and OSC1.
- Base timer
  <1> The clock can be selected from OSC0 (32.768kHz crystal oscillator) and the frequency-divided output of the system clock.
  <2> Interrupts can be generated in 7 time schemes.

■Realtime clock (RTC)
  <1> Calendar function from January 1, 2000 to December 31, 2799 (with automatic leap year compensation)
  <2> Independent counter configuration for century, year, month, day, hour, minute, and second
  <3> Programmable count clock correction function

■Serial interfaces

- SIO0: 8-bit synchronous SIO
  <1> LSB first/MSB first selectable
  <2> Supports communication of less than 8 bits (1 to 8 bits specifiable).
  <3> Built-in 8-bit baudrate generator (transfer clock cycles of 4 tCYC to 512 tCYC)
  <4> Automatic continuous data transfer (9 to 32768 bits specifiable in 1-bit units)
  <5> Interval function (interval time specifiable in 0 to 64 tSCK units)
  <6> Wakeup function
- SMIIC0: Single-master I^2C/8-bit synchronous SIO
  Mode 0: Single-master master mode communication
  Mode 1: 8-bit synchronous serial I/O (MSB first)
- UART0
  <1> Data length: 8 bits (LSB first)
  <2> Start bits: 1 bit
  <3> Stop bits: 1 bit
  <4> Parity bits: None/even parity/odd parity
  <5> Transfer rate: 4/8 tCYC
  <6> Baudrate clock source: The P07 input signal is used as a 1 cycle signal (T0PWMH can be used as the clock source) or a timer 4 period.
  <7> Full duplex communication
- UART2
  <1> Data length: 8 bits (LSB first)
  <2> Start bits: 1 bit
  <3> Stop bits: 1/2 bit
  <4> Parity bit: None/even parity/odd parity
  <5> Transfer rate: 8 to 4096 tCYC
  <6> Baudrate clock source: System clock/OSC0/OSC1/P21 input signal
  <7> Wakeup function
  <8> Full duplex communication

■AD converter

<1> 8/12-bit resolution selectable
<2> Analog inputs: 12 channels
<3> Comparator mode
<4> Automatic reference voltage generation

■Watchdog timer

<1> Runs on the base timer + internal watchdog timer dedicated counter.
<2> Interrupt or reset signals selectable

■Infrared remote control receiver

<1> Noise rejection function
(Noise filter time constant: Approx. 120μs when the 32.768kHz crystal oscillator is selected as the reference clock source)
<2> Supports PPM (Pulse Position Modulation), Manchester and other encoding systems.
<3> HOLDX mode release function

■Interrupts (peripheral function)

Either "Normal" or "LC888300 Compatible" mode is selectable by user option.
* Note: The "LC888300 Compatible" mode is an option that is available to provide compatibility between this model and the LC888300. It is to be unavailable in future developed models.

<1> Provides three levels of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.
<2> When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

• Normal mode: 35 sources (15 modules), 10 vectors

No.	Vector	Interrupt Module
1	08000H	Watchdog timer (1)
2	08004H	Base timer (2)
3	08008H	Timer 0 (2)
4	08018H	Timer 1 (2)/UART2 (4)
5	0801CH	SMIIC0 (1)
6	08020H	Timer 3 (2)/infrared remote control receiver (4)
7	08024H	Timer 4 (1)
8	08030H	ADC (1)/timer 5 (1)
9	08038H	SIO0 (2)
10	0803CH	Port 0 (3)/RTC2 (1)/SEGINT (8)

• LC888300 Compatible mode: 35 sources (15 modules), 13 vectors

No.	Vector	Interrupt Module
1	08000H	Watchdog timer (1)
2	08004H	Base timer (2)
3	08008H	Timer 0 (2)
4	08018H	SIO0 (2)
5	0801CH	Timer 1 (2)
6	08020H	UART2 (4)
7	08024H	Timer 3 (2)
8	08028H	Timer 4 (1)
9	0802CH	Timer 5 (1)
10	08030H	ADC (1)
11	08034H	SMIIC0 (1)
12	08038H	Infrared remote control receiver (4)
13	0803CH	Port 0 (3)/RTC2 (1)/SEGINT (8)

• Priority levels X > H > L
• When interrupts of the same level occur at the same time, an interrupt with a smaller vector address is given priority.
• The number in parentheses indicates the number of sources in a module.

■Subroutine stack: 8K-byte RAM area
• Subroutine calls that automatically save the PSW, interrupt vector call: 6 bytes
• Subroutine calls that do not automatically save the PSW: 4 bytes

■Multiplication/division instructions
• 16 bits × 16 bits (18 tCYC execution time)
• 16 bits ÷ 16 bits (18 to 19 tCYC execution time)
• 32 bits ÷ 16 bits (18 to 19 tCYC execution time)

■Oscillator circuits
• RC oscillator circuit (internal): For system clock
• CF oscillator circuit: For system clock (OSC1)
• RC oscillator circuit (external R_{CR1}): For system clock (OSC1)
• Crystal oscillator circuit (Rf built-in): For low-speed system clock (OSC0) (option available)
• RC oscillator circuit (external R_{CR0}): For low-speed system clock (OSC0)
• SLRC oscillator circuit (internal): For system clock (used during exception processing)

■System clock frequency divider function
• Can run on low consumption current.
• Supports frequency-dividing of 1/1 to 1/128 of the system clock

■Standby function
• HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
1) Oscillation is not halted automatically.
2) HALT mode is released by a system reset or an interrupt .

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- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) OSC1, RC, and OSC0 oscillations automatically stop.
  2) There are five ways of releasing the HOLD mode:
     <1> Setting the reset pin to the low level
     <2> Having an interrupt source established at port 0
     <3> Having an interrupt source established at SIO0
     <4> Having an interrupt source established at UART2
     <5> Having an interrupt source established at SEGINT
- HOLDX mode: Suspends instruction execution and the operation of all the circuits except the peripheral circuits running on OSC0.
  1) OSC1 and RC oscillators automatically stop operation.
  2) OSC0 retains the state established when the HOLDX mode is entered.
  3) There are seven ways of releasing the HOLDX mode:
     <1> Setting the reset pin to the low level
     <2> Having an interrupt source established at port 0
     <3> Having an interrupt source established at SIO0
     <4> Having an interrupt source established at UART2
     <5> Having an interrupt source established at SEGINT
     <6> Having an interrupt source established in the base timer or RTC2 circuit
     <7> Having an interrupt source established in the infrared remote control receiver circuit

■On-chip debugger function
- Supports software debugging with the microcontroller mounted on the target board.
- Supports source line debugging, tracing, breakpoint manipulation, and realtime display.
- Single-wire communication

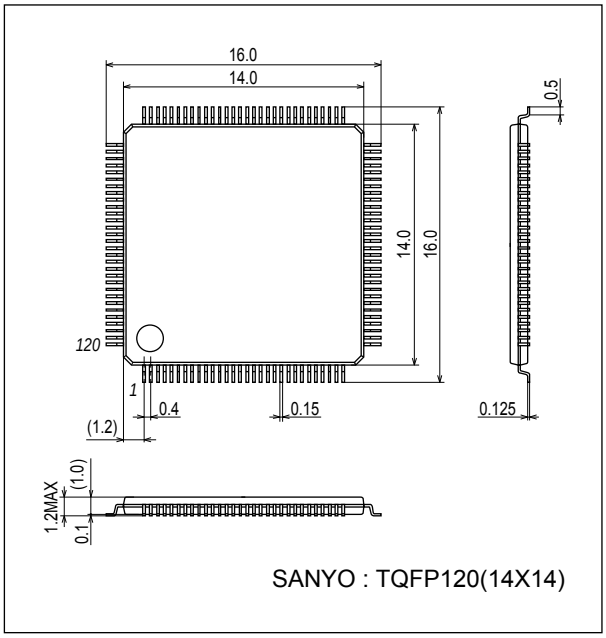
■Operating temperature
- -20 to +75°C

■Package form
- TQFP120 (14×14) (lead-free type)

■Development tools
- On-chip debugger: EOCUIF1 + LC88F85D0A

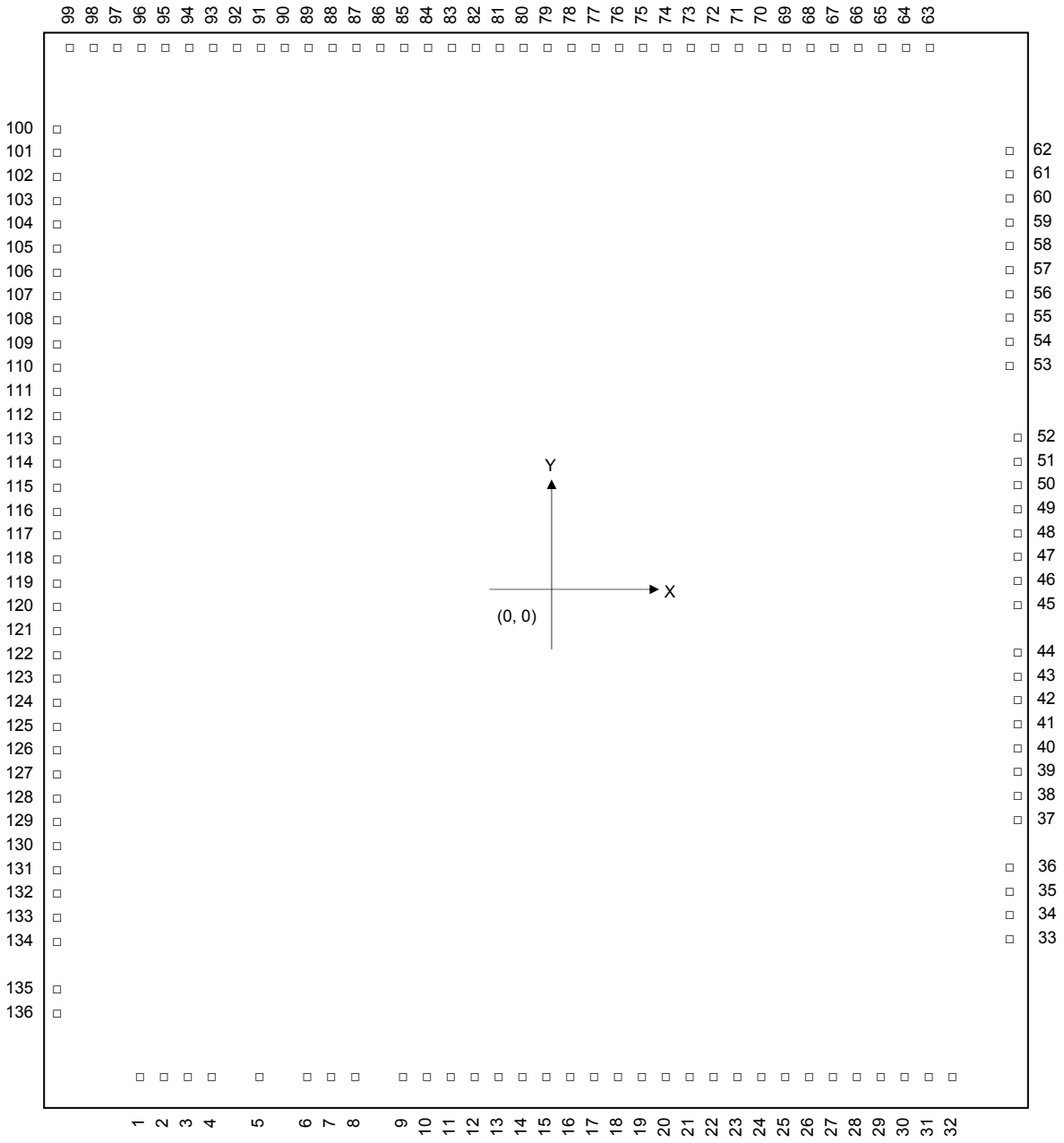
Package Dimensions

unit : mm (typ)
3257A



Pad Assignment

- Chip size (X × Y) : 4.10mm × 3.40mm
- PAD opening siz : 59μm
- PAD pitch : 80μm
- Chip thickness : 280μm ± 20μm



- Note: Package pin numbers differ from chip pad numbers. The numbers shown in the above figure are pad numbers.

Table of PAD Coordinates

Pad No.	Pin Name	Coordinate		Pad No.	Pin Name	Coordinate	
		X μm	Y μm			X μm	Y μm
1	$V_{LCD}4$	-1647.9	-1569.9	48	SEG52	1958.5	208.2
2	$V_{LCD}3$	-1567.9	-1569.9	49	SEG51	1958.5	298.2
3	$V_{LCD}2$	-1483.2	-1569.9	50	SEG50	1958.5	388.2
4	$V_{LCD}1$	-1403.2	-1569.9	51	SEG49	1958.5	478.2
5	TST	-1184.0	-1569.9	52	SEG48	1958.5	568.2
6	XT2	-890.0	-1569.9	53	SEG47	1919.9	710.0
7	XT1	-781.5	-1569.9	54	SEG46	1919.9	790.0
8	RESB	-670.0	-1569.9	55	SEG45	1919.9	870.0
9	V_{DD}	-494.5	-1569.9	56	SEG44	1919.9	950.0
10		-374.5	-1569.9	57	SEG43	1919.9	1030.0
11		-263.5	-1569.9	58	SEG42	1919.9	1110.0
12	CF1	-165.0	-1569.9	59	SEG41	1919.9	1190.0
13	CF2	-85.0	-1569.9	60	SEG40	1919.9	1280.0
14	V_{SS}	10.0	-1569.9	61	SEG39	1919.9	1370.0
15		110.0	-1569.9	62	SEG38	1919.9	1460.0
16		210.0	-1569.9	63	$LCDV_{SS}1$	1420.0	1569.9
17	P00	300.0	-1569.9	64	SEG37	1300.0	1569.9
18	P01	380.0	-1569.9	65	SEG36	1190.0	1569.9
19	P02	460.0	-1569.9	66	SEG35	1080.0	1569.9
20	P03	540.0	-1569.9	67	SEG34	990.0	1569.9
21	P04	620.0	-1569.9	68	SEG33	910.0	1569.9
22	P05	700.0	-1569.9	69	SEG32	830.0	1569.9
23	P06	780.0	-1569.9	70	SEG31	750.0	1569.9
24	P07	860.0	-1569.9	71	SEG30	670.0	1569.9
25	P10	940.0	-1569.9	72	SEG29	590.0	1569.9
26	P11	1020.0	-1569.9	73	SEG28	510.0	1569.9
27	P12	1100.0	-1569.9	74	SEG27	430.0	1569.9
28	P13	1180.0	-1569.9	75	SEG26	350.0	1569.9
29	P14	1260.0	-1569.9	76	SEG25	270.0	1569.9
30	P15	1340.0	-1569.9	77	SEG24	190.0	1569.9
31	P16	1420.0	-1569.9	78	SEG23	110.0	1569.9
32	P17	1500.0	-1569.9	79	SEG22	30.0	1569.9
33	P20	1919.9	-1415.0	80	SEG21	-50.0	1569.9
34	P21	1919.9	-1325.0	81	SEG20	-130.0	1569.9
35	P22	1919.9	-1192.0	82	SEG19	-210.0	1569.9
36	P23	1919.9	-1057.0	83	SEG18	-290.0	1569.9
37	SEG63	1958.5	-871.8	84	SEG17	-370.0	1569.9
38	SEG62	1958.5	-781.8	85	SEG16	-450.0	1569.9
39	SEG61	1958.5	-691.8	86	-	-	-
40	SEG60	1958.5	-601.8	87	COM31/SEG15	-620.0	1569.9
41	SEG59	1958.5	-511.8	88	-	-	-
42	SEG58	1958.5	-421.8	89	COM30/SEG14	-780.0	1569.9
43	SEG57	1958.5	-331.8	90	-	-	-
44	SEG56	1958.5	-241.8	91	COM29/SEG13	-940.0	1569.9
45	SEG55	1958.5	-61.8	92	-	-	-
46	SEG54	1958.5	28.2	93	COM28/SEG12	-1100.0	1569.9
47	SEG53	1958.5	118.2	94	-	-	-

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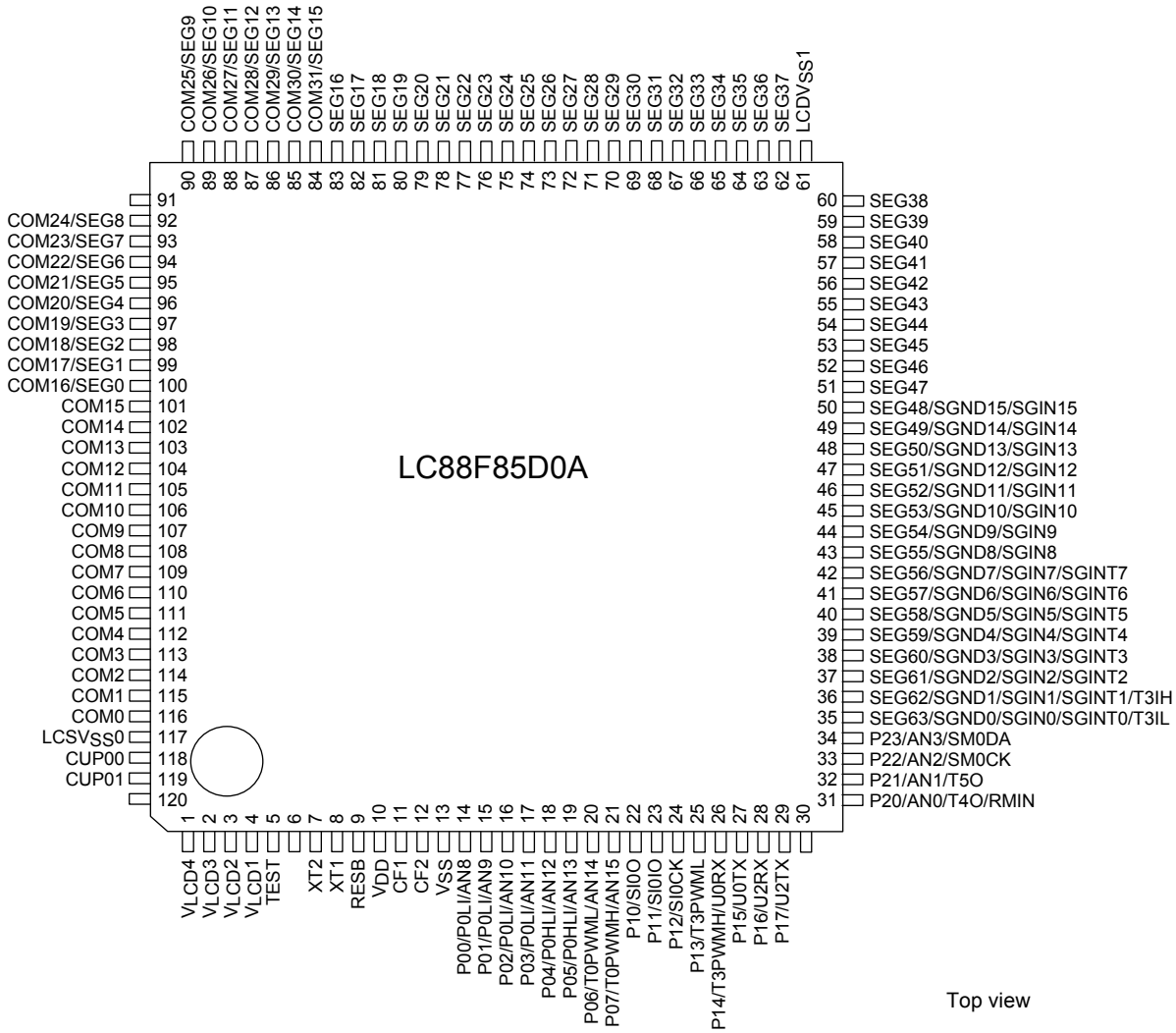
Pad No.	Pin Name	Coordinate		Pad No.	Pin Name	Coordinate	
		X μm	Y μm			X μm	Y μm
95	COM27/SEG11	-1260.0	1569.9	116	-	-	-
96	-	-	-	117	COM16/SEG0	-1919.9	60.0
97	COM26/SEG10	-1420.0	1569.9	118	COM15	-1919.9	-20.0
98	-	-	-	119	COM14	-1919.9	-100.0
99	COM25/SEG9	-1580.0	1569.9	120	COM13	-1919.9	-180.0
100	-	-	-	121	COM12	-1919.9	-260.0
101	COM24/SEG8	-1919.9	1340.0	122	COM11	-1919.9	-340.0
102	-	-	-	123	COM10	-1919.9	-420.0
103	COM23/SEG7	-1919.9	1180.0	124	COM9	-1919.9	-500.0
104	-	-	-	125	COM8	-1919.9	-580.0
105	COM22/SEG6	-1919.9	1020.0	126	COM7	-1919.9	-660.0
106	-	-	-	127	COM6	-1919.9	-740.0
107	COM21/SEG5	-1919.9	860.0	128	COM5	-1919.9	-820.0
108	-	-	-	129	COM4	-1919.9	-900.0
109	COM20/SEG4	-1919.9	700.0	130	COM3	-1919.9	-980.0
110	-	-	-	131	COM2	-1919.9	-1060.0
111	COM19/SEG3	-1919.9	540.0	132	COM1	-1919.9	-1140.0
112	-	-	-	133	COM0	-1919.9	-1220.0
113	COM18/SEG2	-1919.9	380.0	134	$LCSV_{SS}0$	-1919.9	-1320.0
114	-	-	-	135	CUP00	-1919.9	-1443.3
115	COM17/SEG1	-1919.9	220.0	136	CUP01	-1919.9	-1523.3

Note:

- The coordinate values shown in the above table represent the coordinates of the pin pads measured with the center coordinates of the IC set to (0, 0).
- There are three pads for each of the V_{DD} and V_{SS} pins. They should be triple bonded.

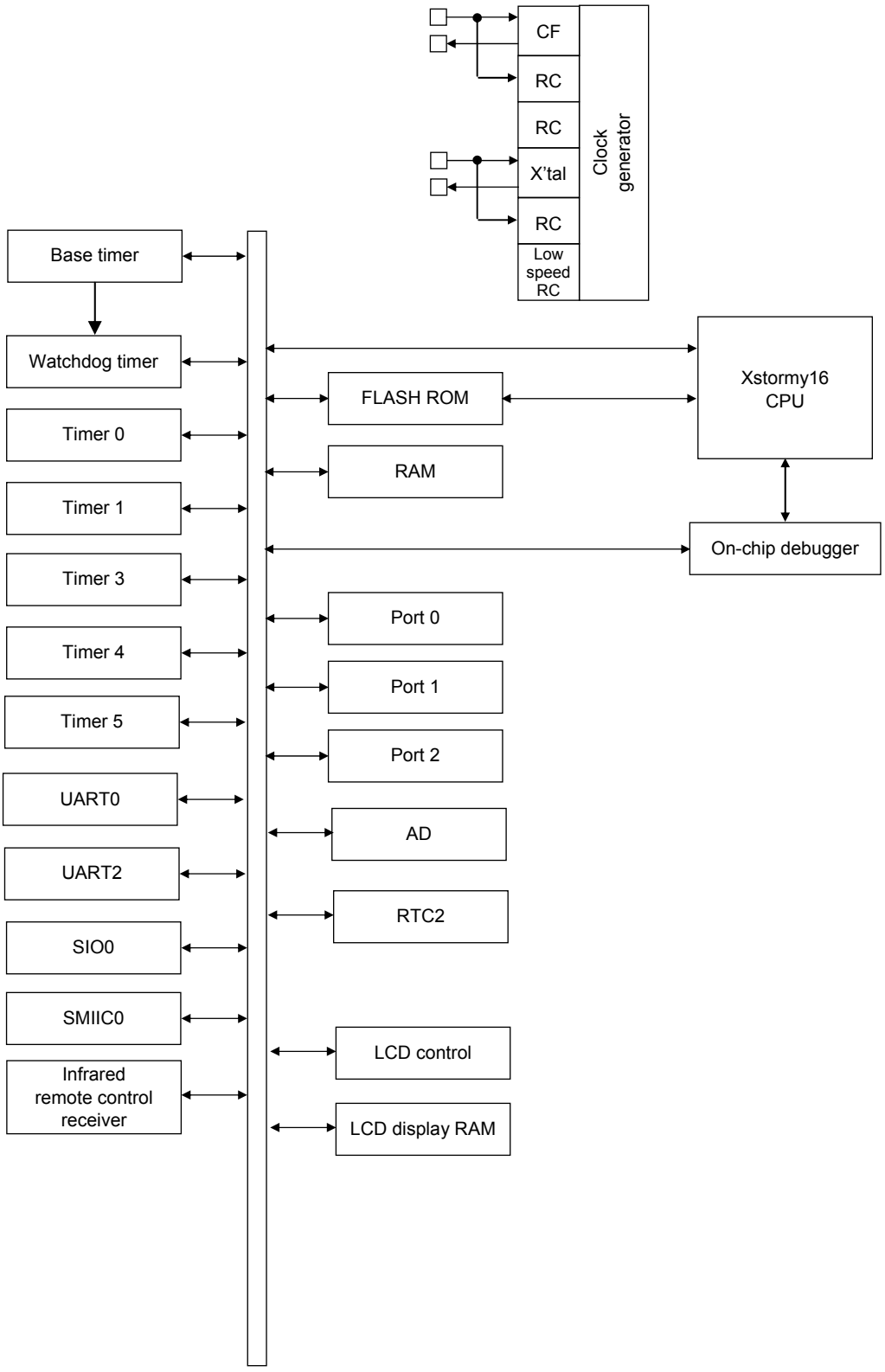
Pin Assignment



Top view

SANYO: TQFP120 (14×14) “Lead-free Type”

System Block Diagram



Pin Description

Pin Name	I/O	Description
V_{SS}	-	- Power supply pin
V_{DD}	-	+ Power supply pin
V_{LCD}1 to 4	-	LCD bias power source (connected to capacitors)
$LCDV_{SS}$0, $LCDV_{SS}$1	-	LCD port power source (-)
CUP00, CUP01	-	Switching pins for generating the LCD drive voltage. A capacitor must be connected across both pins.
PORT 0 P00 to P07	I/O	• 8-bit I/O port • I/O specifiable in 1 bit units • Pull-up registers can be turned on and off in 1-bit units. • HOLD releaset inputs (P00 to P03, P04, P05) • Port 0 interrupt inputs (P00 to P03, P04, P05) • Pin functions P00 (AN8) to P07 (AN15): AD converter inputs P06: Timer 0L output P07: Timer 0H output/UART0 clock input
PORT 1 P10 to P17	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up registers can be turned on and off in 1-bit units. • Pin functions P10: SIO0 data output P11: SIO0 data input/bus input/output P12: SIO0 clock input/output P13: Timer 3L output P14: Timer 3H output/UART0 receive P15: UART0 transmit P16: UART2 receive P17: UART2 transmit
PORT 2 P20 to P23	I/O	• 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up registers can be turned on and off in 1-bit units. • Pin functions P20 (AN0) to P23 (AN3): AD converter inputs P20: Timer 4 output/remote controller receive P21: Timer 5 output P22: SMIIC0 clock input/output P23: SMIIC0 bus input/output/data input
COM0 to COM15	O	• LCD common output
COM16/SEG0 to COM31/SEG15	O	• LCD common output/segment output Common output/segment output switched by a register
SEG16 to SEG47	O	• LCD segment output
SEG48 to SEG63	I/O	• LCD segment output • SEG63-SEG48: General-purpose N-channel open drain output/general-purpose input SEG63-SEG48: LCD output in 4-bit units/general-purpose N-channel open drain output/general-purpose input selectable • SEG63-SEG56: Interrupt function (4-bit units) Chatter removal sampling frequency select (4-bit units) Level/edge sense mode select (4-bit units) Hi/low level or rising/falling edge sense mode select (1-bit units) • SEG63-SEG62: Timer 3 external input
TEST	I/O	• TEST pin • On-chip debugger communication pin • An external 100kΩ pull-down resistor must be connected.
RESB	I	Reset pin
CF1	I	Ceramic oscillator input/RC oscillator resistor to be connected
CF2	O	Ceramic oscillator output
XT1	I	32.768kHz crystal oscillator input/RC oscillator resistor to be connected
XT2	O	32.768kHz crystal oscillator output

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Options Selected in Units of	Output Type	Pull-up Resistor
P00 to P07	1 bit	CMOS	Programmable
P10 to P17 P20 to P23	1 bit	Multiplexed pin outputs are programmable either as CMOS or N-channel open drain output.	Programmable
SEG48 to SEG63	4 bits	N-channel open drain (LCD segment output)	None

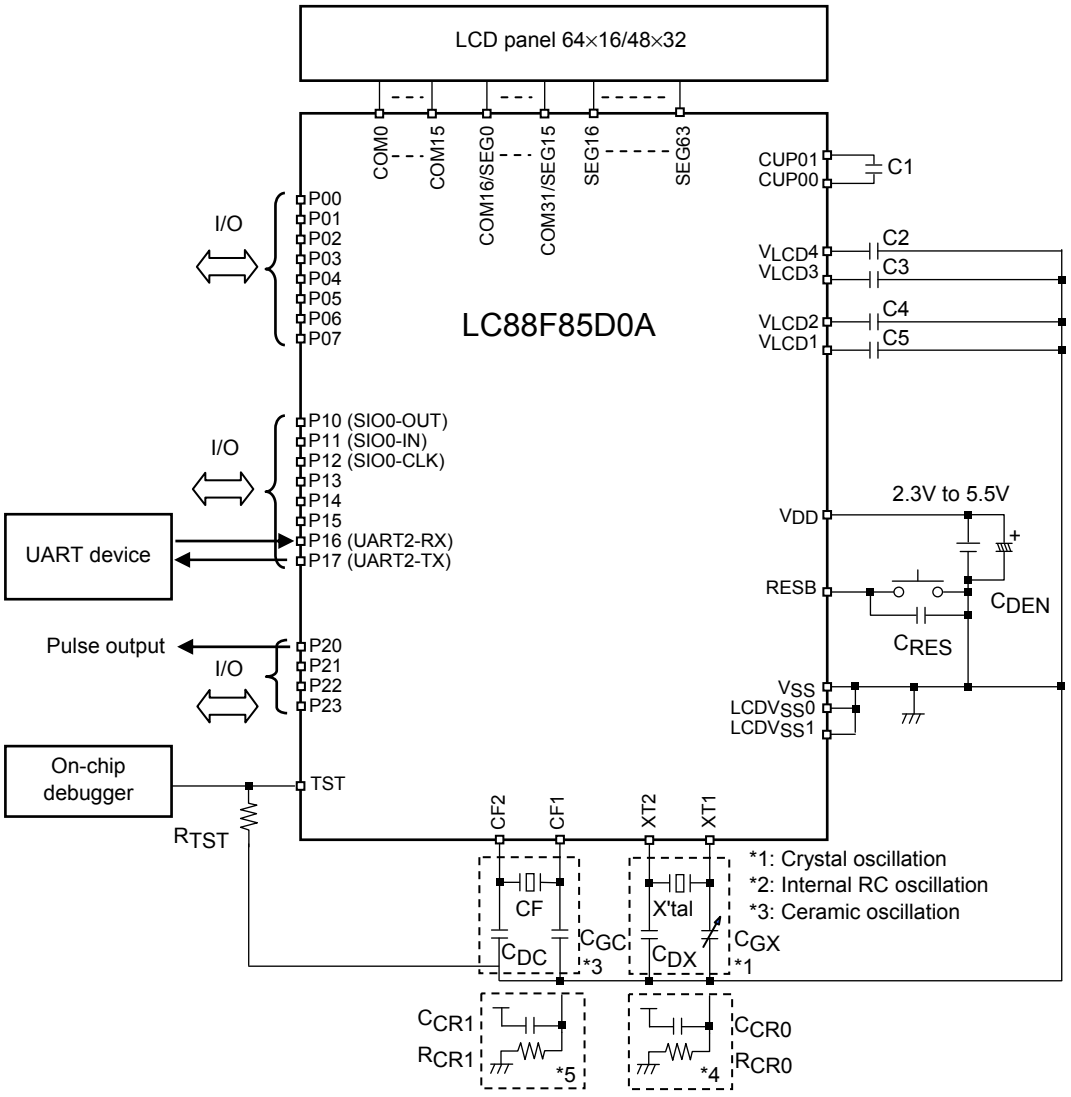
Table of User Options

Option Name	Option	Description
X'tal OSC (*1)	Normal	Normal XT mode
	Low Power	Low power XT mode
Interrupt Vector (*2)	Normal	Interrupt vector switching
	LC888300 Compatible	

*1 The circuit constant values of the external components and oscillation stabilization time differ between the normal XT mode and low power XT mode.

*2 The "LC888300 Compatible" mode is an option that is available to provide compatibility between this model and the LC888300. It is to be unavailable in future models.

Application circuit



X'tal	Crystal resonator	
C_{GX}	Trimmer capacitor	
C_{DX}	Capacitor for X'tal oscillator	
R_{CR0}	Resistor for low-speed oscillator	*4: RC oscillation type
C_{CR0}	Capacitor for low-speed oscillation stabilization	*4: RC oscillation type (*1)
(*1)	0.1μF capacitor is recommended when using XT1/XT2 as the system clock source.	
CF	Ceramic resonator	
C_{GC}	Capacitor for CF oscillator	
C_{DC}	Capacitor for CF oscillator	
R_{CR1}	Resistor for high-speed oscillation	*5: RC oscillation type
C_{CR1}	Capacitor for high-speed oscillation stabilization	*5: RC oscillation type
C1 to C5	Capacitor	
C_{DEN}	Electrolytic capacitor	
C_{RES}	Capacitance for RESB	
R_{TST}	Resistor used when using the on-chip debugger	

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = LCDV_{SS}0 = LCDV_{SS}1 = 0V

Parameter		Symbol	Pin/Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	V_{DD}	V_{DD}		-0.3		+6.5	V
LCD supply voltage		V_{LCD} max	V_{LCD}2 to V_{LCD}4	V_{DD}		-0.3		+6.5	
Maximum LCD supply voltage		LCD max	SEG0 to SEG63 COM0 to COM31	V_{DD}, V_{LCD}4		-0.3		+6.5	
Input voltage		V_I(1)	CF1, XT1, RESB			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 2 SEG63 to SEG48			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 2	CMOS output select Per 1 applicable pin		-5			mA
		IOPH(2)	Port 1	Per 1 applicable pin		-14			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 2	CMOS output select Per 1 applicable pin		-3			
		IOMH(2)	Port 1	CMOS output select Per 1 applicable pin		-9			
	Total output current	ΣIOAH(1)	Ports 0, 2	Total of all applicable pins		-22.5			
		ΣIOAH(2)	Port 1	Total of all applicable pins		-25			
		ΣIOAH(3)	Ports 0, 1, 2	Total of all applicable pins		-47.5			
Low level output current	Peak output current	IOPL(1)	Ports 0, 2	Per 1 applicable pin				13	
		IOPL(2)	Port 1	Per 1 applicable pin				17	
	Mean output current (Note 1-1)	IOML(1)	Ports 0, 2	Per 1 applicable pin				7.5	
		IOML(2)	Port 1	Per 1 applicable pin				10.5	
	Total output current	ΣIOAL(1)	Ports 0, 2	Total of all applicable pins				35	
		ΣIOAL(2)	Port 1	Total of all applicable pins				60	
		ΣIOAL(3)	Ports 0, 1, 2	Total of all applicable pins				80	
Allowable power dissipation		Pd max		Ta=-20 to +75°C				250	mW
Operating ambient temperature		Topr				-20		+75	°C
Storage ambient temperature		Tstg				-65		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Allowable Operating Conditions at Ta = -20°C to +75°C, V_{SS} = LCDV_{SS}0 = LCDV_{SS}1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Ratings			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note2-1)	V_{DD}(1)	V_{DD}	0.098µs≤tCYC≤66µs		4.5		5.5	V
			0.123µs≤tCYC≤66µs		3.0		5.5	
			0.490µs≤tCYC≤66µs		2.0		5.5	
LCD drive voltage	V_{LCD}(1)	V_{LCD}2 to V_{LCD}4					5.5	
Memory sustaining supply voltage	VHD	V_{DD}	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	V_{IH}(1)	Ports 0, 1, 2	Output disabled		0.30V_{DD} +0.70		V_{DD}	
	V_{IH}(2)	CF1, RESB			0.75V_{DD}		V_{DD}	
Low level input voltage	V_{IL}(1)	Ports 0, 1, 2	Output disabled		V_{SS}		0.10V_{DD} +0.40	
	V_{IL}(2)	CF1, RESB			V_{SS}		0.25V_{DD}	
Instruction cycle time (Note 2-2)	tCYC			4.5 to 5.5	0.098		66	µs
				3.0 to 5.5	0.123		66	
				2.0 to 5.5	0.490		66	
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5%	4.5 to 5.5	0.1		10	MHz
				3.0 to 5.5	0.1		8	
				2.0 to 5.5	0.1		2	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1,CF2	10MHz ceramic oscillation See Fig. 1.	4.5 to 5.5		10		MHz
	FmCF(2)	CF1,CF2	8MHz ceramic oscillation See Fig. 1.	3.0 to 5.5		8		
	FmCF(3)	CF1,CF2	4MHz ceramic oscillation See Fig. 1.	2.4 to 5.5		4		
	FmRC		Internal RC oscillation	2.0 to 5.5	0.5	1.0	2.0	
	FmSLRC		Internal SLRC oscillation	2.0 to 5.5	18	30	45	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.2 to 5.5		32.768		
	FmRC1(1)	CF1	High-speed RC oscillation (Note 2-4)	2.4 to 5.5	400		4200	
	FmRC1(2)	CF1	High-speed RC oscillation (Note 2-4)	2.0 to 5.5	400		2000	
	FsRC0	XT1	Low-speed RC oscillation (Note 2-4)	2.2 to 5.5	30		80	

Note2-1: V_{DD} must be held greater than or equal to 3.0V when onboard writing to flash ROM.

Note2-2: Relationship between tCYC and oscillation frequency is 1/FmCF at a frequency division ratio of 1/1 and 2/FmCF at a division ratio of 1/2.

Note2-3: See Tables 1 and 2 for the oscillation constants.

Note2-4: Ta=0°C to 60°C

Electrical Characteristics at Ta = -20°C to +75°C, V_{SS} = LCDV_{SS}0 = LCDV_{SS}1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	I_{IH}(1)	Ports 0, 1, 2 RESB	Output disabled Pull-up resistor off V_{IN}=V_{DD} (including output Tr off leakage current)	2.0 to 5.5			1	μA
Low level input current	I_{IL}(1)	Ports 0, 1, 2	Output disabled Pull-up resistor off V_{IN}=V_{SS} (including output Tr off leakage current)	2.7 to 5.5	-1			μA
High-level output voltage	V_{OH}(1)	Ports 0, 1, 2	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	V_{OH}(2)		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(3)		I_{OH}=-0.1mA	2.0 to 5.5	V_{DD}-0.4			
	V_{OH}(4)	COM0 to COM31	I_{OH}=-25μA	2.0 to 5.5	V_{LCD}4 -0.05			
	V_{OH}(5)	SEG0 to SEG63	I_{OH}=-10μA	2.0 to 5.5	V_{LCD}4 -0.05			
Low level output voltage	V_{OL}(1)	Ports 0, 1, 2	I_{OL}(1)=10mA	4.5 to 5.5			1.5	
	V_{OL}(2)		I_{OL}(1)=1.6mA	3.0 to 5.5			0.4	
	V_{OL}(3)		I_{OL}(1)=0.7mA	2.0 to 5.5			0.4	
	V_{OL}(4)	COM0 to COM31	I_{OLH}=25μA	2.0 to 5.5			V_{SS} +0.05	
	V_{OL}(5)	SEG0 to SEG63	I_{OL}=10μA	2.0 to 5.5			V_{SS} +0.05	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2	V_{OH}=0.9V_{DD}	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.0 to 4.5	18	55	180	
Hysteresis voltage	VHYS	Ports 0, 1, 2 RESB		2.0 to 5.5		0.1V_{DD}		V
Pin capacitance	CP	All pins	For pins other than that under test V_{IN}=V_{SS} f=1MHz Ta=25°C	2.0 to 5.5		10		pF

LCD Drive Voltage at Ta = -20°C to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Special notes: 0.1µF capacitors are connected to $V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, and $V_{LCD}4$. (with no panel load)

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
LCD drive voltage	$V_{LCD}1$	V_{DD} $V_{LCD}1$	Contrast “00”	2.0 to 5.5	Typ ×0.88	1.030	Typ ×1.10	V
			Contrast “01”			1.045		
			Contrast “02”			1.060		
			Contrast “03”			1.075		
			Contrast “04”			1.090		
			Contrast “05”			1.105		
			Contrast “06”			1.120		
			Contrast “07”			1.135		
			Contrast “08”			1.150		
			Contrast “09”			1.165		
			Contrast “10”			1.180		
			Contrast “11”			1.195		
			Contrast “12”			1.210		
			Contrast “13”			1.225		
			Contrast “14”			1.240		
			Contrast “15”			1.255		
	$V_{LCD}2$					$2×V_{LCD}1$		
	$V_{LCD}3$					$3×V_{LCD}1$		
	$V_{LCD}4$					$4×V_{LCD}1$		

Serial I/O Characteristics at Ta = -20°C to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

SIO0 Serial I/O Characteristics (When wakeup function is not in used) (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 6.	2.0 to 5.5	4			tCYC
		Low level pulse width	tSCKL(1)				2			
		High level pulse width	tSCKH(1)				2			
			tSCKHA(1)		• Automatic communication mode • See Fig. 6.		6			
			tSCKHBSY(1a)		• Automatic communication mode • See Fig. 6.		23			
			tSCKHBSY(1b)		• Mode other than automatic communication mode • See Fig. 6.		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output type selected • See Fig. 6.	2.0 to 5.5	4			tCYC
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Automatic communication mode • CMOS output type selected • See Fig. 6.		6			tCYC
			tSCKHBSY(2a)		• Automatic communication mode • CMOS output type selected • See Fig. 6.		4		23	
			tSCKHBSY(2b)		• Mode other than automatic communication mode • See Fig. 6.		4			
Serial input	Data setup time		tsDI(1)	SI0(P11), SB0(P11)	• Specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.0 to 5.5	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• (Note4-1-2)	2.0 to 5.5			1tCYC +0.05	
	Output clock		tdDO(2)		• (Note4-1-2)				1tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-1-2: Specified with respect to the falling edge of SIOCLK. Specified as the time up to the time the output state is changed in the open drain output mode. See Fig. 6.

SIO1 Serial I/O Characteristics (When wakeup function is not in used) (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(3)	SCK0(P12)	• See Fig. 6.	2.0 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
			tSCKHBSY(3)				2			
Serial input	Data setup time		tsDI(2)	SI0(P11), SB0(P11)	• Specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.0 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Input clock	Output delay time	tdD0(3)	SO0(P10), SB0(P11)	• (Note4-2-2)	2.0 to 5.5			1tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-2-2: Specified with respect to the falling edge of SIOCLK. Specified as the time up to the time the output state is changed in the open drain output mode. See Fig. 6.

SMIIC0 Simple SIO Mode I/O Characteristics

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(7)	SM0CK (P22)	• See Fig. 6.	2.0 to 5.5	4			tCYC
		Low level pulse width	tSCKL(7)				2			
		High level pulse width	tSCKH(7)				2			
	Output clock	Period	tSCK(8)	SM0CK (P22)	• CMOS output type selected • See Fig. 6.		4			
		Low level pulse width	tSCKL(8)				1/2			tSCK
		High level pulse width	tSCKH(8)				1/2			
Serial input	Data setup time		tsDI(5)	SM0DA (P23)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.0 to 5.5	0.03			µs
	Data hold time		thDI(5)				0.03			
Serial output	Output delay time		tdD0(7)	SM0DA (P23)	• Specified with respect to falling edge of SIOCLK • Specified as the time up to the beginning of output change . • See Fig. 6.	2.0 to 5.5			1tCYC +0.05	

Note 4-3-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

SMIIC0 I²C Mode I/O Characteristics

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Clock	Input clock	Period	tSCL	SM0CK (P22)	• See Fig. 8.	2.0 to 5.5	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM0CK (P22)	• Specified as the time up to the beginning of output change.	2.0 to 5.5	10			
		Low level pulse width	tSCLLx				1/2			tSCL
		High level pulse width	tSCLHx				1/2			
SM0CK, SM0DA pin input spike suppression time			tsp	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5			1	Tfilt
Start-to-stop period bus release time	Input		tBUF	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5	2.5			Tfilt
	Output		tBUFx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as the time up to the beginning of output change.		5.5			µs
					• High-speed clock mode • Specified as the time up to the beginning of output change.		1.6			
Start/restart condition hold time	Input		tHD;STA	SM0CK(P22) SM0DA(P23)	• When SMIIC register control bit I²CSHDS=0 • See Fig. 8.	2.0 to 5.5	2.0			Tfilt
					• When SMIIC register control bit I²CSHDS=1 • See Fig. 8.		2.5			
	Output		tHD;STAx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as the time up to the beginning of output change.		4.1			µs
					• High-speed clock mode • Specified as the time up to the beginning of output change.		1.0			
Restart condition setup time	Input		tSU;STA	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5	1.0			Tfilt
	Output		tSU;STAx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as the time up to the beginning of output change.		5.5			µs
					• High-speed clock mode • Specified as the time up to the beginning of output change.		1.6			

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Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	Unit
Stop condition setup time	Input	tSU;STO	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5	1.0			Tfilt
	Output	tSU;STOx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as the time up to the beginning of output change.		4.9			µs
				• High-speed clock mode • Specified as the time up to the beginning of output change.		1.1			
Data hold time	Input	tHD;DAT	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5	0			Tfilt
	Output	tHD;DATx	SM0CK(P22) SM0DA(P23)	• Specified as the time up to the beginning of output change.		1		1.5	
Data setup time	Input	tSU;DAT	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5	1			Tfilt
	Output	tSU;DATx	SM0CK(P22) SM0DA(P23)	• Specified as the time up to the beginning of output change.		1tSCL-1.5Tfilt			
SM0CK, SM0DA pin fall time	Input	tF	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5			300	ns
	Output	tF	SM0CK(P22) SM0DA(P23)	• When SMIIC register control bits PSLW=1, P5V=1	5	20+0.1Cb		250	
				• When SMIIC register control bits PSLW=1, P5V=0	3	20+0.1Cb		250	
				• When SM0CK and SM0DA port outputs are placed in fast mode • Cb≤400pF	3.0 to 5.5			100	

Note 4-4-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-4-2: Tfilt denotes the value that is determined by the values of register SMIC0BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set up (BPR1, BPR0) so that Tfilt falls within the following range:

250ns ≥ Tfilt > 140ns

Note 4-4-3: Cb denotes the total capacitance (in pF) of the loads connected to each bus. Cb ≤ 400pF

Note 4-4-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG within the following ranges:

250ns ≥ Tfilt > 140ns

BRDQ (bit 5) = 1

SCL frequency setting ≤ 100kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250ns ≥ Tfilt > 140ns

BRDQ (bit 5) = 0

SCL frequency setting ≤ 400kHz

UART0 Operating Conditions at Ta = -20 to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR0	U0RX(P14), U0TX(P15), U0BRG(P07)		2.0 to 5.5	4		8	tBGCYC

Note 4-5: tBGCYC denotes 1 period of the baudrate clock source.

UART2 Operating Conditions at Ta = -20 to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR2	U2RX(P16), U2TX(P17)		2.0 to 5.5	8		4096	tBGCYC

Note 4-6: tBGCYC denotes 1 period of the baudrate clock source.

Pulse Input Conditions at Ta = -20 to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
	tPIL(2)	RESB	Resettable.	2.0 to 5.5	10			µs

AD Converter Characteristics at Ta = -20 to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

12-bits AD Conversion Mode

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	NAD	AN0(P20), AN1(P21), AN2(P22), AN3(P23), AN8(P00) to AN15(P07)		2.9 to 5.5		12		bit
Absolute accuracy	ETAD		(Note 6-1)	2.9 to 5.5			±16	LSB
Conversion time	TCAD12		Conversion time is calculated.	4.5 to 5.5	27		209	µs
				2.9 to 5.5	67		209	
Analog input voltage range	VAIN			2.9 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.9 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	2.9 to 5.5	-1			

• Conversion time calculation method: TCAD12= ((52/(AD division ratio))+2) × tCYC

8-bits AD Conversion Mode

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	NAD	AN0(P20), AN1(P21), AN2(P22), AN3(P23), AN8(P00) to AN15(P07)		2.9 to 5.5		8		bit
Absolute accuracy	ETAD		(Note 6-1)	2.9 to 5.5			±1.5	LSB
Conversion time	TCAD8		Conversion time is calculated.	4.5 to 5.5	17		129	µs
				2.9 to 5.5	42		129	
Analog input voltage range	VAIN			2.9 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.9 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	2.9 to 5.5	-1			

• Conversion time calculation method: TCAD8= ((32/(AD division ratio))+2) × tCYC

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy.

Note 6-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.

The conversion time is twice the normal value when one of the following conditions occurs:

- The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

Consumption Current Characteristics at Ta = -20 to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/ Remarks	Conditions		V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	V_{DD}	• FOSC0=32.768kHz • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 • Normal XT mode [No panel load]	LCD display ON	2.0 to 5.5		87	170	µA
	IDDOP(2)				2.0 to 3.6		44	110	
	IDDOP(3)			LCD display OFF	2.0 to 5.5		75	155	
	IDDOP(4)				2.0 to 3.6		35	95	
	IDDOP(5)		• FOSC0=32.768kHz • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 • Low power XT mode [No panel load]	LCD display ON	2.0 to 5.5		53	100	
	IDDOP(6)				2.0 to 3.6		35	65	
	IDDOP(7)			LCD display OFF	2.0 to 5.5		48	92	
	IDDOP(8)				2.0 to 3.6		31	55	
	IDDOP(9)		• FmCF=10MHz ceramic oscillator • FOSC0=0Hz (oscillation stopped) • System clock set to 10MHz side • Internal RC oscillation stopped • Frequency division ratio set to 1/1		4.5 to 5.5		8.4	15.2	mA
	IDDOP(10)		• FmCF=8MHz ceramic oscillator oscillator • FOSC0=0Hz (oscillation stopped) • System clock set to 8MHz side • Internal RC oscillation stopped • Frequency division ratio set to 1/1		4.5 to 5.5		7.6	14.7	
	IDDOP(11)				3.0 to 4.5		5.8	11	
	IDDOP(12)		• FmCF=4MHz ceramic oscillator • FOSC0=0Hz (oscillation stopped) • System clock set to 4MHz • Internal RC oscillation stopped • Frequency division ratio set to 1/2		4.5 to 5.5		3.6	5.5	
	IDDOP(13)				2.2 to 4.5		2.2	4.7	
	IDDOP(14)		• System clock set to internal RC side • Internal RC oscillation oscillated • FOSC0=0Hz (oscillation stopped) • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1		2.0 to 5.5		2.2	5.6	
	IDDOP(15)				2.0 to 3.6		1.2	3.6	
	IDDOP(16)		• FOSC1=1MHz R_{CR1}=470kΩ • System clock set to FOSC1 side • Internal RC oscillation stopped • FOSC0=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 *Ta=0 to 60°C		2.0 to 5.5		1.5	2.6	
	IDDOP(17)				2.0 to 3.6		1.0	2.5	
	IDDOP(18)		• FOSC0=64kHz R_{CR0}=910kΩ • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 *Ta=0 to 60°C		2.0 to 5.5		100	187	µA
	IDDOP(19)				2.0 to 3.6		62	120	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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Parameter	Symbol	Pin/ Remarks	Conditions		Specification				
					V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 7-2)	IDDHALT(1)	V_{DD}	HALT mode • FOSC0=32.768kHz • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 • Normal XT mode [No panel load]	LCD display ON	2.0 to 5.5		45	110	μA
	IDDHALT(2)				2.0 to 3.6		16	50	
	IDDHALT(3)			LCD display OFF	2.0 to 5.5		36	90	
	IDDHALT(4)				2.0 to 3.6		7.8	51	
	IDDHALT(5)		HALT mode • FOSC0=32.768kHz • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 • Low power XT mode [No panel load]	LCD display ON	2.0 to 5.5		15.5	53	
	IDDHALT(6)				2.0 to 3.6		12	30	
	IDDHALT(7)			LCD display OFF	2.0 to 5.5		6.5	40	
	IDDHALT(8)				2.0 to 3.6		4	30	
	IDDHALT(9)		HALT mode • FmCF=10MHz ceramic oscillator • FOSC0=0Hz (oscillation stopped) • System clock set to 10MHz side • Internal RC oscillation stopped • Frequency division ratio set to 1/1		4.5 to 5.5		2.0	3.4	mA
	IDDHALT(10)		HALT mode • FmCF=8MHz ceramic oscillator • Internal RC oscillation stopped • FOSC0=0Hz (oscillation stopped) • System clock set to 8MHz side • Internal RC oscillation stopped • Frequency division ratio set to 1/1		4.5 to 5.5		1.7	2.9	
	IDDHALT(11)				3.0 to 4.5		1.2	2.1	
	IDDHALT(12)		HALT mode • FmCF=4MHz ceramic oscillator • FOSC0=0Hz (oscillation stopped) • System clock set to 4MHz side • Internal RC oscillation stopped • Frequency division ratio set to 1/2		4.5 to 5.5		0.7	1.2	
	IDDHALT(13)				2.2 to 4.5		0.3	0.85	
	IDDHALT(14)		HALT mode • System clock set to internal RC side • Internal RC oscillation oscillated • FOSC0=0Hz (oscillation stopped) • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1		2.0 to 5.5		0.7	1.3	
	IDDHALT(15)				2.0 to 3.6		0.3	0.6	
	IDDHALT(16)		HALT mode • FOSC1=1MHz R_{CR1}=470kΩ • System clock set to FOSC1 side • Internal RC oscillation stopped • FOSC0=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 *Ta=0 to 60°C		2.0 to 5.5		0.2	0.5	
	IDDHALT(17)				2.0 to 3.6		0.1	0.3	
	IDDHALT(18)		HALT mode • FOSC0=64kHz R_{CR0}=910kΩ • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 *Ta=0 to 60°C		2.0 to 5.5		20	60	μA
	IDDHALT(19)				2.0 to 3.6		10	40	

Note 7-2: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HOLD mode consumption current	IDDHOLD(1)	V_{DD}	HOLD mode • CF1=V_{DD} or open (external clock mode)	2.0 to 5.5		0.08	35	μA
	IDDHOLD(2)			2.0 to 3.6		0.02	25	
HOLDX mode consumption current	IDDHOLD(3)		HOLDX mode • CF1=V_{DD} or open (external clock mode) • FOSC0=32.768kHz • Normal XT mode	2.0 to 5.5		30	65	
	IDDHOLD(4)			2.0 to 3.6		5	55	
	IDDHOLD(5)		HOLDX mode • CF1=V_{DD} or open (external clock mode) • FOSC0=32.768kHz • Low power XT mode	2.0 to 5.5		0.6	35	
	IDDHOLD(6)			2.0 to 3.6		0.4	25	

Note 7-3: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

F-ROM Writing Characteristics at Ta = +10°C to +55°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard writing current	IDDFW(1)	V_{DD}	• Excluding power dissipation in the microcontroller block	3.0 to 5.5			15	mA
Writing time	tFW(1)		• 512-/1K-byte erase operation	3.0 to 5.5			30	ms
	tFW(2)		• 2-byte writing operation	3.0 to 5.5			60	μs

Characteristics of a Sample OSC1 System Clock Oscillation Circuit

Sample main system clock oscillation circuit characteristics

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of the Main System Clock Oscillation Circuit that Uses a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [ms]	max [ms]	
10MHz	MURATA Manufacturing Co., Ltd.	CSTCE10M0G52-R0	(10)	(10)	OPEN	150	2.4 to 5.5	0.02	0.5	C1 and C2 integrated type
8MHz		CSTCE8M00G52-R0	(10)	(10)	OPEN	470	2.4 to 5.5	0.02	0.5	C1 and C2 integrated type
4MHz		CSTCR4M00G53-R0	(15)	(15)	OPEN	1.5K	2.2 to 5.5	0.02	0.5	C1 and C2 integrated type
		CSTCR4M00G53095-R0	(15)	(15)	OPEN	1.5K	2.0 to 5.5	0.02	0.5	C1 and C2 integrated type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} exceeds its lower limit operating voltage (see Figure 4).

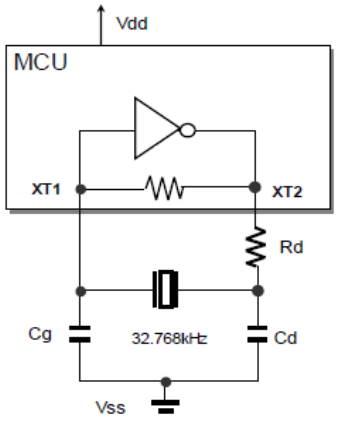
Characteristics of a Sample Subsystem Clock Oscillation Circuit

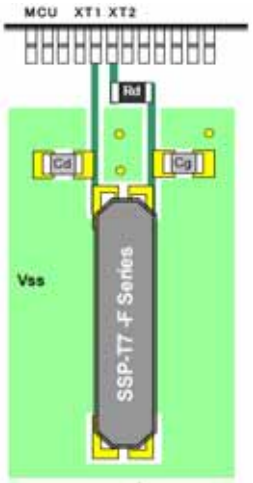
Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit that uses a Crystal Oscillator (*5)

Nominal Frequency	Vendor Name	Resonator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz (*1)	Seiko Instruments (*2)	SSP-T7-F	18	22	OPEN	750K	2.0 to 5.5	1.4	3	CL=12.5pF (*3) Normal XT mode
		VT-200-F								
		SSP-T7-FL	2	3	OPEN	0	2.0 to 5.5	0.8	3	CL=4.4pF(*4) Low power XT mode
		VT-200-FL								

(*1) Normal XT mode (*3) or low power XT mode (*4) should be selected for the sub-system clock oscillator circuit.
(*2) Contact Seiko Instruments, Inc., (http://www.sii-crystal.com) for further information about the use of the resonator.
(*3) When considering the use of normal XT mode, use an resonator that has a large load capacitance.
(*4) When considering the use of low power XT mode, use a resonator that has a small load capacitance. The applicable CL value of 4.4pF makes it possible to achieve a high time accuracy for the subclock oscillator as well as high-speed oscillation startup and low power dissipation. In addition to this value, 6.0pF and 7.0pF also fall within the applicable CL value range.
(*5) A sample PCB trace pattern for a Seiko Instrument resonator is shown below.





(Note 1) The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after an instruction for starting the subclock oscillator circuit is issued or the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).
(Note 2) The circuit constants shown are the reference values that are provided by the resonator vendor for evaluation. To make final verification of the oscillation characteristics on production boards, call the resonator vendor for evaluation on printed circuit boards.
(Note 3) When using an oscillator circuit, observe the following wiring precautions to avoid the possible adverse influence of wiring capacitance, especially in low power XT mode:
- Place the components that are involved in oscillation as close to the resonator as possible with the shortest possible traces as the oscillation characteristics are subject to the variation of trace patterns.
- Do not take a signal directly from the oscillator circuit.
- Do not place the oscillator circuit in the vicinity of any lines that carry large current.
- Exercise extreme care in the wiring method when using low power XT mode.

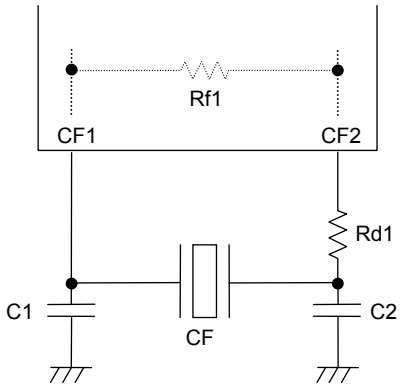


Figure 1 CF Oscillator Circuit

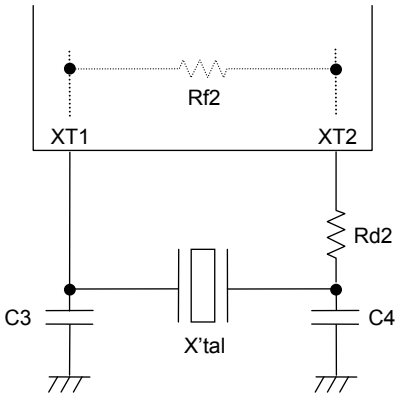


Figure 2 XT Oscillator Circuit

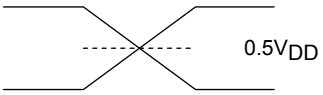
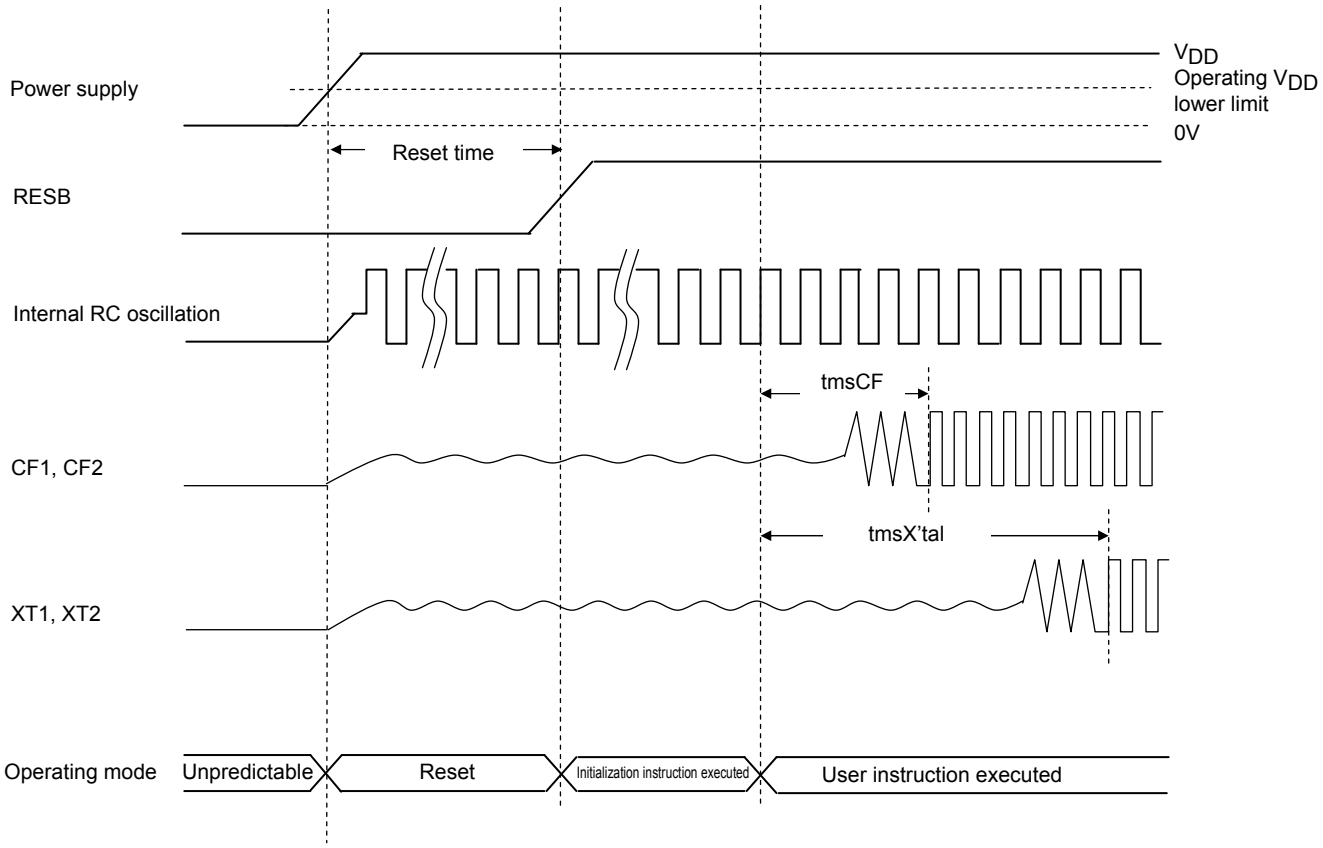
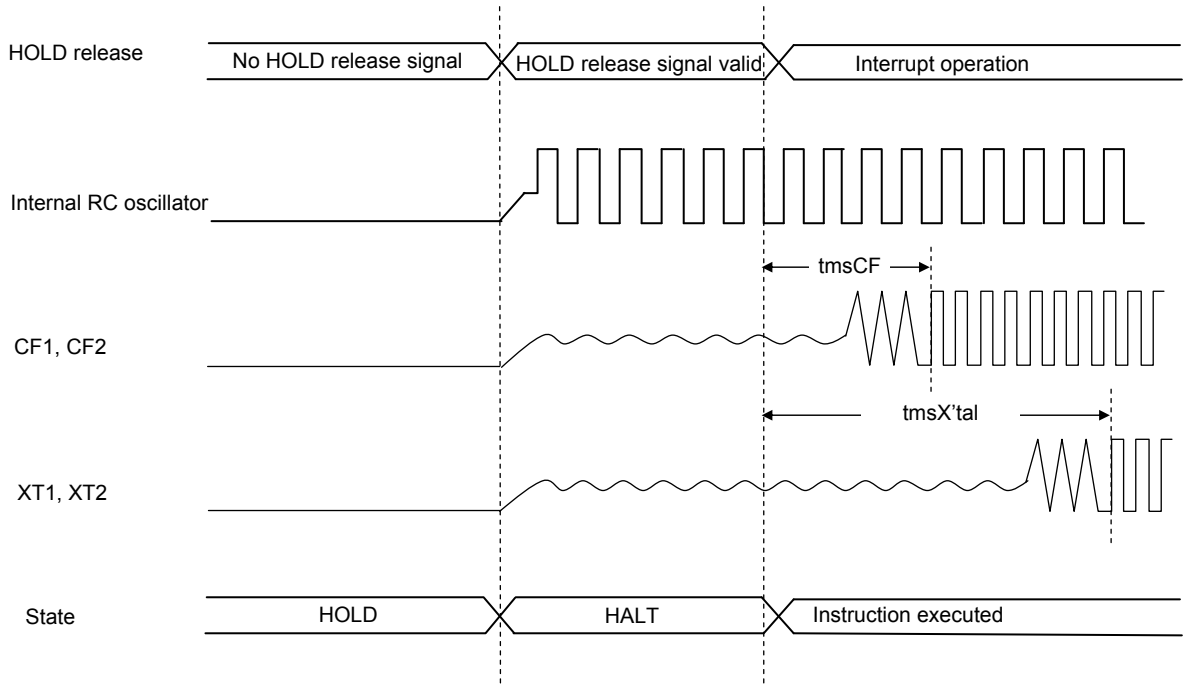


Figure 3 AC Timing Measurement Point

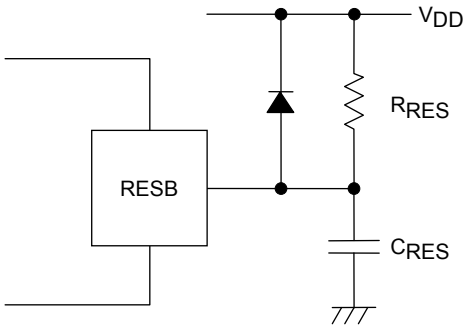


Reset Time and Oscillation Stabilization Time



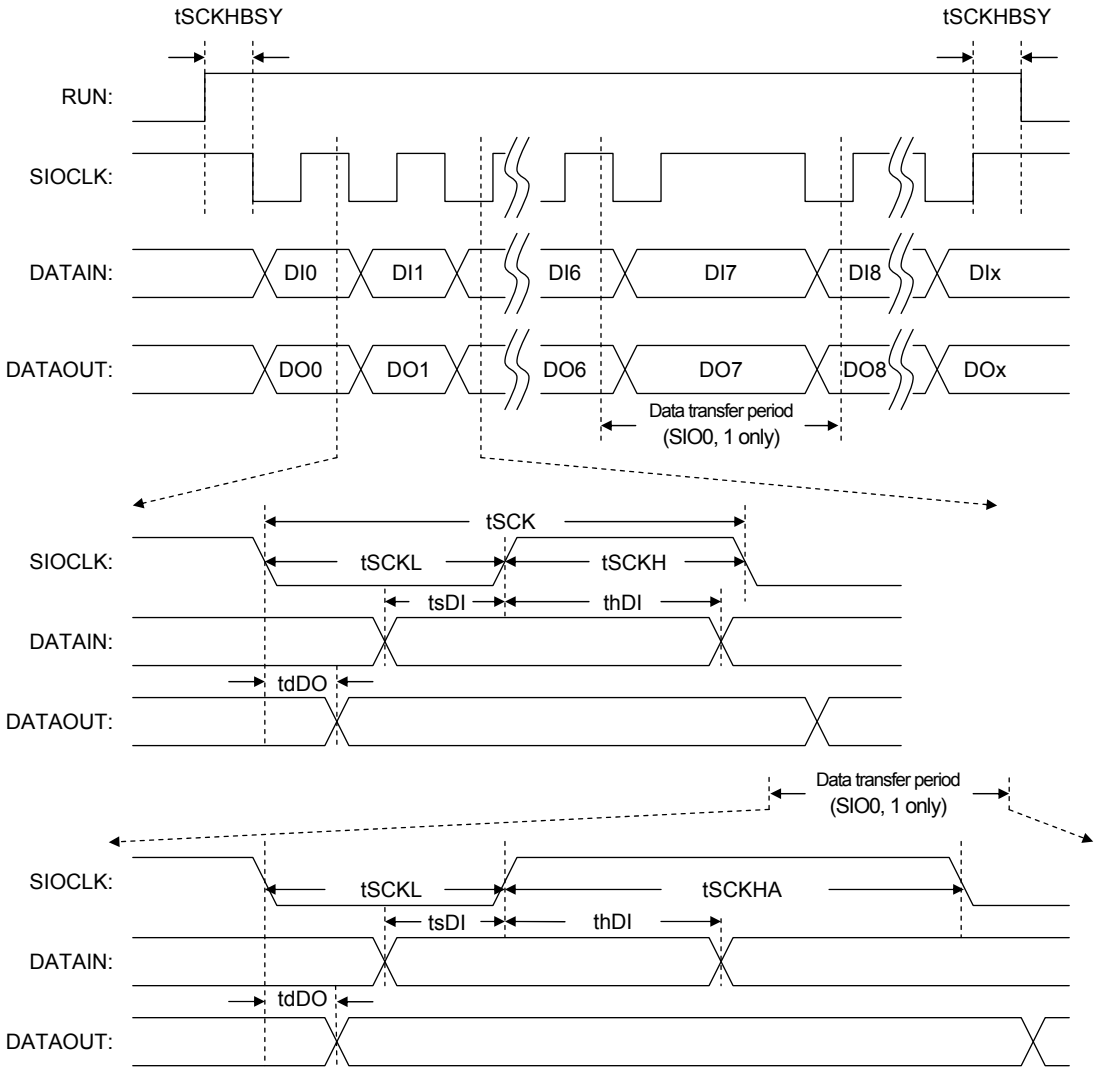
HOLD Reset and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



Note:
Make sure that reset is in effect when power is turned on. Determine the values of C_{RES} and R_{RES} so that the reset is in effect for a period of 10μs after the power gets stabilized.

Figure 5 Reset Circuit



*: Remarks: DIx and DOx are the final communication bits. X = 0 to 32768

Figure 6 Serial I/O Waveforms Examples

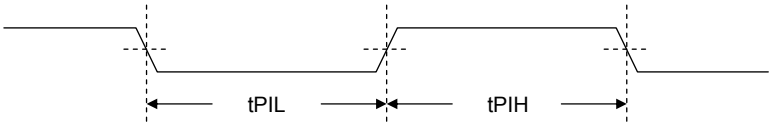
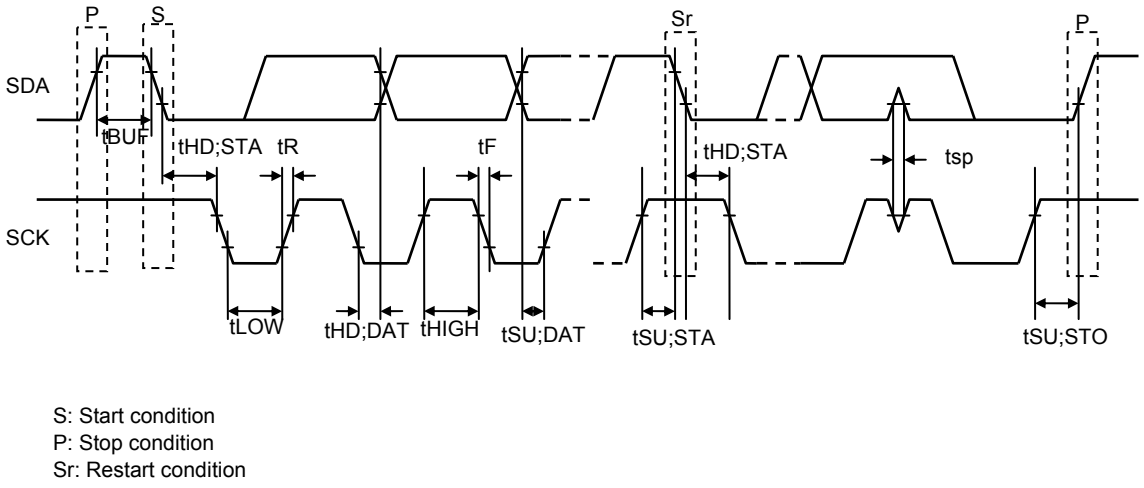


Figure 7 Pulse Input Timing Signal Waveform



S: Start condition
P: Stop condition
Sr: Restart condition

Figure 8 I^2C Timing

Note: The oscillation frequency of any RC oscillator using OSC1 or OSC0 varies according to the printed circuit patterns and components mounted on the board. It also varies greatly according to the shape and form of the product (chip, plastic package, etc.) and board capacitance. Consequently, the characteristics charts given below should be used merely as reference values and the resistance value be determined after evaluating them with the actual product.

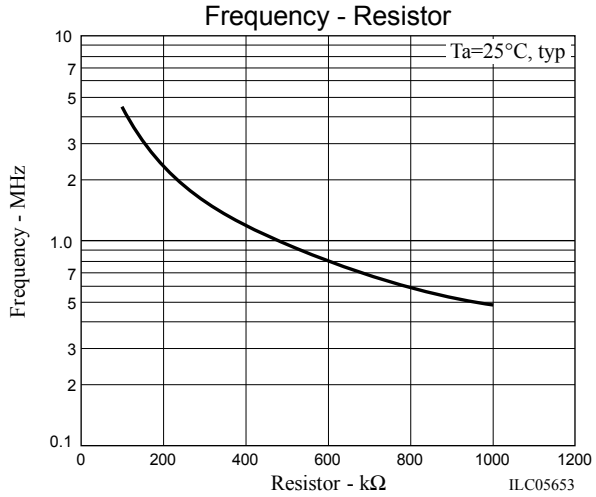


Figure 9 OSC1 Oscillation Frequency vs. Resistance Characteristics

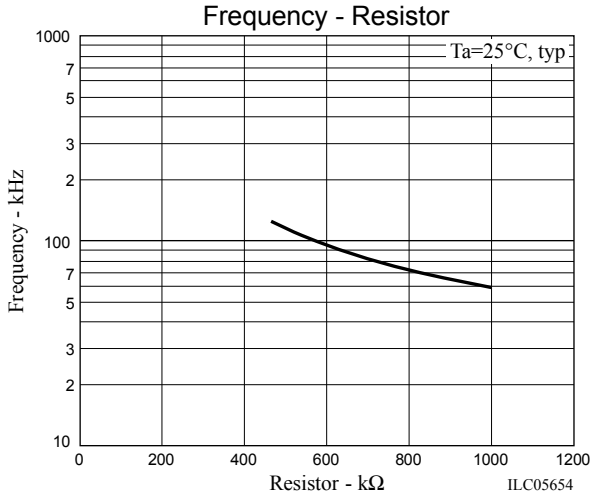


Figure 10 OSC0 Oscillation Frequency vs. Resistance Characteristics