Ordering number : ENA1007

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LC87F6D64A — CMOS IC FROM 64K byte, RAM 2048 byte on-chip 8-bit 1-chip Microcontroller

Overview

The SANYO LC87F6D64A is 8-bit microcomputer with the following on-chip functional blocks:

- CPU: operable at a minimum bus cycle time of 100ns
- 64K-byte flash ROM (re-writeable on board/On-chip debugger)
- On-chip RAM: 2048 byte
- VFD automatic display controller/driver
- 16-bit timer/counter (can be divided into two 8-bit timers)
- two 8-bit timer with prescaler
- timer for use as date/time clock
- Day-Minute-Second Counter (DMSC)
- System clock divider function
- Synchronous serial I/O port (with automatic block transmit /receive function)
- Asynchronous/synchronous serial I/O port
- Remote control receive function
- 8-channel×8-bit AD converter
- 14-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

■Flash ROM

- Single 5V power supply, writeable on-board.
- Block erase in 128 byte units
- 65536 × 8 bits

■RAM

- 2048 × 9 bits

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

■Minimum Bus Cycle Time
- 100ns (10MHz) V_{DD}=3.0 to 5.5V
- 150ns (4MHz) V_{DD}=2.5 to 5.5V

Note: The bus cycle time indicates ROM read time.

■Minimum Instruction Cycle Time (tCYC)
- 300ns (10MHz) V_{DD}=3.0 to 5.5V
- 750ns (4MHz) V_{DD}=2.5 to 5.5V

■Ports
- Input/output ports

  Data direction programmable for each bit individually: 10 (P1n, P7n)
  Data direction programmable in nibble units: 8 (P0n)
  (When N-channel open drain output is selected, data can be input in bit units.)
- VFD output ports

  Large current outputs for digits: 9 (S0/T0 to S8/T8)
  Large current outputs for digits/segments: 7 (S9/T9 to S15/T15)
  Digit/segment outputs: 8 (S16 to S23)
  Segment outputs: 30 (S24 to S53)
- Oscillator pins: 2 (CF1/XT1, CF2/XT2)
- Reset pin: 1 ($\overline{RES}$)
- Power supply: 4 ($V_{SS}1$, $V_{DD}1$ to $V_{DD}3$)
- VFD power supply: 1 (VP)

■VFD Automatic Display Controller
- Programmable segment/digit output pattern

  Output can be switched between digit/segment waveform output
  (pins 9 to 23 can be used for output of digit waveforms).
  parallel-drive available for large current VFD.
- 16-step dimmer function available

■Timers
- Timer 0: 16-bit timer/counter with capture register

  Mode 0: 2 channel 8-bit timer with programmable 8-bit prescaler and 8-bit capture register
  Mode 1: 8-bit timer with 8-bit programmable prescaler and 8-bit capture register
  + 8-bit counter with 8-bit capture register
  Mode 2: 16-bit timer with 8-bit programmable prescaler and 16-bit capture register
  Mode 3: 16-bit counter with 16-bit capture register
- Timer 4: 8-bit timer with 6-bit prescaler
- Timer 5: 8-bit timer with 6-bit prescaler
- Base Timer

  1) The clock signal can be selected from any of the following.
  Sub-clock (32.768kHz crystal oscillator), system clock, and prescaler output from timer 0
  2) Interrupts can be selected to occur at one of five different times.
- Day and time counter

  1) Using with a base timer, it can be used as 65000 day + minute + second counter.

■SIO
- SIO 0: 8-bit synchronous serial interface

  1) LSB first /MSB first function available
  2) Internal 8-bit baud-rate generator (maximum transmit clock period 4/3 tCYC)
  3) Consecutive automatic data communication
  (1 to 256 bits (communication available for each bit) (stop and reopening available for each byte))
- SIO 1: 8-bit asynchronous/synchronous serial interface

  Mode 0: Synchronous 8-bit serial IO (2-wire or 3-wire, transmit clock 2 to 512 tCYC)
  Mode 1: Asynchronous serial IO (half duplex, 8 data bits, 1 stop bit, baud rate 8 to 2048 tCYC)
  Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2 to 512 tCYC)
  Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

■AD Converter: 8 bits × 8 channels

■Remote Control Receiver Circuit (sharing pins with P70/INT0/RMIN)
- Noise rejection function
  (Units of noise rejection filter: about 120μs, when selecting a 32.768kHz crystal oscillator as a clock.)
- Supporting reception formats with a guide-pulse of half-clock/clock/none.
- Determines a end of reception by detecting a no-signal periods (No carrier).
  (Supports same reception format with a different bit length.)
- X'tal HOLD mode release function

■Watchdog Timer
- The watching timer period is set using an external RC.
- Watchdog timer can produce interrupt, system reset.

■Clock Output Function
1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 as system clock.
2) Able to output oscillation clock of sub clock.

■Interrupts: 14 sources, 10 vector interrupts
- Three priority (low, high and highest) multiple interrupts are supported. During interrupt handling, an equal or lower priority interrupt request is refused.
- If interrupt requests to two or more vector addresses occur at once, the higher priority interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt Signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/remote control receiver
4	0001BH	H or L	INT3/Base timer 0/1
5	00023H	H or L	T0H
6	0002BH	H or L	
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC
10	0004BH	H or L	Port0/T4/T5

- Priority Level: X>H>L
- For equal priority levels, vector with lowest address takes precedence.

■Subroutine Stack Levels: 1024 levels maximum (Stack is located in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits
- On-chip RC oscillation circuit for system clock use.
- On-chip CF oscillation circuit* for system clock use. (Rf built in)
- On-chip Crystal oscillation circuit* low speed system clock use. (Rf built in)
- Frequency variable RC oscillation circuit (internal) for system clock.
  1) Adjustable in ±4% (typ) step from a selected center frequency.
  2) Measures oscillation clock using a input signal from XT1 as a reference.

* The CF oscillation terminal and the crystal oscillation terminal cannot be used at the same time because of commonness.

■System Clock Divider Function

- Able to reduce current consumption
  Available minimum instruction cycle time: 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs.
  (Using 10MHz main clock)

■Standby Function

- HALT mode
  HALT mode is used to reduce power consumption. Program execution is stopped. Peripheral circuits still operate but VFD display and some serial transfer operations stop.
  1) Oscillation circuits are not stopped automatically.
  2) Release occurs on system reset or by interrupt.
- HOLD mode
  HOLD mode is used to reduce power consumption. Both program execution and peripheral circuits are stopped.
  1) The CF, RC, X'tal and frequency variable RC oscillators automatically stop operation.
  2) Release occurs on any of the following conditions.
     (1) input to the reset pin goes "Low"
     (2) a specified level is input to at least one of INT0, INT1, INT2
     (3) an interrupt condition arises at port 0
- X'tal HOLD mode.
  X'tal HOLD mode is used to reduce power consumption. Program execution is stopped.
  All peripheral circuits except the base-timer are stopped.
  1) The CF, RC, frequency variable RC oscillation circuits stop automatically.
  2) Crystal oscillator is maintained in its state at HOLD mode inception.
  3) Release occurs on any of the following conditions.
     (1) input to the reset pin goes "Low"
     (2) Setting at least one of the INT0, INT1 and INT2 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established in the base timer circuit
     (5) Having an interrupt source established in the remote control receiver circuit

■On-chip Debugger

- Supports software debugging with the IC mounted on the target board.

■Package Form

- QFP80(14×14): Lead-free type

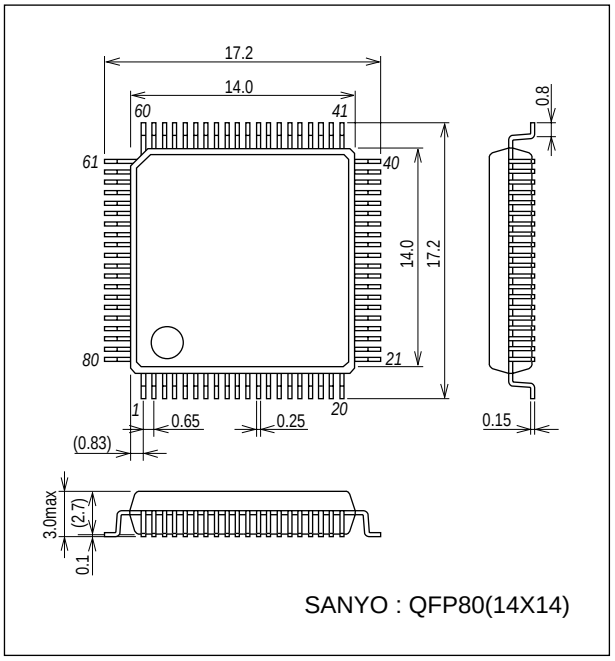
■Development Tools

- On-chip debugger: TCB87- type-B + LC87F6D64A

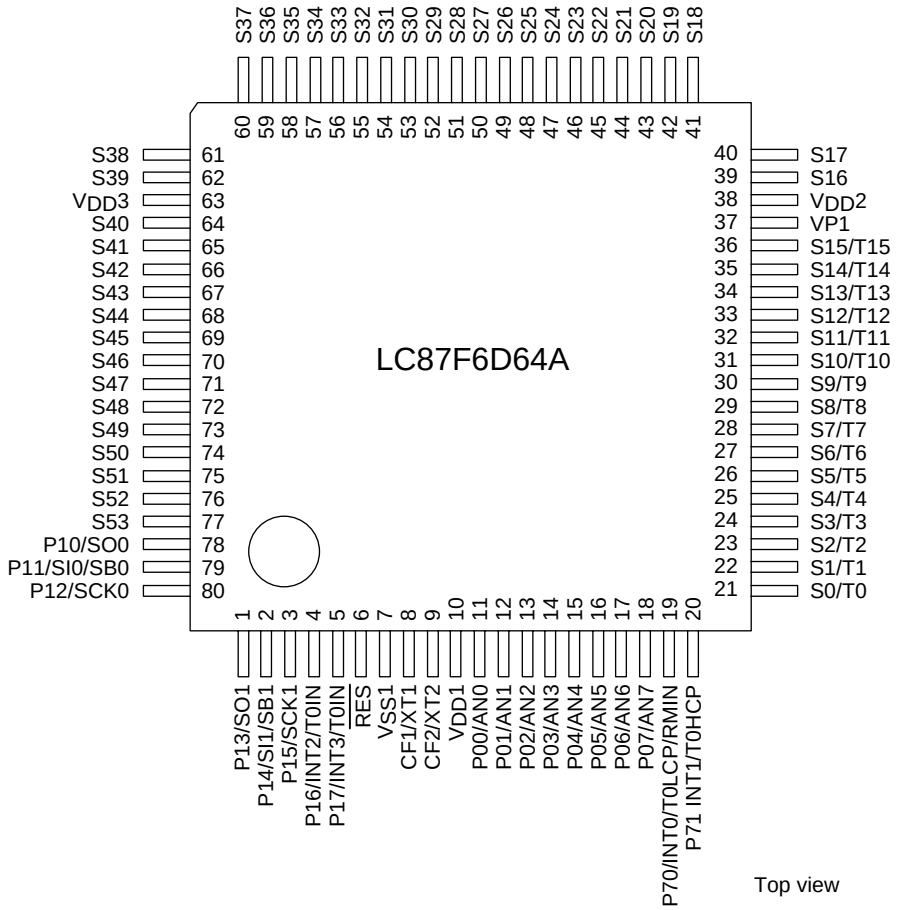
Package Dimensions

unit : mm (typ)

3255

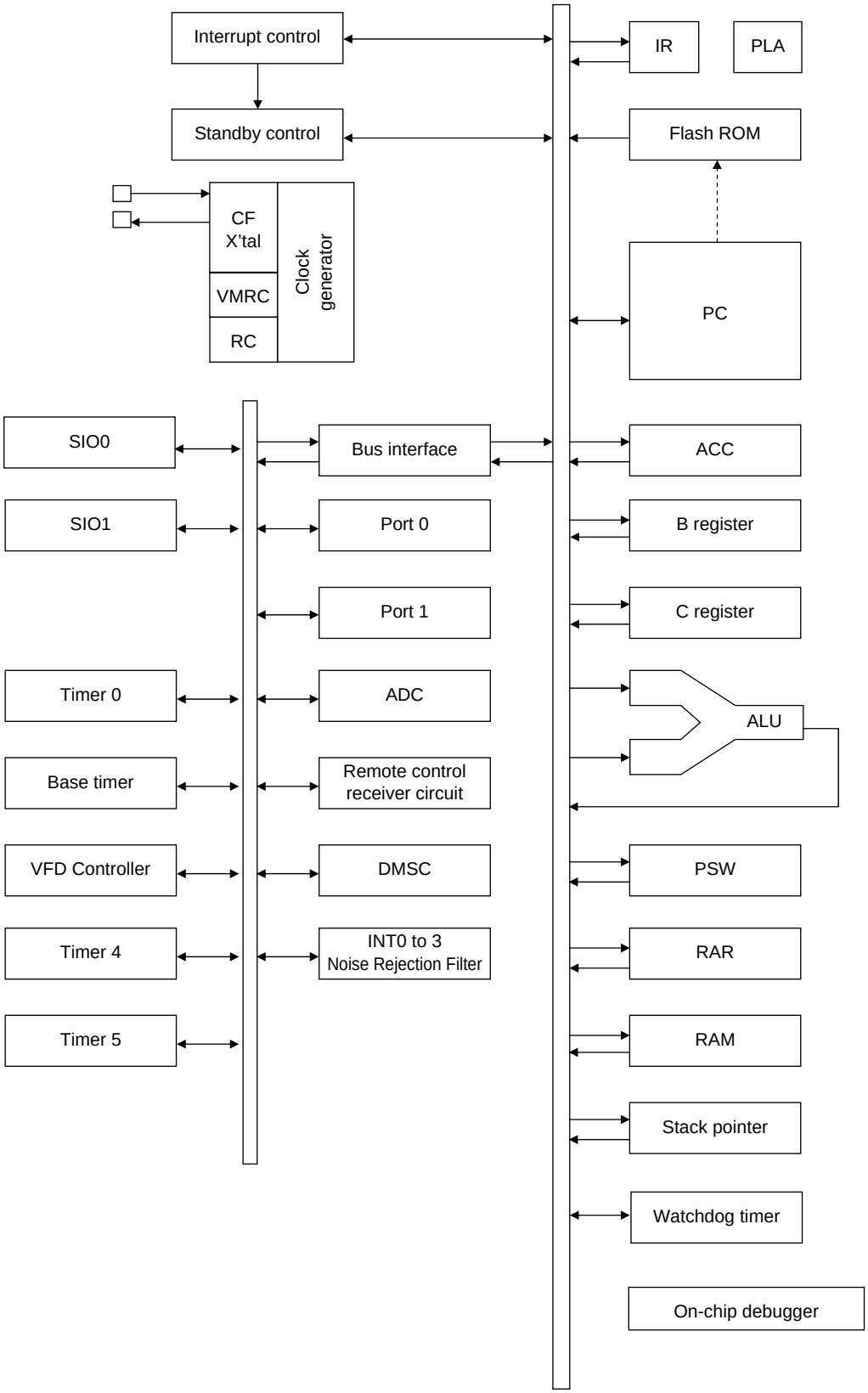


Pin Assignment



SANYO: QFP80(14×14) “Lead-free Type”

System Block Diagram



Pin Description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Option</th></tr>
<tr><td>$V_{SS}1$</td><td>-</td><td>• Power supply (-)</td><td>No</td></tr>
<tr><td>$V_{DD}1$
$V_{DD}2$
$V_{DD}3$</td><td>-</td><td>• Power supply (+)</td><td>No</td></tr>
<tr><td>VP</td><td>-</td><td>• VFD Power supply (-)</td><td>No</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>• 8bit input/output port
• Data direction programmable in nibble units
• Use of pull-up resistor can be specified in nibble units
• Input for HOLD release
• Input for port 0 interrupt
• Other functions
P04: clock output (system clock/can selected from sub clock)
On-chip debugger pins: DBGP0 to DBGP2 (P05 to P07)</td><td>Yes</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>• 8bit input/output port
• Data direction programmable for each bit
• Use of pull-up resistor can be specified for each bit
• Other pin functions
P10: SIO0 data output
P11: SIO0 data input/bus input/output
P12: SIO0 clock input/output
P13: SIO1 data output
P14: SIO1 data input/bus input/output
P15: SIO1 clock input/output
P16: INT2
P17: INT3/Buzzer output
The following types of interrupt detection are possible:
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/
Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>PORT7
P70 to P71</td><td></td><td>• 2bit input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit
• Other functions
P70: INT0 input/HOLD release input/Timer 0L capture input/
output for watchdog timer/Remote control receiver input
P71: INT1 input/HOLD release input/Timer 0H capture input
The following types of interrupt detection are possible:
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/
Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
</table></td><td></td></tr>
<tr><td>S0/T0 to S8/T8</td><td>O</td><td>• Large current output for VFD display controller digit (can be used for segment)</td><td>No</td></tr>
<tr><td>S9/T9 to S15/T15</td><td>O</td><td>• Large current output for VFD display controller segment/digit</td><td>No</td></tr>
<tr><td>S16 to S53</td><td>O</td><td>• Output for VFD display controller segment</td><td>No</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset terminal</td><td>No</td></tr>
<tr><td>CF1/XT1</td><td>I</td><td><ceramic oscillator selected>
• Input terminal for ceramic oscillator
< crystal oscillator selected>
• Input for 32.768kHz crystal oscillation
When not in use, connect to $V_{DD}1$.</td><td>No</td></tr>
<tr><td>CF2/XT2</td><td>O</td><td><ceramic oscillator selected>
• Output terminal for ceramic oscillator
< crystal oscillator selected>
• Output for 32.768kHz crystal oscillation
When not in use, set to oscillation mode and leave open circuit.</td><td>No</td></tr>
</table>

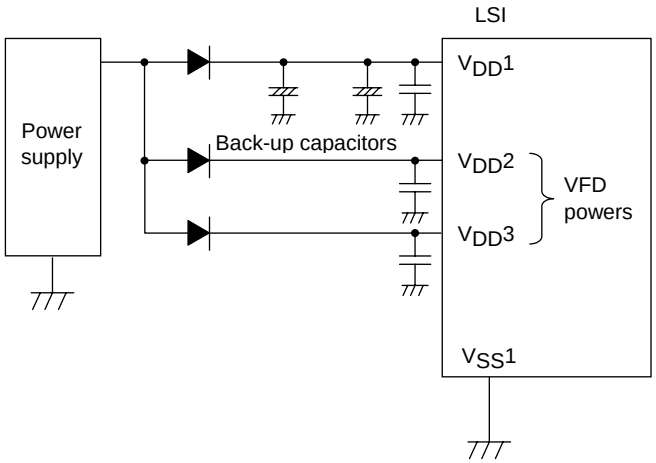
Port Output Types

Output configuration and pull-up/pull-down resistor options are shown in the following table.
Input/output is possible even when port is set to output mode.

Terminal	Option Selected in Units of	Options	Output Format	Pull-up Resistor	Pull-down Resistor
P00 to P07 (Note 1)	each bit	1	CMOS	Programmable	-
		2	Nch-open drain	Programmable	-
P10 to P17	each bit	1	CMOS	Programmable	-
		2	Nch-open drain	Programmable	-
P70	-	None	Nch-open drain	Programmable	-
P71	-	None	CMOS	Programmable	-
S0/T0 to S15/T15 S16 to S53	-	None	High voltage Pch-open drain	-	Fixed

Note 1: Programmable pull-up resisters of Port 0 can be attached in nibble units (P00 to P03, P04 to P07).

* Note: Connect as follows to reduce noise on V_{DD} and increase the back-up time.
$V_{SS}1$ must be connected together and grounded.



Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1$ = 0V

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1$=$V_{DD}2$=$V_{DD}3$		-0.3		+6.5	V
Input voltage		V_I(1)	CF1/XT1, $\overline{RES}$			-0.3		V_{DD}+0.3	
		V_I(2)	VP			V_{DD}-45		V_{DD}+0.3	
Output voltage		V_O(1)	S0/T0 to S15/T15 S16 to S53			V_{DD}-45		V_{DD}+0.3	
		V_O(2)	CF2/XT2			-0.3		V_{DD}+0.3	
Input/Output voltage		V_{IO}(1)	Ports 0, 1, 7			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1	• CMOS output selected • Current at each pin		-10			mA
		IOPH(2)	Port 71	Current at each pin		-5			
		IOPH(3)	S0/T0 to S15/T15	Current at each pin		-30			
		IOPH(4)	S16 to S53	Current at each pin		-15			
	Average output current	IOMH(1)	Ports 0, 1	• CMOS output selected • Current at each pin		-7.5			
		IOMH(2)	Port 71	Current at each pin		-3			
		IOMH(3)	S0/T0 to S15/T15	Current at each pin		-15			
		IOMH(4)	S16 to S53	Current at each pin		-10			
	Total output current	ΣIOAH(1)	Port 0	Total of all pins		-30			
		ΣIOAH(2)	Port 1	Total of all pins		-30			
		ΣIOAH(3)	Ports 0, 1	Total of all pins		-30			
		ΣIOAH(4)	Port 71	Total of all pins		-5			
		ΣIOAH(5)	S0/T0 to S15/T15	Total of all pins		-60			
		ΣIOAH(6)	S16 to S33	Total of all pins		-60			
		ΣIOAH(7)	S0/T0 to S15/T15 S16 to S33	Total of all pins		-60			
		ΣIOAH(8)	S34 to S39	Total of all pins		-60			
		ΣIOAH(9)	S40 to S47	Total of all pins		-60			
		ΣIOAH(10)	S48 to S53	Total of all pins		-60			
		ΣIOAH(11)	S34 to S53	Total of all pins		-60			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1	Current at each pin				20	
		IOPL(2)	Port 7	Current at each pin				10	
	Total output current	IPML(1)	Ports 0, 1	Current at each pin				15	
		IOML(2)	Port 7	Current at each pin				7.5	
	Total output current	ΣIOAL(1)	Port 0	Total of all pins				50	
		ΣIOAL(2)	Port 1	Total of all pins				50	
		ΣIOAL(3)	Port 7	Total of all pins				20	
		ΣIOAL(4)	Ports 0, 1, 7	Total of all pins				80	
Maximum power dissipation		Pd max	QFP80(14×14)	Ta=-40 to +85°C					mW
Operating temperature range		Topr				-40		+85	°C
Storage temperature range		Tstg				-55		+125	

Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage range (Note 2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}3$	0.300µs≤tCYC≤200µs		3.0		5.5	V
	$V_{DD}(2)$		0.735µs≤tCYC≤200µs		2.5		5.5	
Hold voltage	VHD	$V_{DD}1$	RAM and the register data are kept in HOLD mode.		2.0		5.5	
Pull-down supply voltage	VP	VP			-35		V_{DD}	
Input high voltage	$V_{IH}(1)$	Ports 0, 1	Output disable	2.5 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	Port 70 Watchdog timer	Output disable	2.5 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(3)$	XT1/CF1, $\overline{RES}$		2.5 to 5.5	$0.75V_{DD}$		V_{DD}	
Input low voltage	$V_{IL}(1)$	Ports 0, 1 Port 71 Port 70 port input/interrupt	Output disable	2.5 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
	$V_{IL}(2)$	Port 70 Watchdog timer	Output disable	2.5 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(3)$	XT1/CF1, $\overline{RES}$		2.5 to 5.5	V_{SS}		$0.25V_{DD}$	
Operation cycle time	tCYC			3.0 to 5.5	0.300		200	µs
				2.5 to 5.5	0.735		200	
External system clock frequency	FEXCF(1)	CF1	• CF2 open circuit • system clock divider set to 1/1 • external clock DUTY=50±5%	3.0 to 5.5	0.1		10	MHz
				2.5 to 5.5	0.1		4	
			• CF2 open circuit • system clock divider set to 1/2 • external clock DUTY=50±5%	3.0 to 5.5	0.2		20	
				2.5 to 5.5	0.2		8	
Oscillation stabilizing time period (Note 2-2)	FmCF(1)	CF1, CF2	• 10MHz ceramic resonator oscillation • Refer to figure 1	3.0 to 5.5		10		MHz
	FmCF(2)	CF1, CF2	• 4MHz ceramic resonator oscillation • Refer to figure 1	2.5 to 5.5		4		
	FmRC		RC oscillation	2.5 to 5.5	0.3	1.0	2.0	
	FmVMRC		Frequency variable RC oscillation circuit	2.5 to 5.5		4		
	FsX'tal	XT1, XT2	32.768kHz crystal resonator oscillation Refer to figure 2	2.5 to 5.5		32.768		kHz

Note 2-1: Re-writeable on board V_{DD}≥4.5V.

Note 2-2: The oscillation constant is shown in table 1 and table 2.

The CF oscillation terminal and the crystal oscillation terminal cannot be used at the same time because of commonness.

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Input high current	$I_{IH}(1)$	Ports 0, 1, 7	• Output disable • Pull-up resister OFF. • $V_{IN}=V_{DD}$ (including OFF state leak current of the output Tr.)	2.5 to 5.5			1	µA
	$I_{IH}(2)$	$\overline{RES}$	$V_{IN}=V_{DD}$	2.5 to 5.5			1	
	$I_{IH}(3)$	CF1/XT1	$V_{IN}=V_{DD}$	2.5 to 5.5			1	
Input low current	$I_{IL}(1)$	Ports 0, 1, 7	• Output disable • Pull-up resister OFF. • $V_{IN}=V_{SS}$ (including OFF state leak current of the output Tr.)	2.5 to 5.5	-1			
	$I_{IL}(2)$	$\overline{RES}$	$V_{IN}=V_{SS}$	2.5 to 5.5	-1			
	$I_{IL}(3)$	CF1/XT1	$V_{IN}=V_{SS}$	2.5 to 5.5	-1			
Output high voltage	$V_{OH}(1)$	Port 0: CMOS output option Ports 1	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.5mA	3.0 to 5.5	V_{DD}-1			
	$V_{OH}(3)$		I_{OH}=-0.1mA	2.5 to 5.5	V_{DD}-0.5			
	$V_{OH}(4)$	Port 71	I_{OH}=-0.4mA	2.5 to 5.5	V_{DD}-1			
	$V_{OH}(5)$	S0/T0 to S15/T15	I_{OH}=-20.0mA	4.5 to 5.5	V_{DD}-1.8			
	$V_{OH}(6)$		I_{OH}=-10.0mA	3.0 to 5.5	V_{DD}-1.8			
	$V_{OH}(7)$		• I_{OH}=-1.0mA • I_{OH} at any single pin is not over 1mA.	2.5 to 5.5	V_{DD}-1			
	$V_{OH}(8)$	S16 to S53	I_{OH}=-5.0mA	4.5 to 5.5	V_{DD}-1.8			
	$V_{OH}(9)$		I_{OH}=-2.5mA	3.0 to 5.5	V_{DD}-1.8			
	$V_{OH}(10)$		• I_{OH}=-1.0mA • I_{OH} at any single pin is not over 1mA.	2.5 to 5.5	V_{DD}-1			
Output low voltage	$V_{OL}(1)$	Ports 0, 1	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=5mA	3.0 to 5.5			1.5	
	$V_{OL}(3)$		I_{OL}=1.6mA	2.5 to 5.5			0.4	
	$V_{OL}(4)$	Port 7	I_{OL}=1mA	2.5 to 5.5			0.4	
Pull-up resistor	Rpu	Ports 0, 1, 7	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	40	70	kΩ
				2.5 to 4.5	25	70	150	
Output off-leak current	IOFF(1)	S0/T0 to S15/T15, S16 to S53	• Output P-ch Tr. OFF • $V_{OUT}=V_{SS}$	2.5 to 5.5	-1			µA
	IOFF(2)		• Output P-ch Tr. OFF • $V_{OUT}=V_{DD}$-40V	2.5 to 5.5	-30			
Pull-down resistor	Rpd	• S0/T0 to S15/T15 • S16 to S53	• Output P-ch Tr. OFF • V_{OUT}=3V • Vp=-30V	5.0	60	100	200	kΩ
Hysteresis voltage	VHYS(1)	• Ports 0, 1, 7 • $\overline{RES}$		2.5 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	• f=1MHz • All other terminals connected to V_{SS}. • Ta=25°C	2.5 to 5.5		10		pF

Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 6. • (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.	2.5 to 5.5	4/3			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 5.5	0.03			µs
	Data hold time		thDI(1)			2.5 to 5.5	0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.5 to 5.5			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.5 to 5.5			1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)	2.5 to 5.5			(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.5 to 5.5	2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 5.5	0.03			µs
	Data hold time		thDI(2)			2.5 to 5.5	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.5 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P16)	• Interrupt acceptable • Events to timer 0, 1 can be input.	2.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P17) (Noise rejection ratio set to 1/1.)	• Interrupt acceptable • Events to timer 0 can be input.	2.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P17) (Noise rejection ratio set to 1/32.)	• Interrupt acceptable • Events to timer 0 can be input.	2.5 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P17) (Noise rejection ratio set to 1/128.)	• Interrupt acceptable • Events to timer 0 can be input.	2.5 to 5.5	256			
	tPIL(5)	$\overline{RES}$	Reset possible	2.5 to 5.5	200			µs

AD Converter Characteristics at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07)		3.0 to 5.5		8		bit
Absolute precision	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	tCAD		AD conversion time=32×tCYC (ADCR2=0) (Note 6-2)	4.5 to 5.5	15.62 (tCYC= 0.488µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 to 5.5	23.52 (tCYC= 0.735µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time=64×tCYC (ADCR2=1) (Note 6-2)	4.5 to 5.5	18.82 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
				3.0 to 5.5	47.04 (tCYC= 0.735µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Note 6-1: Absolute precision not including quantizing error (±1/2 LSB).

Note 6-2: Conversion time means time from executing AD conversion instruction to loading complete digital value to register.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Current dissipation during basic operation (Note 7-1)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• FmCF=10Hz for ceramic resonator oscillation • System clock: 10MHz • Internal RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		8.0	24	mA
				3.0 to 4.5		6.1	19	
	IDDOP(2)		• CF1=15MHz for external clock • System clock: CF1 oscillation • Internal RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		10.5	32	
				3.0 to 4.5		9.5	28	
	IDDOP(3)		• FmCF=4MHz for ceramic resonator oscillation • System clock: 4MHz • Internal RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		3.8	9.5	
				3.0 to 4.5		3.1	7.8	
	IDDOP(4)		• FmCF=0Hz (No oscillation) • System clock: RC oscillation • Divider set to 1/2	4.5 to 5.5		0.72	3	
				2.5 to 4.5		0.53	2	
	IDDOP(5)		• FsX'tal=32.768kHz for crystal oscillation • System clock: 32.768KHz • Internal RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		39	220	µA
				2.5 to 4.5		25	150	

Note 7-1: The currents of the output transistors and the pull-up MOS transistors are ignored.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Current dissipation HALT mode (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	HALT mode • FmCF=10MHz for Ceramic resonator oscillation • System clock : 10MHz • Internal RC oscillation stopped. • Divider: 1/1	4.5 to 5.5		3.0	9	mA
				3.0 to 4.5		2.1	6.3	
	IDDHALT(2)		HALT mode • CF1=15MHz for external clock • System clock : CF1 oscillation • Internal RC oscillation stopped. • Divider 1/2	4.5 to 5.5		4.2	12.5	
				3.0 to 4.5		2.5	7.8	
	IDDHALT(3)		HALT mode • FmCF=4MHz for Ceramic resonator oscillation • System clock : 4MHz • Internal RC oscillation stopped. • Divider: 1/1	4.5 to 5.5		1.4	3.5	
				2.5 to 4.5		1.0	2.5	
	IDDHALT(4)		HALT mode • FmCF=0Hz (When oscillation stops.) • System clock : RC oscillation • Divider: 1/2	4.5 to 5.5		420	1600	µA
				2.5 to 4.5		280	1100	
	IDDHALT(5)		HALT mode • FsX'tal=32.768kHz for crystal oscillation • Internal RC oscillation stopped. • System clock : 32.768kHz • Divider: 1/2	4.5 to 5.5		24	80	
				2.5 to 4.5		14	60	
Current dissipation HOLD mode	IDDHOLD(1)	$V_{DD}1$	HOLD mode • CF1=V_{DD} or open circuit (when using external clock)	4.5 to 5.5		0.10	20	
				2.5 to 4.5		0.02	15	
Current dissipation Date/time clock HOLD mode	IDDHOLD(2)	$V_{DD}1$	Date/time clock HOLD mode • CF1=V_{DD} or open circuit (when using external clock) • FsX'tal=32.768kHz for crystal oscillation	4.5 to 5.5		21	65	
				2.5 to 4.5		11	50	

Note 7-1: The currents of the output transistors and the pull-up MOS transistors are ignored.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
On-board writing current	IDDFW(1)	$V_{DD}1$	• The current dissipation of the microcomputer is excluded.	4.5 to 5.5		5	10	mA
Writing time	tFW(1)		• Erase time	4.5 to 5.5		20	30	ms
	tFW(2)		• Writing time			40	60	µs

Characteristics of a Sample Main System Clock Oscillation Circuit

The characteristics in the table bellow is based on the following conditions:
1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Frequency	Manufacturer	Oscillator	Circuit Parameters			Operating Supply Voltage Range [V]	Oscillation Stabilizing Time		Notes
			C1 [pF]	C2 [pF]	Rd1 [Ω]		typ [ms]	max [ms]	
10MHz	MURATA	CSTCE10M0G52-R0	10	10	1k	2.8 to 5.5	0.029		
		CSTLS10M0G53-B0	15	15	1k	3.0 to 5.5	0.028		
4MHz	MURATA	CSTCR4M00G53-R0	15	15	2.2k	2.3 to 5.5	0.034		
		CSTLS4M00G53-B0	15	15	2.2k	2.3 to 5.5	0.030		

The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (Refer to Figure 4)

Characteristics of a Sample Subsystem Clock Oscillator Circuit

The characteristics in the table bellow is based on the following conditions:
1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Frequency	Manufacturer	Oscillator	Circuit Parameters				Operating Supply Voltage Range [V]	Oscillation Stabilizing Time		Notes
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [s]	max [s]	

The oscillation stabilizing time is a period until the oscillation becomes stable after executing the instruction which starts the sub-clock oscillation or after releasing the HOLD mode. (Refer to Figure 4)

Notes: Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

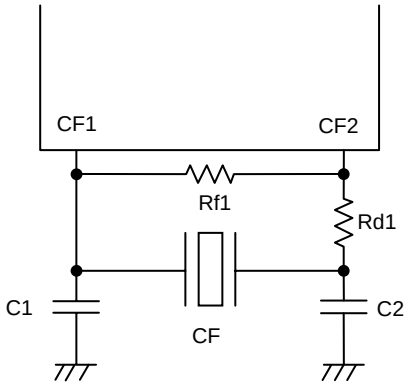


Figure 1 Ceramic Oscillation Circuit

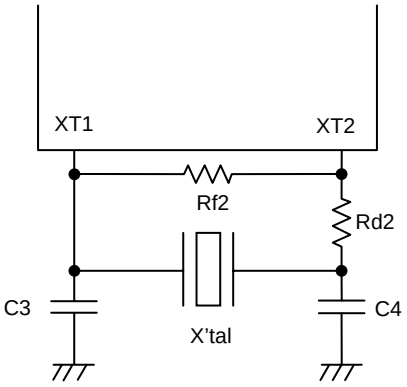


Figure 2 Crystal Oscillation Circuit

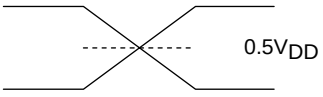
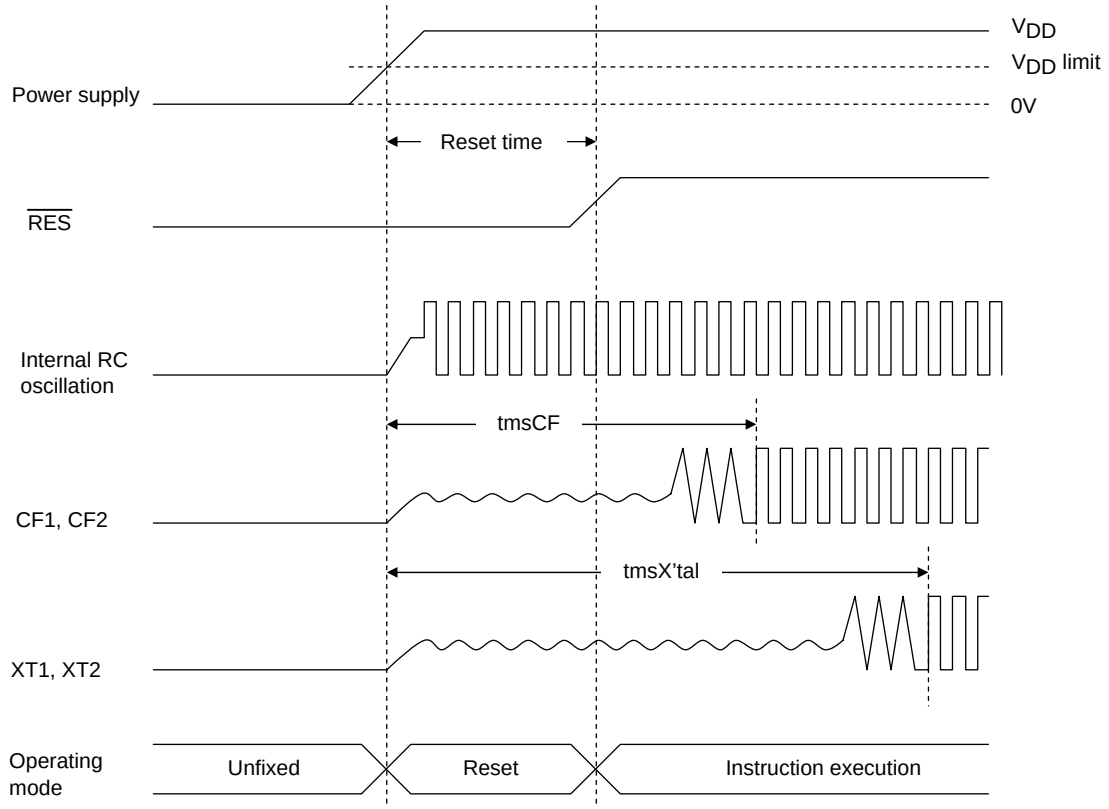
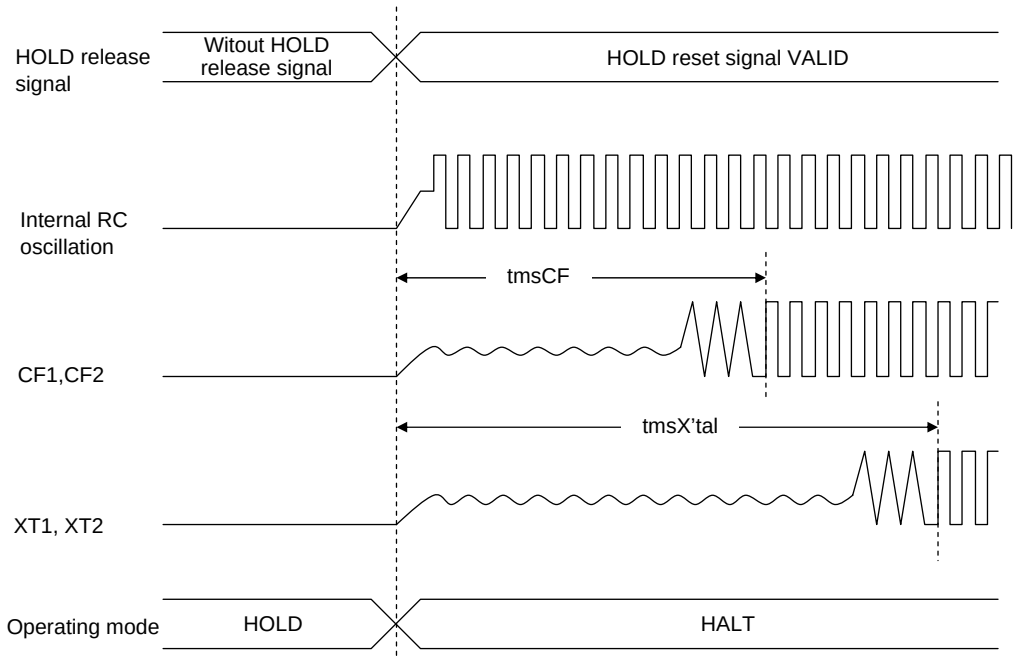


Figure 3 AC Timing Measurement Point

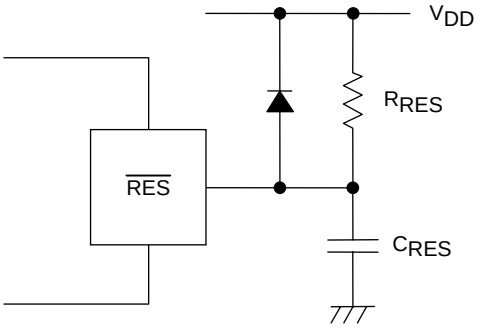


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



Note:
Set C_{RES}, R_{RES} values such that reset time exceeds 200μs.

Figure 5 Reset Circuit

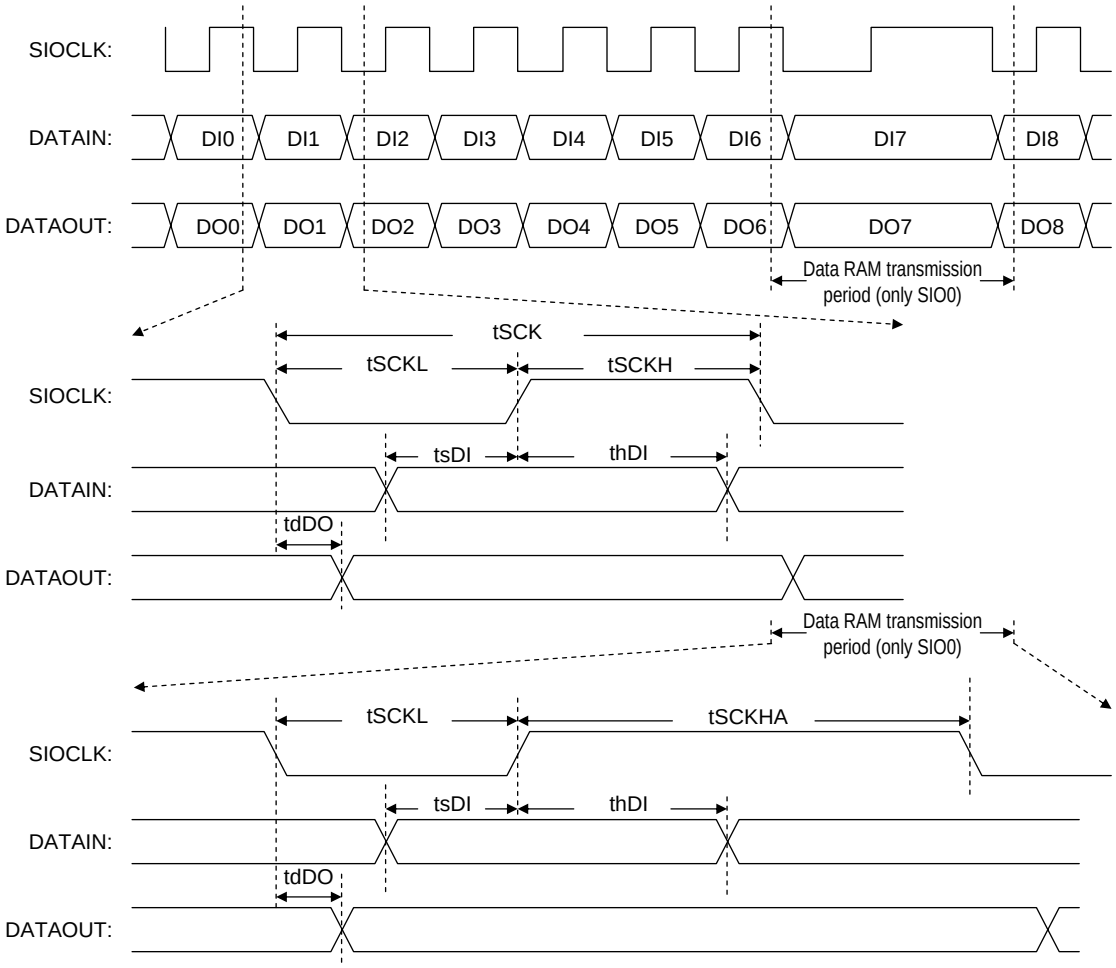


Figure 6 Serial I/O Waveform

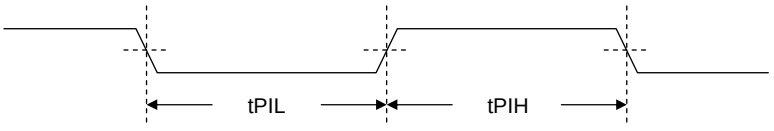


Figure 7 Pulse Input Timing Signal Waveform