No. *5601

LC82151

Single-Chip Facsimile Controller

Preliminary

Overview

The LC82151 is a facsimile controller that integrates the main functions required by facsimile systems on a single chip. The LC82151 includes a FAX modem with ADPCM and HDLC functions, image processing functions that can create high-quality binary image data without external memory, a CODEC accelerator, a CPU and CPU peripheral circuits, general-purpose I/O ports, and other functions. A facsimile system with excellent cost-performance characteristics can be created easily by providing ROM and RAM.
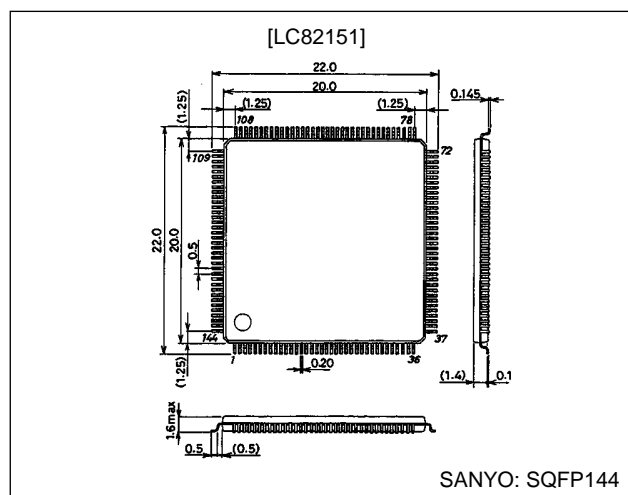
Functions

- CPU and peripheral circuits
  - High-speed 16-bit CPU (65C816) operating at 7.4 MHz
  - 16-MB program address space
  - CODEC accelerator
  - Two-channel DMA controller
  - Four 16-bit timers
  - 16-bit watchdog timer
  - TPH interface
  - Serial I/O interface
  - Parallel I/O: 10 to 43 pins
- Image processing
  - Processes 2048 pixels per line
  - Processing speed: 540 ns per pixel (maximum)
  - Built-in 8-bit A/D converter (Includes a sensor signal delay function.)
  - Sensor drive circuit (Supports CCDs and all major CIS devices.)
  - Distortion correction (White distortion: 8-pixel averaging correction, black correction: Allows the black correction subtraction data to be set.)
  - γ-correction (Supports user-defined correction curves.)
  - Simple binary conversion processing (fixed threshold and density-adaptive threshold)
  - Halftone processing error diffusion method (64 levels)
  - Image reduction (decimation, fine black line retention, and fine white line retention)

- Modem
  - Group 3 FAX modem
    - ITU-T V.29 (9600, 7200, and 4800 bps)
    - ITU-T V.27ter (4800 and 2400 bps)
    - ITU-T V.21ch2 (300 bps)
  - Simultaneous high/low-speed wait function
  - Short training function (ITU-T V.27ter only)
  - HDLC function (for all transmission speeds)
  - Synthesizer function
  - Caller ID function
    - Bell 202 (1200 bps)
    - ITU-T V.23 (1200 bps)
  - ADPCM function
    - Encoding: 2, 3, or 4 bits
    - Sampling frequencies: 9.6, 7.2, 4.8, and 3.6 kHz
  - RTC low-voltage backup
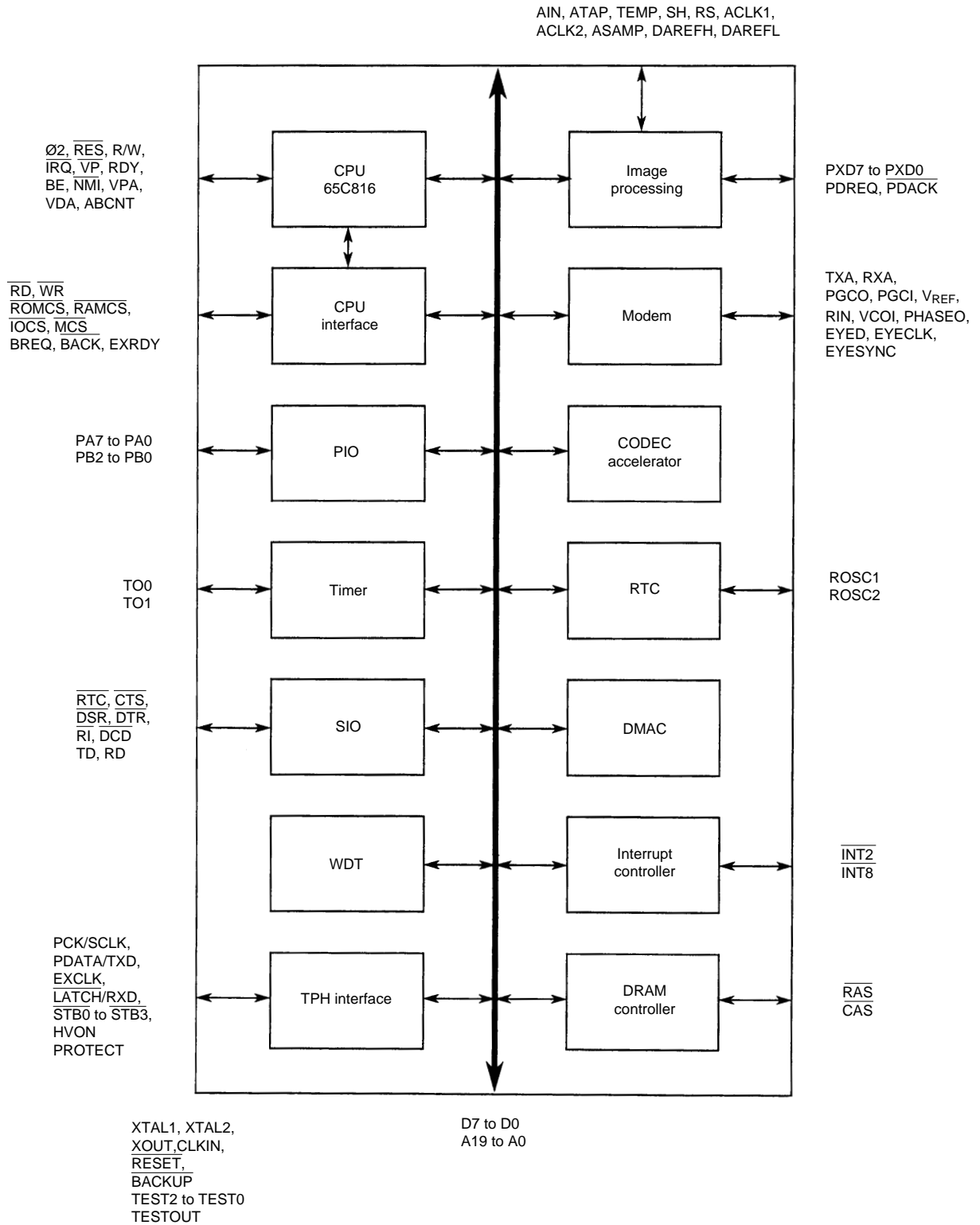 - 5-V single-voltage power supply

Package Dimension

unit: mm

3214-SQFP144

[LC82151]

SANYO: SQFP144

Block Diagram

AIN, ATAP, TEMP, SH, RS, ACLK1,
ACLK2, ASAMP, DAREFH, DAREFL

Ø2, $\overline{RES}$, R/W,
$\overline{IRQ}$, $\overline{VP}$, RDY,
BE, $\overline{NMI}$, VPA,
VDA, ABCNT

| CPU 65C816 | Image processing |

PXD7 to PXD0
PDREQ, PDACK

$\overline{RD}$, $\overline{WR}$
$\overline{ROMCS}$, $\overline{RAMCS}$,
$\overline{IOCS}$, $\overline{MCS}$
BREQ, BACK, EXRDY

| CPU interface | Modem |

TXA, RXA,
PGCO, PGCI, V_{REF},
RIN, VCOI, PHASEO,
EYED, EYECLK,
EYESYNC

PA7 to PA0
PB2 to PB0

| PIO | CODEC accelerator |

TO0
TO1

| Timer | RTC |

ROSC1
ROSC2

$\overline{RTC}$, $\overline{CTS}$,
$\overline{DSR}$, $\overline{DTR}$,
RI, DCD
TD, RD

| SIO | DMAC |

| WDT | Interrupt controller |

$\overline{INT2}$
INT8

PCK/SCLK,
PDATA/TXD,
EXCLK,
$\overline{LATCH}$/RXD,
$\overline{STB0}$ to $\overline{STB3}$,
HVON
PROTECT

| TPH interface | DRAM controller |

$\overline{RAS}$
CAS

XTAL1, XTAL2,
XOUT,CLKIN,
$\overline{RESET}$,
BACKUP
TEST2 to TEST0
TESTOUT

D7 to D0
A19 to A0

Pin Assignment

Type					
I	Input pins	B	Bidirectional pins	NC	No connection
O	Output pins	P	Power pins		

Pin No.	Pin	I/O	Pin function
1	V_{SS}	P	Ground
2	$\overline{VP}$	I	ICE vector address signal
3	RDY	O	ICE ready signal
4	VPA	I	ICE valid program address signal
5	VDA	I	ICE valid data address signal
6	A19	O	
7	A18	O	
8	A17	O	Address bus
9	A16	O	
10	D7	B	
11	D6	B	
12	D5	B	
13	D4	B	
14	D3	B	Data bus
15	D2	B	
16	D1	B	
17	D0	B	
18	V_{DD}	P	Power supply
19	V_{SS}	P	Ground
20	$\overline{RD}$	O	Read signal from the CPU
21	$\overline{WR}$	O	Write signal from the CPU
22	$\overline{ROMCS}$	O	Program ROM chip select signal
23	$\overline{RAMCS}$	O	Working RAM chip select signal
24	$\overline{IOCS}$	O	External I/O chip select signal
25	$\overline{MCS}$	O	External I/O chip select signal
26	$\overline{RAS}$/PG1	B	DRAM row address strobe/general-purpose port G
27	$\overline{CAS}$/PG2	B	DRAM column address strobe/general-purpose port G
28	PA7	B	
29	PA6	B	
30	PA5	B	
31	PA4	B	
32	PA3	B	General-purpose port A
33	PA2	B	
34	PA1	B	
35	PA0	B	
36	V_{SS}	P	Ground
37	V_{DD}	P	Power supply
38	RIN	I	PLL bias input
39	PHASEO	O	PLL phase detector output
40	VCOI	I	PLL voltage-controlled oscillator input
41	$\overline{INT8}$/PB7	B	External interrupt request signal/general-purpose port B
42	$\overline{INT2}$/PB6	B	
43	$\overline{BACK}$/PB5	B	CPU bus acknowledge signal/general-purpose port B
44	BREQ/PB4	B	CPU bus request signal/general-purpose port B
45	EXRDY/PB3	B	External ready input/general-purpose port B
46	PB2	B	
47	PB1	B	General-purpose port B
48	PB0	B	
49	$\overline{NMI}$	I	Non-maskable interrupt request signal
50	TEST2	I	Test pin

Continued from preceding page.

Pin No.	Pin	I/O	Pin function
51	TEST1	I	Test pins
52	TEST0	I	
53	TESTOUT	I	
54	V$_{DD}$	P	Power supply
55	V$_{SS}$	P	Ground
56	ROSC1	I	RTC crystal oscillator connections
57	ROSC2	O	
58	$\overline{BACKUP}$	I	Low power mode input
59	$\overline{RESET}$	I	System reset signal
60	AV$_{DD}$	P	Analog system power supply
61	AV$_{SS}$	P	Analog system ground
62	AIN	I	Sensor signal input
63	TEMP	I	Thermistor input
64	ATAP	O	A/D converter reference voltage output
65	DAREFH	I	D/A converter high-level reference voltage input
66	DAREFL	I	D/A converter low-level reference voltage input
67	TXA	O	Modem analog transmit output
68	RXA	I	Modem analog receive input
69	PGCO	O	Modem gain adjustment output
70	PGCI	I	Modem gain adjustment input
71	V$_{REF}$	I	Modem analog block reference input
72	V$_{SS}$	P	Ground
73	V$_{DD}$	P	Power supply
74	SH	O	Image sensor start pulse
75	RS	O	Image sensor reset pulse
76	ACLK1	O	Image sensor data transfer clocks
77	ACLK2	O	
78	ASAMP	O	Built-in A/D converter sampling point monitor signal
79	PXD7/PC7	B	Image data output/general-purpose port C
80	PXD6/PC6	B	
81	PXD5/PC5	B	
82	PXD4/PC4	B	
83	PXD3/PC3	B	
84	PXD2/PC2	B	
85	PXD1/PC1	B	
86	PXD0/PC0	B	
87	PDREQ/PF7	B	Image data DMA request signal/general-purpose port F
88	$\overline{PDACK}$/PF6	B	Image data DMA acknowledge signal/general-purpose port F
89	EYED/PF5	B	Eye pattern data output/general-purpose port F
90	V$_{DD}$	P	Power supply
91	V$_{SS}$	P	Ground
92	EYECLK/PF4	B	Eye pattern data clock/general-purpose port F
93	EYESYNC/PF3	B	Eye pattern data synchronizing signal/general-purpose port F
94	TO1/PF2	B	Timer outputs/general-purpose port F
95	TO0/PF1	B	
96	PCK/SCLK/PE7	B	Thermal head data transfer clock/serial I/O clock/general-purpose port E
97	PDATA/TXD/PE6	B	Thermal head serial output data/serial I/O send data/general-purpose port E
98	EXCLK/PE5	B	Thermal head control external clock/general-purpose port E
99	$\overline{LATCH}$/RXD/PE4	B	Thermal head data latch signal/serial I/O receive data/general-purpose port E
100	$\overline{STB3}$/PE3	B	Thermal head strobe signal/general-purpose port E
101	$\overline{STB2}$/PE2	B	
102	$\overline{STB1}$/PE1	B	
103	$\overline{STB0}$/PE0	B	
104	HVON/PF0	B	Head power on/off control signal/general-purpose port F
105	PROTECT/PG0	B	Head protection abnormality indication signal input/general-purpose port G

Continued from preceding page.

Pin No.	Pin	I/O	Pin function
106	XTAL1	I	System clock crystal oscillator element connection (29.4912 MHz)
107	XTAL2	O	
108	V_{SS}	P	Ground
109	V_{DD}	P	Power supply
110	XOUT	O	Crystal oscillator clock output
111	CLKIN	I	System clock input
112	A15	B	Address bus
113	A14	B	
114	A13	B	
115	A12	B	
116	A11	B	
117	A10	B	
118	A9	B	
119	A8	B	
120	TD/PD7	B	Serial port transmit data output/general-purpose port D
121	RD/PD6	B	Serial port receive data input/general-purpose port D
122	$\overline{RTS}$/PD5	B	Request to send signal/general-purpose port D
123	$\overline{CTS}$/PD4	B	Clear to send signal/general-purpose port D
124	$\overline{DSR}$/PD3	B	Data set ready/general-purpose port D
125	$\overline{DTR}$/PD2	B	Data terminal ready/general-purpose port D
126	V_{DD}	P	Power supply
127	V_{SS}	P	Ground
128	$\overline{RI}$/PD1	B	Ring indicator/general-purpose port D
129	$\overline{DCD}$/PD0	B	Data carrier detect/general-purpose port D
130	A7	B	Address bus
131	A6	B	
132	A5	B	
133	A4	B	
134	A3	B	
135	A2	B	
136	A1	B	
137	A0	B	
138	ABCNT	O	ICE bus control signal
139	BE	O	ICE bus enable signal
140	ø2	O	ICE system clock
141	$\overline{RES}$	O	ICE reset signal
142	RWB	I	ICE read/write signal
143	$\overline{IRQ}$	O	ICE interrupt request signal
144	V_{DD}	P	Power supply

Sample Application

Document

Fluorescent lamp

Stepping motor

Lens   Image sensor

Motor driver

Temperature sensor

Cutter

Thermal head

Stepping motor   Paper

Facsimile controller

LC82151

NCU

Public telephone network

Telephone

RAM

ROM

To LCD

To key matrix
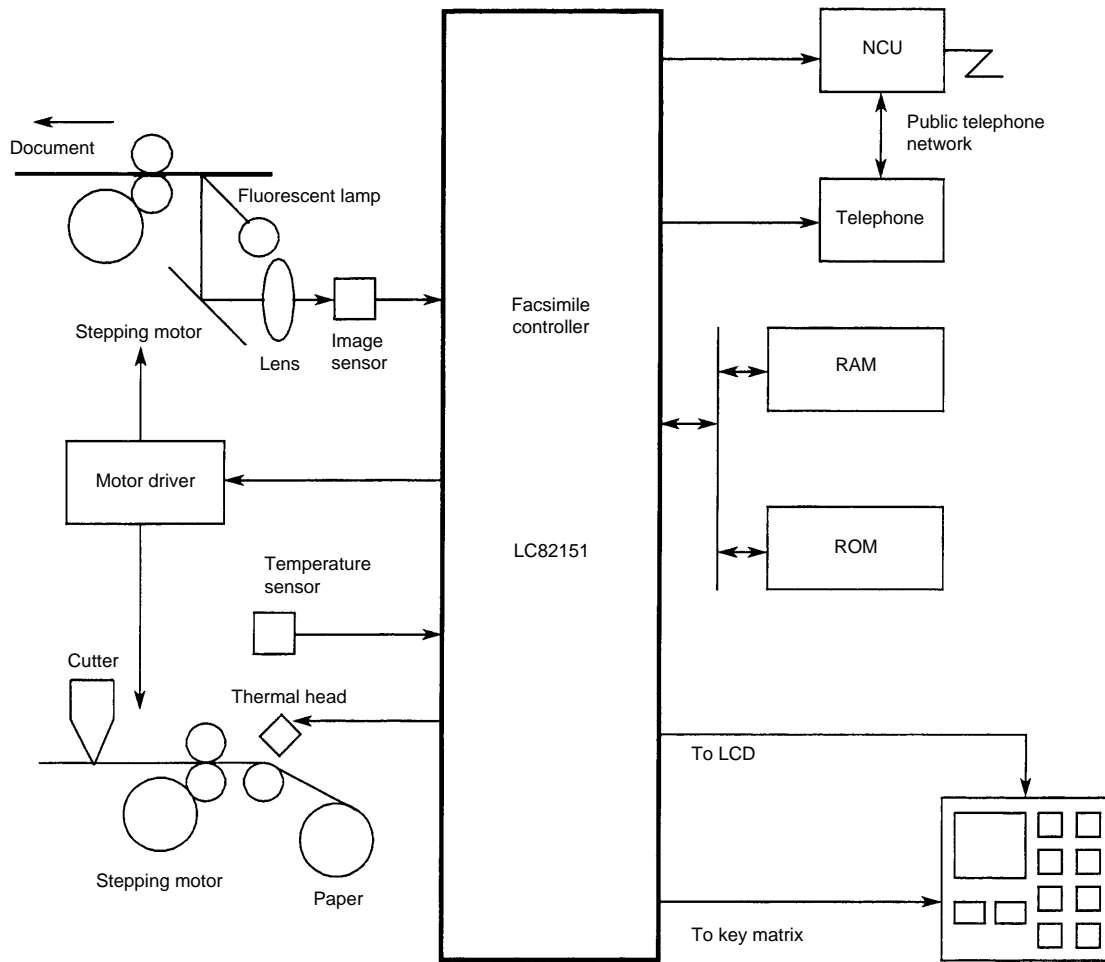
Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		−0.3 to +7.0	V
Input and output voltage	V_I, V_O		−0.3 to V_{DD} +0.3	V
Allowable power dissipation	Pd max	Ta 70°C	550	mW
Operating temperature	Topr		−30 to +70	°C
Storage temperature	Tstg		−55 to +125	°C
Soldering temperature		Manual soldering (3 seconds)	350	°C
		Reflow soldering (10 seconds)	235	°C

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5		5.5	V
Input voltage	V_{IN}		0		V_{DD}	V

Electrical Characteristics at Ta = –30 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	V_{IH1}		2.2			V
Input low-level voltage	V_{IL1}				0.8	V
Input leakage current	I_L		−10		+10	µA
Output high-level voltage	V_{OH}	I_{OH} = −4mA	2.4			V
Output low-level voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Output leakage current	I_{OZ}	When outputs are high impedance	−10		+10	µA
Charge pump output current	I_{POZ}	PHASEO = 2 V	7	15	27	mA
	I_{NOZ}	PHASEO = 2 V	−8	−15	−28	mA
Vref input voltage	V_{REF}	VREF		V_{DD}/2		V
Vref impedance	V_{REF}	VREF	1			M
Input voltage range	V_{IA}	RXA, PGCI	$V_{DD} \times 0.2$		$V_{DD} \times 0.8$	V
Operating voltage range	V_{OA}	TXA, PGCO	$V_{DD} \times 0.2$		$V_{DD} \times 0.8$	V
Output impedance	R_O	TXA, PGCO			7.0	k
Oscillator frequency	f_{CLK1}	XTAL1, XTAL2, CLKIN		29.4912		MHz
	f_{CLK2}	ROSC1, ROSC 2		32.768		kHz
Current drain	I_{DD1}	Operating		100		mA
	I_{DD2}	In backup mode, V_{DD} = 2.5 V, $\overline{BACKUP}$ = 0		5		µA

Power on Timing

Applications must control the timing of the power on sequence carefully. Although AV_{SS} and V_{SS} are completely isolated internally in the LC82151, AV_{DD} and V_{DD} are connected through the substrate. This means that there must be no potential difference between AV_{DD} and V_{DD}. Also, the power supply voltage rise and fall times must be under 3 ms.

Analog Characteristic

D/A Converter

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Resolution				6		bit
Reference resistors value		DAREFL, DAREFH		5.0		k

A/D Converter at an ATAP potential of 4.2 V

A/D Converter

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Resolution				8		bit
Linearity error					±1	LSB
Differential linearity error					±1	LSB