Ordering number : ENA1419

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LC79401KNE — CMOS LSI Dot-Matrix LCD Drivers

Overview

The LC79401KNE is a 80-outputs segment driver LSI for graphic dot-matrix liquid crystal display systems. The LC79401KNE latches 80 bits of display data sent from a controller using a 4-bit parallel transfer technique and generates LCD drive signals. When combined as a kit with common driver, either the LC79430KNE (QIP100E), the LC79401KNE can drive large screen LCD panels.

Features

- Incorporates LCD drive circuits for 80 bits of display.
- Supports display duties from 1/64 to 1/256
- The provision of a chip disable pin supports power reduction in large-scale panels.
- Allows external provision of the bias power supply
- Operating supply voltage/operating temperature
  V_{DD} (logic block) : 2.7 to 5.5V/-20 to +85°C
  V_{DD}-V_{EE} (LCD block) : 12 to 32V/-20 to +85°C
- Data transfer clock : 6.0MHz (max), bidirectional shifting supported
- Data input : 4-bit parallel input
- CMOS process
- 100-pin flat plastic package (QIP100E)

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Specifications

Absolute Maximum Ratings at Ta = 25±2°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage (Logic)	V_{DD} max		-0.3 to +7.0	V
Maximum supply voltage (LCD)	V_{DD}-V_{EE} max	*1	0 to 35	V
Maximum input voltage	V_I max		-0.3 to V_{DD}+0.3	V
Storage temperature	Tstg		-40 to +125	°C

Note *1 $V_{DD} \geq V1 > V3 > V4 > V_{EE}$, V_{DD}-V3≤7V, V4-V_{EE}≤7V

Allowable Operating Ranges at Ta = -20 to +85°C, V_{SS} = 0V

Parameter	Symbol	Conditions		min	typ	max	unit
Supply voltage (Logic)	V_{DD}			2.7		5.5	V
Supply voltage (LCD)	V_{DD}-V_{EE}	*2, 3		12		32	V
Input high level voltage	V_{IH}	DI1 to DI4, CP, LOAD, CDI, R/L, M, $\overline{\text{DISPOFF}}$		0.8V_{DD}			V
Input low level voltage	V_{IL}	DI1 to DI4, CP, LOAD, CDI, R/L, M, $\overline{\text{DISPOFF}}$				0.2V_{DD}	V
CP Shift clock	f_{CP}	CP				6.0	MHz
CP pulse width	t_{WC}	CP		50			ns
LOAD pulse width	t_{WL}	LOAD		50			ns
Setup time	t_{SETUP}	DI1 to DI4 → CP		30			ns
Hold time	t_{HOLD}	DI1 to DI4 → CP	V_{DD}=2.7 to 4.5V	40			ns
			V_{DD}=4.5 to 5.5V	30			ns
CP → LOAD	t_{CL}	CP → LOAD		80			ns
LOAD → CP	t_{LC1}	LOAD → CP		110			ns
	t_{LC2}	LOAD → CP	V_{DD}=2.7 to 4.5V	30			ns
			V_{DD}=4.5 to 5.5V	15			ns
CP and LOAD rise time	t_R	CP, LOAD				*4	ns
CP and LOAD fall time	t_F	CP, LOAD				*4	ns

Note *2 $V_{DD} \geq V1 > V3 > V4 > V_{EE}$, V_{DD}-V3≤7V, V4-V_{EE}≤7V

*3 When the power is turned on, either the logic system power must be turned on before the LCD drive system power or else they must both be turned on at the same time. When the power is turned off, either the LCD drive system power must be turned off before the logic system power, or else both must be turned off at the same time.

*4 The CP and LOAD rise time (t_R) and the CP and LOAD fall time (t_F) must satisfy equations (1) and (2) below at the same time.

$$(1)\ t_R,\ t_F < \frac{1}{2f_{CP}} - t_{WC} \qquad (2)\ t_R,\ t_F < 50\text{ns}$$

Electrical Characteristics at Ta = 25±2°C, V_{DD} = 2.7 to 5.5V

Parameter	Symbol	Conditions	min	typ	max	unit
Input high level current	I_{IH}	$V_{IN}=V_{DD}$, LOAD, CP, CDI, R/L, DI1 to DI4, M, $\overline{DISPOFF}$			1	μA
Input low level current	I_{IL}	$V_{IN}=V_{SS}$, LOAD, CP, CDI, R/L, DI1 to DI4, M, $\overline{DISPOFF}$	-1			μA
Output high level voltage	V_{OH}	I_{OH}=-400μA, CDO	V_{DD}-0.4			V
Output low level voltage	V_{OL}	I_{OL}=400μA, CDO			0.4	V
Driver on resistance	R_{ON}(1)	$V_{DD}-V_{EE}$=30V, $\lvert V_{DE}-V_O \rvert$=0.5V: O1 to O80 *5		0.6	1.5	kΩ
	R_{ON}(2)	$V_{DD}-V_{EE}$=20V, $\lvert V_{DE}-V_O \rvert$=0.5V: O1 to O80 *5		0.7	2.0	kΩ
Standby current drain	I_{ST}	CDI=V_{DD}, $V_{DD}-V_{EE}$=30V, CP=6.0MHz, Output unloaded: V_{SS}			200	μA
Operating current drain	I_{SS} *6	$V_{DD}-V_{EE}$=30V, CP=6MHz, LOAD=14kHz, M=35Hz: V_{SS}			4.0	mA
	I_{EE} *7	$V_{DD}-V_{EE}$=30V, CP=6MHz, LOAD=14kHz, M=35Hz: V_{EE}			0.5	mA
Input capacitance	C_I	f=6.0MHz ; CP		8		pF

Note *5 V_{DE} = one of V1, V3, V4 or V_{EE}, V1 = V_{DD}, V3 = 15/17 (V_{DD}-V_{EE}), V4 = 2/17 (V_{DD}-V_{EE})

*6 I_{SS} is the current flowing from V_{DD} to V_{SS}

*7 I_{EE} is the current flowing from V_{DD} to V_{EE}

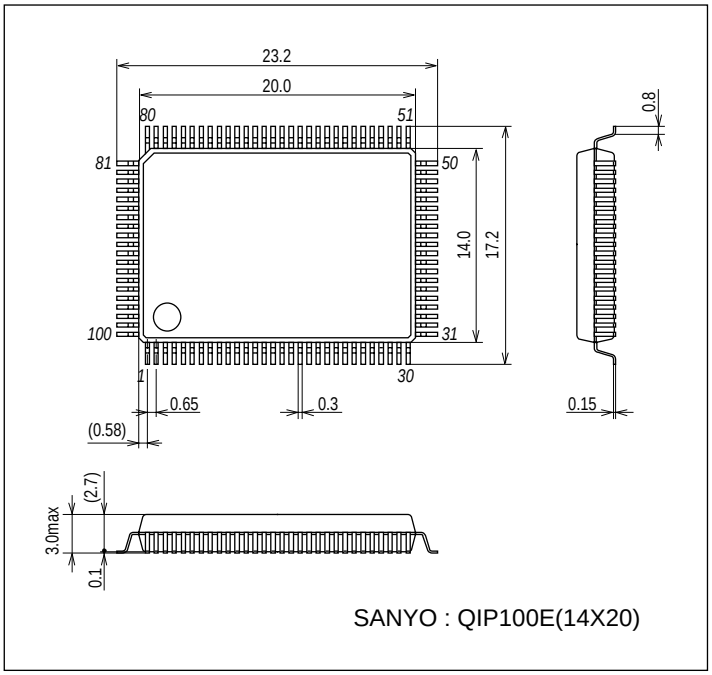
Switching Characteristics at Ta = 25±2°C, V_{SS} = 0V, V_{DD} = 2.7 to 5.5V

Parameter	Symbol	Conditions		min	typ	max	unit
Output delay time 1	t_{D1}	Load=15pF: CDO	V_{DD}=2.7 to 4.5V			100	ns
			V_{DD}=4.5 to 5.5V			80	ns
Output delay time 2	t_{D2}	Load=15pF: CDO	V_{DD}=2.7 to 4.5V			100	ns
			V_{DD}=4.5 to 5.5V			80	ns

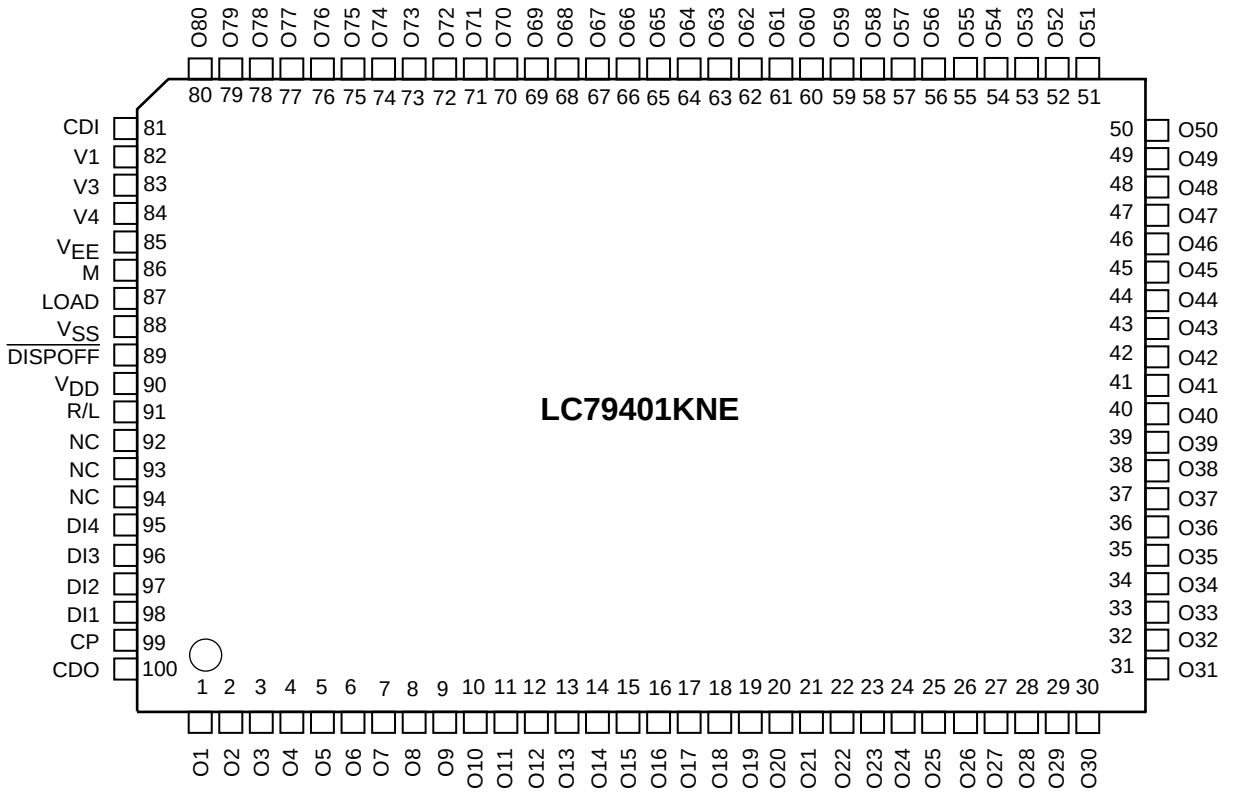
Package Dimensions

unit:mm (typ)

3151A

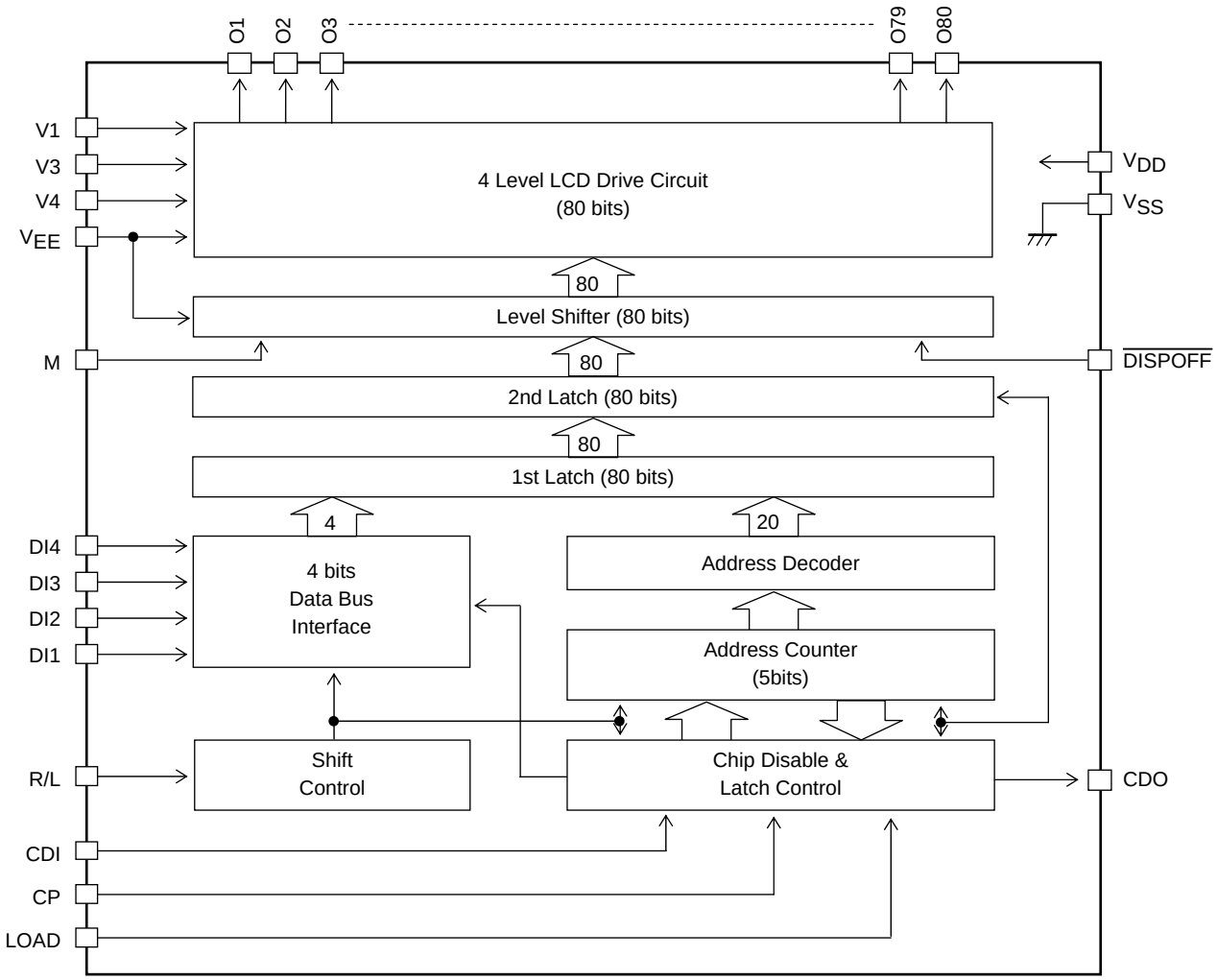


Pin Assignment



Top view

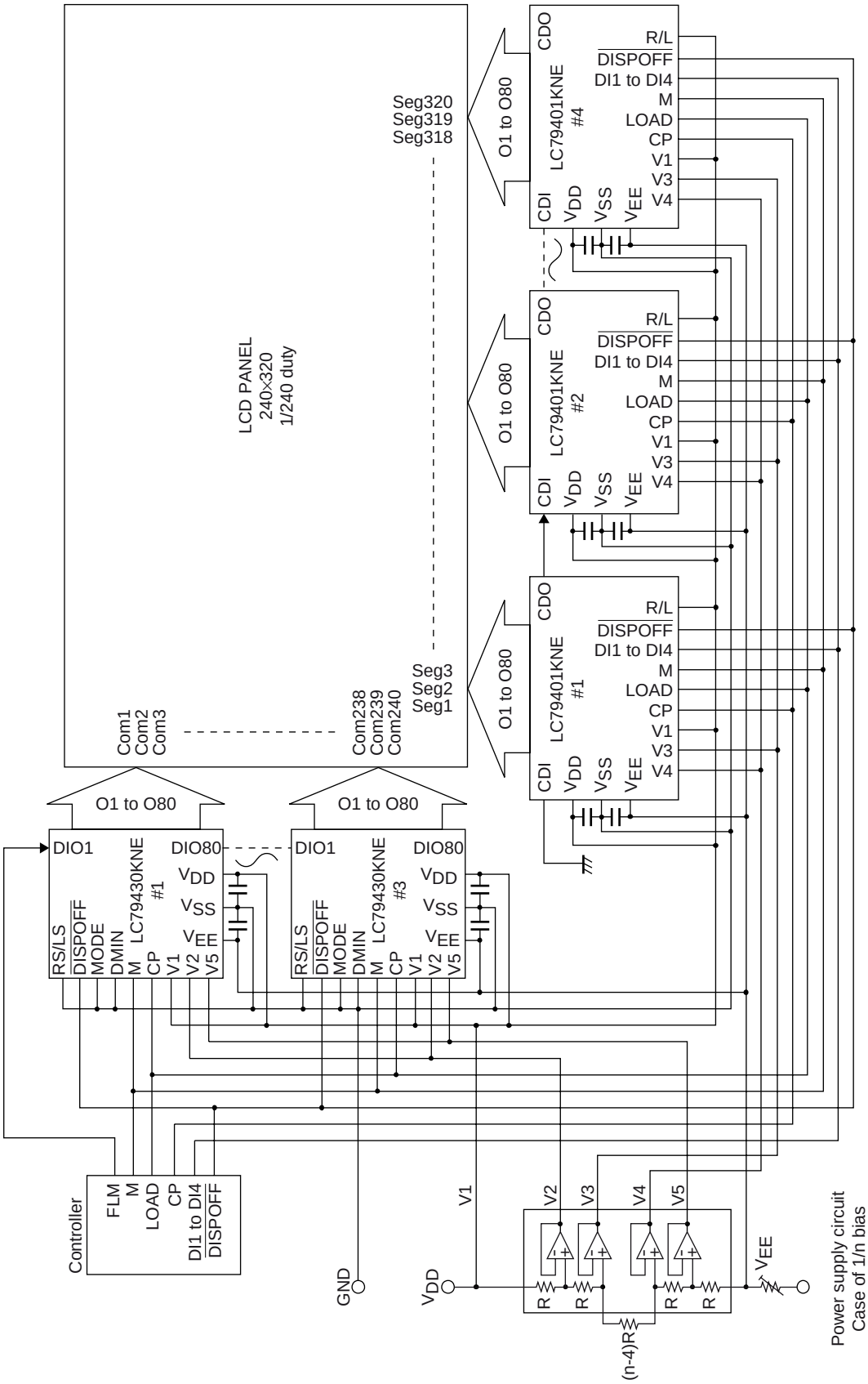
Equivalent Circuit Block Diagram



Pin Function

<table>
<tr><th>Pin No</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>90
88
85</td><td>V_{DD}
V_{SS}
V_{EE}</td><td>Supply</td><td>V_{DD}-V_{SS} : Logic power supply
V_{DD}-V_{EE} : LCD drive circuit power supply</td></tr>
<tr><td>82
83
84</td><td>V1
V3
V4</td><td>Supply</td><td>LCD drive level power supply
V1,V_{EE} : Selected level
V3,V4 : Unselected level</td></tr>
<tr><td>99</td><td>CP</td><td>I</td><td>Display data acquisition clock (falling edge trigger)</td></tr>
<tr><td>87</td><td>LOAD</td><td>I</td><td>Display data latch clock (falling edge trigger)
The display data LCD drive signal is output on the falling edge.</td></tr>
<tr><td>95
96
97
98</td><td>DI4
DI3
DI2
DI1</td><td>I</td><td><table><tr><th>Display data</th><th>LCD drive output</th><th>LCD display</th></tr><tr><td>H</td><td>Selected level</td><td>On</td></tr><tr><td>L</td><td>Unselected level</td><td>Off</td></tr></table></td></tr>
<tr><td>91</td><td>R/L</td><td>I</td><td>Control pin that inverts the data output destination<table><tr><th rowspan="2">R/L</th><th rowspan="2">Data input</th><th colspan="7">Number of clock</th></tr><tr><th>1</th><th>2</th><th>3</th><th>…</th><th>18</th><th>19</th><th>20</th></tr><tr><td rowspan="4">L</td><td>DI1</td><td>O77</td><td>O73</td><td>O69</td><td>…</td><td>O9</td><td>O5</td><td>O1</td></tr><tr><td>DI2</td><td>O78</td><td>O74</td><td>O70</td><td>…</td><td>O10</td><td>O6</td><td>O2</td></tr><tr><td>DI3</td><td>O79</td><td>O75</td><td>O71</td><td>…</td><td>O11</td><td>O7</td><td>O3</td></tr><tr><td>DI4</td><td>O80</td><td>O76</td><td>O72</td><td>…</td><td>O12</td><td>O8</td><td>O4</td></tr><tr><td rowspan="4">H</td><td>DI1</td><td>O4</td><td>O8</td><td>O12</td><td>…</td><td>O72</td><td>O76</td><td>O80</td></tr><tr><td>DI2</td><td>O3</td><td>O7</td><td>O11</td><td>…</td><td>O71</td><td>O75</td><td>O79</td></tr><tr><td>DI3</td><td>O2</td><td>O6</td><td>O10</td><td>…</td><td>O70</td><td>O74</td><td>O78</td></tr><tr><td>DI4</td><td>O1</td><td>O5</td><td>O9</td><td>…</td><td>O69</td><td>O73</td><td>O77</td></tr></table></td></tr>
<tr><td>86</td><td>M</td><td>I</td><td>LCD drive output alternation signal</td></tr>
<tr><td>81</td><td>CDI</td><td>I</td><td>Chip disable pin
High level : Data is not acquired.
Low level : Data is acquired</td></tr>
<tr><td>100</td><td>CDO</td><td>O</td><td>Connect to the CDI pin on the next chip when cascade connection is used.</td></tr>
<tr><td>89</td><td>$\overline{\text{DISPOFF}}$</td><td>I</td><td>Input that controls the O1 to O80 output pins. During periods when this pin
Is low, the O1 to O80 output pins output the V1 level. See the truth table.</td></tr>
<tr><td>1 to 80</td><td>O1 to O80</td><td>O</td><td>LCD drive outputs
The output level are determined by the combination of the output the data,
The M signal, and The $\overline{\text{DISPOFF}}$ pin as shown in the table.<table><tr><th>M</th><th>Q</th><th>$\overline{\text{DISPOFF}}$</th><th>Output</th></tr><tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V1</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V4</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V_{EE}</td></tr><tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr></table>Note : don’t care (fixed at high or low)</td></tr>
<tr><td>92
93
94</td><td>NC
NC
NC</td><td>-</td><td>Must be left open.</td></tr>
</table>

Application Example (LC79401KNE/LC79430KNE)



Switching Characteristics Diagram