



**SANYO Semiconductors**

# DATA SHEET

An ON Semiconductor Company

## LC79401KNE — CMOS LSI Dot-Matrix LCD Drivers

### Overview

The LC79401KNE is a 80-outputs segment driver LSI for graphic dot-matrix liquid crystal display systems. The LC79401KNE latches 80 bits of display data sent from a controller using a 4-bit parallel transfer technique and generates LCD drive signals. When combined as a kit with common driver, either the LC79430KNE (QIP100E), the LC79401KNE can drive large screen LCD panels.

### Features

- Incorporates LCD drive circuits for 80 bits of display.
- Supports display duties from 1/64 to 1/256
- The provision of a chip disable pin supports power reduction in large-scale panels.
- Allows external provision of the bias power supply
- Operating supply voltage/operating temperature  
 $V_{DD}$  (logic block) : 2.7 to 5.5V/-20 to +85°C  
 $V_{DD-V_{EE}}$  (LCD block) : 12 to 32V/-20 to +85°C
- Data transfer clock : 6.0MHz (max), bidirectional shifting supported
- Data input : 4-bit parallel input
- CMOS process
- 100-pin flat plastic package (QIP100E)

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<http://www.sanyosemi.com/en/network/>

# LC79401KNE

## Specifications

**Absolute Maximum Ratings** at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage (Logic)	$V_{DD}$ max		-0.3 to +7.0	V
Maximum supply voltage (LCD)	$V_{DD}-V_{EE}$ max	*1	0 to 35	V
Maximum input voltage	$V_I$ max		-0.3 to $V_{DD}+0.3$	V
Storage temperature	Tstg		-40 to +125	$^\circ\text{C}$

Note \*1  $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$ ,  $V_{DD}-V_3 \leq 7\text{V}$ ,  $V_4-V_{EE} \leq 7\text{V}$

**Allowable Operating Ranges** at  $T_a = -20$  to  $+85^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage (Logic)	$V_{DD}$		2.7		5.5	V
Supply voltage (LCD)	$V_{DD}-V_{EE}$	*2, 3	12		32	V
Input high level voltage	$V_{IH}$	DI1 to DI4, CP, LOAD, CDI, R/L, M, DISPOFF	$0.8V_{DD}$			V
Input low level voltage	$V_{IL}$	DI1 to DI4, CP, LOAD, CDI, R/L, M, DISPOFF			$0.2V_{DD}$	V
CP Shift clock	$f_{CP}$	CP			6.0	MHz
CP pulse width	$t_{WC}$	CP	50			ns
LOAD pulse width	$t_{WL}$	LOAD	50			ns
Setup time	$t_{SETUP}$	DI1 to DI4 $\rightarrow$ CP	30			ns
Hold time	$t_{HOLD}$	DI1 to DI4 $\rightarrow$ CP	$V_{DD}=2.7$ to $4.5\text{V}$	40		ns
			$V_{DD}=4.5$ to $5.5\text{V}$	30		ns
CP $\rightarrow$ LOAD	$t_{CL}$	CP $\rightarrow$ LOAD	80			ns
LOAD $\rightarrow$ CP	$t_{LC1}$	LOAD $\rightarrow$ CP		110		ns
			$V_{DD}=2.7$ to $4.5\text{V}$	30		ns
			$V_{DD}=4.5$ to $5.5\text{V}$	15		ns
CP and LOAD rise time	$t_R$	CP, LOAD			*4	ns
CP and LOAD fall time	$t_F$	CP, LOAD			*4	ns

Note \*2  $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$ ,  $V_{DD}-V_3 \leq 7\text{V}$ ,  $V_4-V_{EE} \leq 7\text{V}$

\*3 When the power is turned on, either the logic system power must be turned on before the LCD drive system power or else they must both be turned on at the same time. When the power is turned off, either the LCD drive system power must be turned off before the logic system power, or else both must be turned off at the same time.

\*4 The CP and LOAD rise time ( $t_R$ ) and the CP and LOAD fall time ( $t_F$ ) must satisfy equations (1) and (2) below at the same time.

$$(1) t_R, t_F < \frac{1}{2f_{CP}} - t_{WC} \quad (2) t_R, t_F < 50\text{ns}$$

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## Electrical Characteristics at $T_a = 25 \pm 2^\circ\text{C}$ , $V_{DD} = 2.7$ to $5.5\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
Input high level current	$I_{IH}$	$V_{IN}=V_{DD}$ , LOAD, CP, CDI, R/L, DI1 to DI4, M, DISPOFF			1	$\mu\text{A}$
Input low level current	$I_{IL}$	$V_{IN}=V_{SS}$ , LOAD, CP, CDI, R/L, DI1 to DI4, M, DISPOFF	-1			$\mu\text{A}$
Output high level voltage	$V_{OH}$	$I_{OH}=-400\mu\text{A}$ , CDO	$V_{DD}-0.4$			V
Output low level voltage	$V_{OL}$	$I_{OL}=400\mu\text{A}$ , CDO			0.4	V
Driver on resistance	$R_{ON(1)}$	$V_{DD}-V_{EE}=30\text{V}$ , $ V_{DE}-V_O =0.5\text{V}$ : O1 to O80 *5		0.6	1.5	$\text{k}\Omega$
	$R_{ON(2)}$	$V_{DD}-V_{EE}=20\text{V}$ , $ V_{DE}-V_O =0.5\text{V}$ : O1 to O80 *5		0.7	2.0	$\text{k}\Omega$
Standby current drain	$I_{ST}$	CDI= $V_{DD}$ , $V_{DD}-V_{EE}=30\text{V}$ , CP=6.0MHz, Output unloaded: $V_{SS}$			200	$\mu\text{A}$
Operating current drain	$I_{SS}$ *6	$V_{DD}-V_{EE}=30\text{V}$ , CP=6MHz, LOAD=14kHz, M=35Hz: $V_{SS}$			4.0	mA
	$I_{EE}$ *7	$V_{DD}-V_{EE}=30\text{V}$ , CP=6MHz, LOAD=14kHz, M=35Hz: $V_{EE}$			0.5	mA
Input capacitance	$C_I$	f=6.0MHz; CP		8		pF

Note \*5  $V_{DE}$  = one of V1, V3, V4 or  $V_{EE}$ , V1 =  $V_{DD}$ , V3 =  $15/17 (V_{DD}-V_{EE})$ , V4 =  $2/17 (V_{DD}-V_{EE})$

\*6  $I_{SS}$  is the current flowing from  $V_{DD}$  to  $V_{SS}$

\*7  $I_{EE}$  is the current flowing from  $V_{DD}$  to  $V_{EE}$

## Switching Characteristics at $T_a = 25 \pm 2^\circ\text{C}$ , $V_{SS} = 0\text{V}$ , $V_{DD} = 2.7$ to $5.5\text{V}$

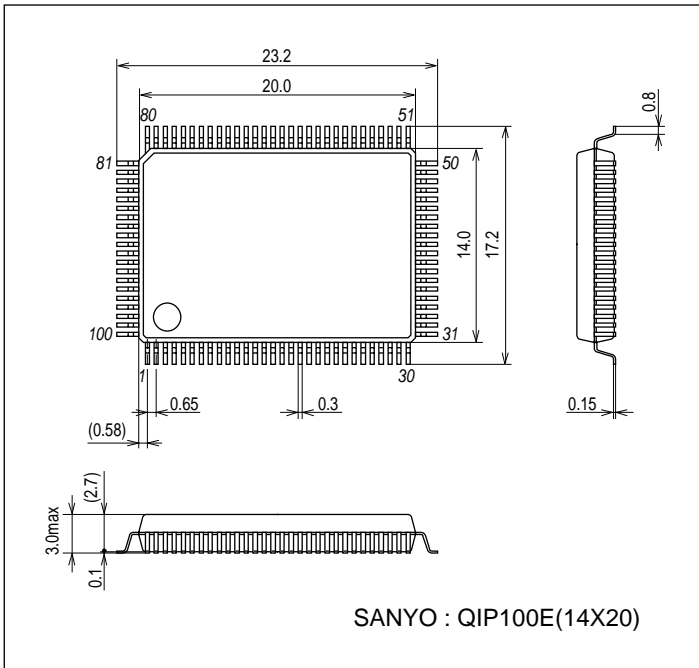
Parameter	Symbol	Conditions	min	typ	max	unit	
Output delay time 1	$t_{D1}$	Load=15pF: CDO	$V_{DD}=2.7$ to $4.5\text{V}$			100	ns
			$V_{DD}=4.5$ to $5.5\text{V}$			80	ns
Output delay time 2	$t_{D2}$	Load=15pF: CDO	$V_{DD}=2.7$ to $4.5\text{V}$			100	ns
			$V_{DD}=4.5$ to $5.5\text{V}$			80	ns

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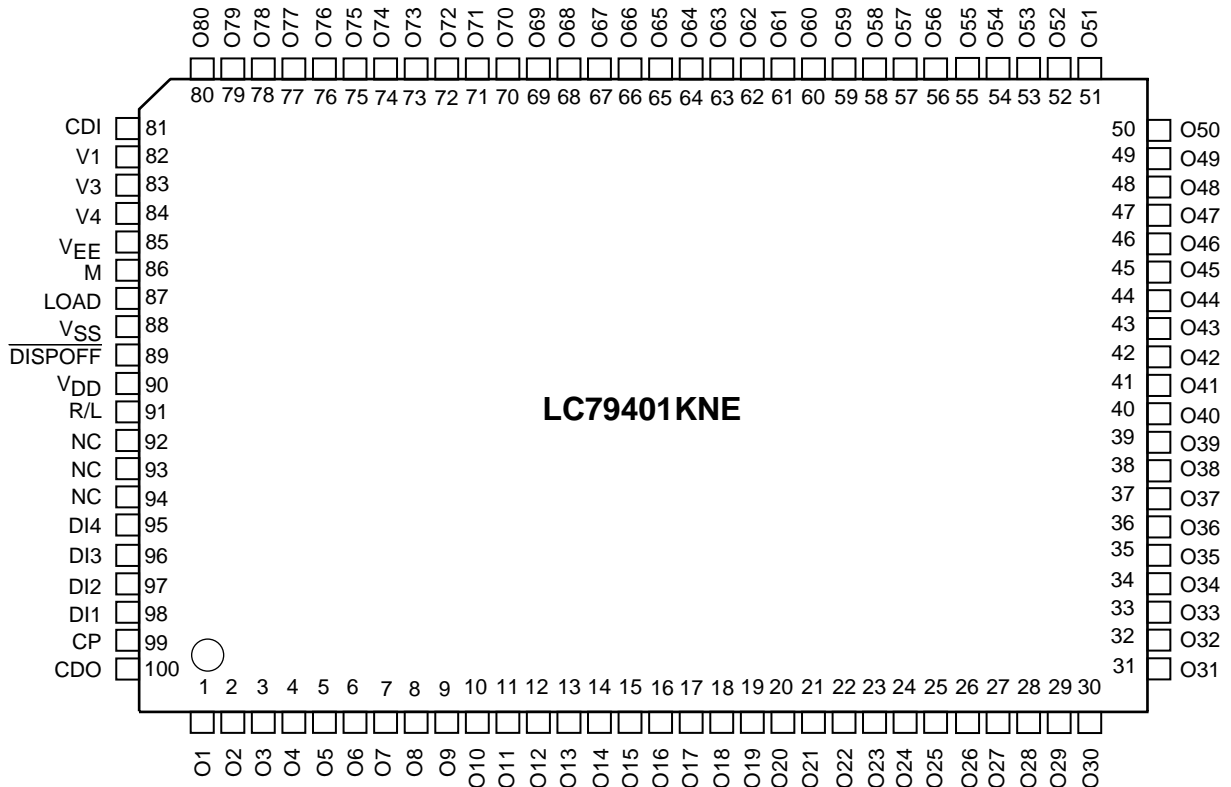
## Package Dimensions

unit:mm (typ)

3151A



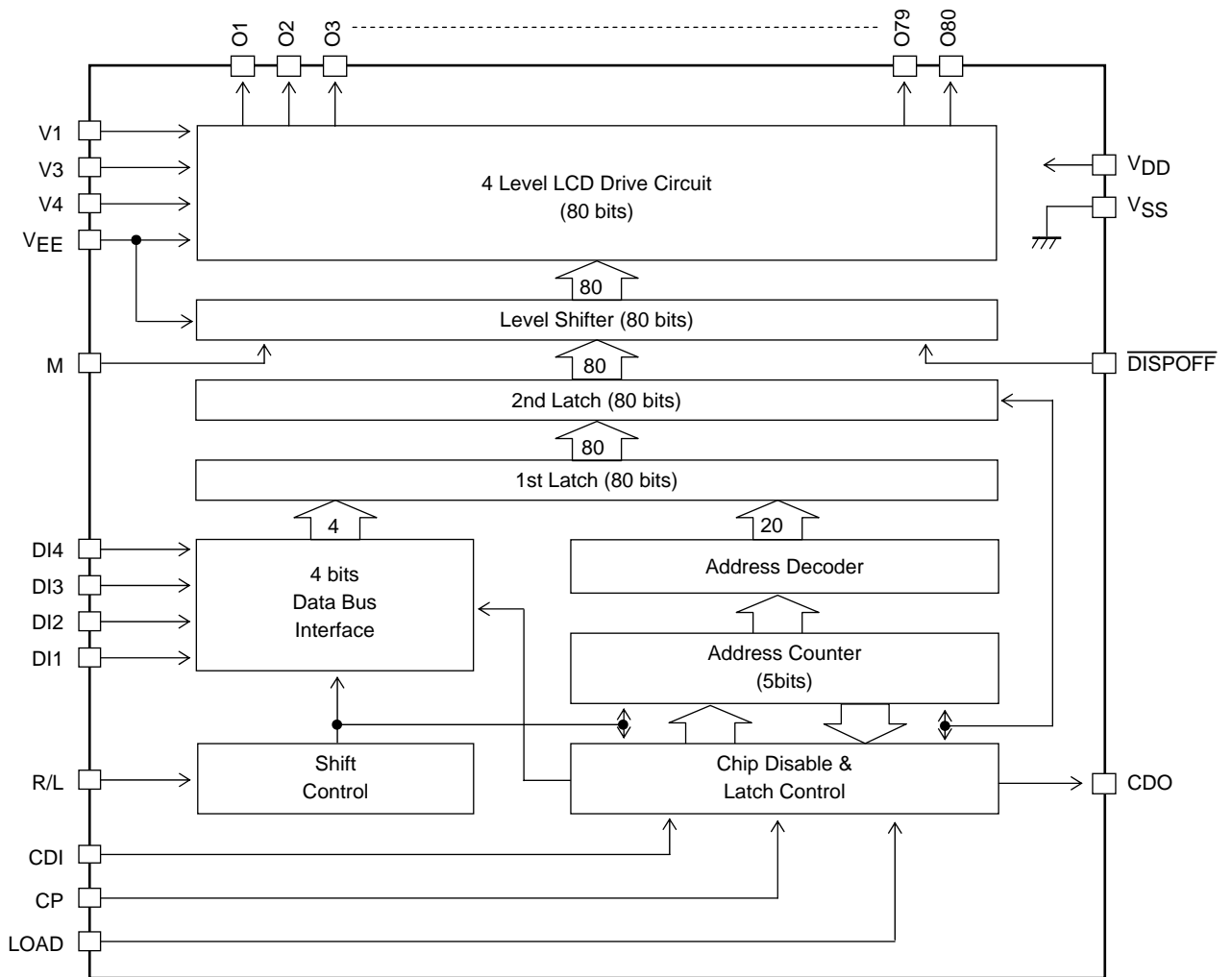
## Pin Assignment



Top view

# LC79401KNE

## Equivalent Circuit Block Diagram



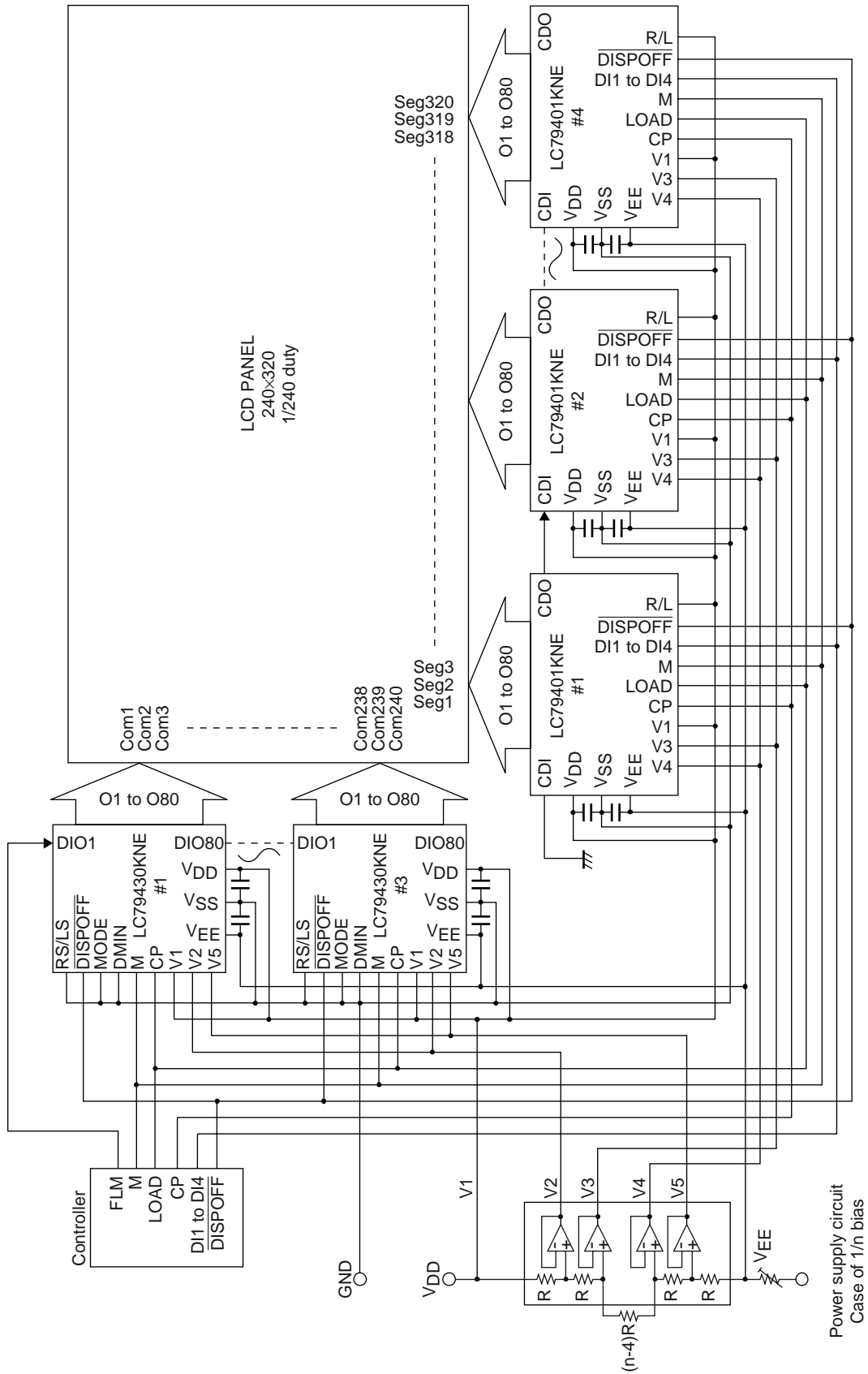
# LC79401KNE

## Pin Function

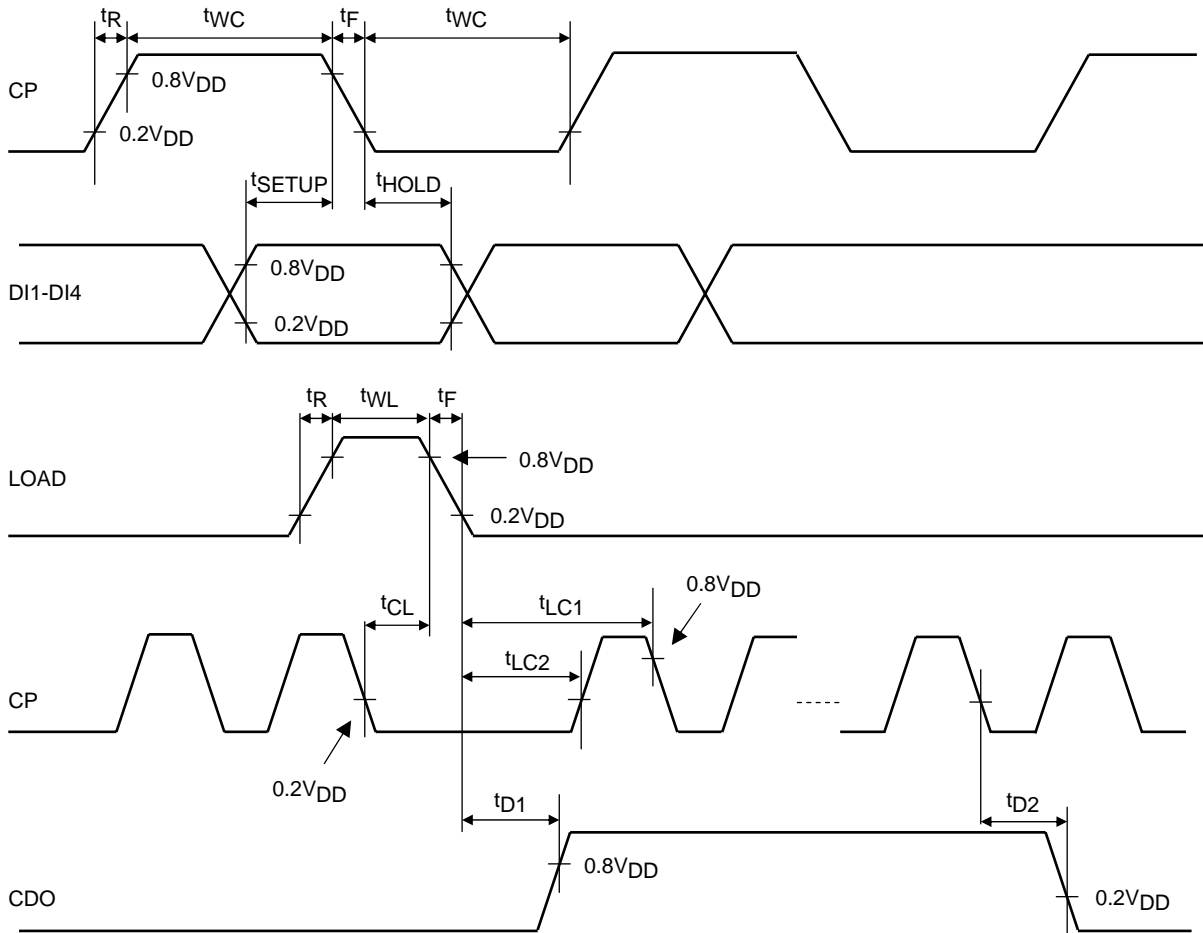
Pin No	Symbol	I/O	Function																																																																																		
90	V <sub>DD</sub>	Supply	V <sub>DD</sub> -V <sub>SS</sub> : Logic power supply V <sub>DD</sub> -V <sub>EE</sub> : LCD drive circuit power supply																																																																																		
88	V <sub>SS</sub>																																																																																				
85	V <sub>EE</sub>																																																																																				
82	V1	Supply	LCD drive level power supply V1, V <sub>EE</sub> : Selected level V3, V4 : Unselected level																																																																																		
83	V3																																																																																				
84	V4																																																																																				
99	CP	I	Display data acquisition clock (falling edge trigger)																																																																																		
87	LOAD	I	Display data latch clock (falling edge trigger) The display data LCD drive signal is output on the falling edge.																																																																																		
95 96 97 98	DI4 DI3 DI2 DI1	I	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Display data</th> <th>LCD drive output</th> <th>LCD display</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Selected level</td> <td>On</td> </tr> <tr> <td>L</td> <td>Unselected level</td> <td>Off</td> </tr> </tbody> </table>	Display data	LCD drive output	LCD display	H	Selected level	On	L	Unselected level	Off																																																																									
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91	R/L	I	<p>Control pin that inverts the data output destination</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">R/L</th> <th rowspan="2">Data input</th> <th colspan="7">Number of clock</th> </tr> <tr> <th>1</th> <th>2</th> <th>3</th> <th>...</th> <th>18</th> <th>19</th> <th>20</th> </tr> </thead> <tbody> <tr> <td rowspan="4">L</td> <td>DI1</td> <td>O77</td> <td>O73</td> <td>O69</td> <td>...</td> <td>O9</td> <td>O5</td> <td>O1</td> </tr> <tr> <td>DI2</td> <td>O78</td> <td>O74</td> <td>O70</td> <td>...</td> <td>O10</td> <td>O6</td> <td>O2</td> </tr> <tr> <td>DI3</td> <td>O79</td> <td>O75</td> <td>O71</td> <td>...</td> <td>O11</td> <td>O7</td> <td>O3</td> </tr> <tr> <td>DI4</td> <td>O80</td> <td>O76</td> <td>O72</td> <td>...</td> <td>O12</td> <td>O8</td> <td>O4</td> </tr> <tr> <td rowspan="4">H</td> <td>DI1</td> <td>O4</td> <td>O8</td> <td>O12</td> <td>...</td> <td>O72</td> <td>O76</td> <td>O80</td> </tr> <tr> <td>DI2</td> <td>O3</td> <td>O7</td> <td>O11</td> <td>...</td> <td>O71</td> <td>O75</td> <td>O79</td> </tr> <tr> <td>DI3</td> <td>O2</td> <td>O6</td> <td>O10</td> <td>...</td> <td>O70</td> <td>O74</td> <td>O78</td> </tr> <tr> <td>DI4</td> <td>O1</td> <td>O5</td> <td>O9</td> <td>...</td> <td>O69</td> <td>O73</td> <td>O77</td> </tr> </tbody> </table>	R/L	Data input	Number of clock							1	2	3	...	18	19	20	L	DI1	O77	O73	O69	...	O9	O5	O1	DI2	O78	O74	O70	...	O10	O6	O2	DI3	O79	O75	O71	...	O11	O7	O3	DI4	O80	O76	O72	...	O12	O8	O4	H	DI1	O4	O8	O12	...	O72	O76	O80	DI2	O3	O7	O11	...	O71	O75	O79	DI3	O2	O6	O10	...	O70	O74	O78	DI4	O1	O5	O9	...	O69	O73	O77
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86	M	I	LCD drive output alternation signal																																																																																		
81	CDI	I	Chip disable pin High level : Data is not acquired. Low level : Data is acquired																																																																																		
100	CDO	O	Connect to the CDI pin on the next chip when cascade connection is used.																																																																																		
89	$\overline{\text{DISPOFF}}$	I	Input that controls the O1 to O80 output pins. During periods when this pin is low, the O1 to O80 output pins output the V1 level. See the truth table.																																																																																		
1 to 80	O1 to O80	O	<p>LCD drive outputs</p> <p>The output level are determined by the combination of the output the data, The M signal, and The <math>\overline{\text{DISPOFF}}</math> pin as shown in the table.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>M</th> <th>Q</th> <th><math>\overline{\text{DISPOFF}}</math></th> <th>Output</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>H</td> <td>V3</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>V1</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>V4</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>V<sub>EE</sub></td> </tr> <tr> <td>*</td> <td>*</td> <td>L</td> <td>V1</td> </tr> </tbody> </table> <p>Note : don't care (fixed at high or low)</p>	M	Q	$\overline{\text{DISPOFF}}$	Output	L	L	H	V3	L	H	H	V1	H	L	H	V4	H	H	H	V <sub>EE</sub>	*	*	L	V1																																																										
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# LC79401KNE

## Application Example (LC79401KNE/LC79430KNE)



Switching Characteristics Diagram



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