

SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LC75890W _____

смов IC 1/4duty and Static Drive General-Purpose LCD Display Drivers

Overview

The LC75890W and LC75890E are 1/4 duty and static drive general-purpose LCD display drivers that can be used for displaying segments for household appliances, home audio visual products, portable devices and other such products under the control of a microcontroller. The LC75890W can drive up to 148 segments directly, and the LC75890E can drive up to 132 segments directly. In addition the LC75890W can control up to 12 general-purpose output ports, and the LC75890E can control up to 11 general-purpose output ports. They can control the brightness of the LED backlight of RGB, because they have the PWM output of greatest 3CH built-in. Incorporation of the oscillation circuit helps to reduce the number of external resistors and capacitors required. Incorporation of the LCD drive bias voltage stabilization.

Features

- Support for 1/4-duty 1/3-bias or static drive techniques under serial data control.
 - <LC75890W(SQFP48)>

When 1/4-duty drive : Capable of driving up to 148 segments When Static drive : Capable of driving up to 37 segments <LC75890E(QIP44M)> When 1/4-duty drive : Capable of driving up to 132 segments

When Static drive : Capable of driving up to 33 segments

• Support for display segment on, off, or blinking for each segment output pin under serial data control.

Continued on next page.

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- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output port function.
 - <LC75890W : Support for up to 12 general-purpose output ports>
 - <LC75890E : Support for up to 11 general-purpose output ports>
- Support for the PWM output function of a maximum of 3ch. (It can output from the general-purpose output port).
- Serial data control of the frame frequency of the common and segment output waveforms.
- Serial data control of the segment blinking frequency.
- Serial data control of switching between the internal oscillator operating mode and external clock operating mode.
- Serial data input supports CCB format communication with the system controller.
- Independent V_{LCD} for the LCD driver block.
- Built-in LCD drive bias voltage stabilization circuit.
- The $\overline{\text{INH}}$ pin allows the display to be forced to the off state.
- Incorporation of an oscillator circuit. (Incorporation of resistor and capacitor for an oscillation)

Specifications Absolute Maximum Ratings at Ta = 25° C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max	V _{DD}	-0.3 to +4.2	Ň
	V _{LCD} max	V _{LCD}	-0.3 to +6.5	V
Input voltage	V _{IN} 1	CE, CL, DI, INH	-0.3 to +4.2	Ň
	V _{IN} 2	OSCI : External clock operating mode	-0.3 to V _{DD} +0.3	V
Output voltage	VOUT	S1 to S37, COM1 to COM4, P1 to P12 *1	-0.3 to V _{LCD} +0.3	V
Output current	IOUT1	S1 to S36 *1	300	μA
	I _{OUT} 2	COM1 to COM4, S37	3	
	IOUT ³	P1 to P12 *1 *2	5	mA
Allowable power dissipation	Pd max1	LC75890W(SQFP48) Ta=85°C	100	
	Pd max2	LC75890E(QIP44M) Ta=85°C	100	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Note : *1 In the case of the LC75890E(QIP44M), the output pins are effective for only S1 to S11, S13 to S23, S25 to S34, and S37 pins.

*2 The sum of output current through P1 to P12 must be 40mA or less.

Allowable Operating Ranges at Ta = -40 to $+85^{\circ}C$, $V_{SS} = 0V$

Deremeter	Cumhal		Conditions		11-34		
Parameter	Symbol Conditions		min	typ	max	Unit	
Supply voltage	V _{DD}	V _{DD}		2.7		3.6	
	VLCD	V _{LCD} : Internal osc	illator operating mode	2.7		5.5	V
		V _{LCD} : External clo	ock operating mode	V _{DD}		5.5	
Input high-level voltage	V _{IH} 1	CE, CL, DI, INH		0.7V _{DD}		3.6	V
	V _{IH} 2	OSCI: External clo	ck operating mode	0.7V _{DD}		V _{DD}	v
Input low-level voltage	V _{IL} 1	CE, CL, DI, INH		0		0.2V _{DD}	V
	V _{IL} 2	OSCI: External clock operating mode		0		0.2V _{DD}	v
External clock operating frequency	^f CK	OSCI: External clock operating mode [Figure 3]		10	38	600	kHz
External clock duty cycle	DCK	OSCI: External cloc	k operating mode [Figure 3]	30	50	70	%
Data setup time	tds	CL, DI	[Figure 1][Figure 2]	160			ns
Data hold time	tdh	CL, DI	[Figure 1][Figure 2]	160			ns
CE wait time	tcp	CE, CL	[Figure 1][Figure 2]	160			ns
CE setup time	tcs	CE, CL	[Figure 1][Figure 2]	160			ns
CE hold time	tch	CE, CL	[Figure 1][Figure 2]	160			ns
High-level clock pulse width	tφH	CL	[Figure 1][Figure 2]	160			ns
Low-level clock pulse width	tφL	CL	[Figure 1][Figure 2]	160			ns
Rise time	tr	CE, CL, DI	[Figure 1][Figure 2]		160		ns
Fall time	tf	CE, CL, DI	[Figure 1][Figure 2]		160		ns
INH switching time	tc	ĪNH	[Figure 4][Figure 5]	10			μs

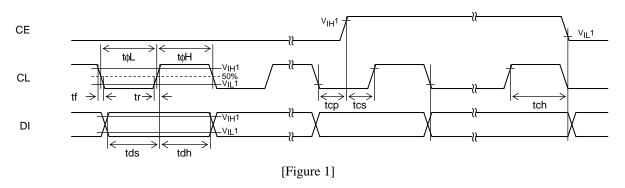
Parameter	Symbol	Pin	Conditions	Ratings			
i alametei	Cymbol		Conditions	min	typ	max	Unit
Hysteresis	٧ _H	CE, CL, DI, INH			0.1V _{DD}		V
Input high-level current	I _{IH} 1	CE, CL, DI, INH	V _I = 3.6V			1.0	
	I _{IH} 2	OSCI	$V_I = V_{DD}$: External clock operating mode			1.0	μA
Input low-level current	l _{IL} 1	CE, CL, DI, ĪNH	$V_{I} = 0V$	-1.0			
	I _{IL} 2	OSCI	V _I = 0V: External clock operating mode	-1.0			μA
Output high-level voltage	V _{OH} 1	S1 to S37 *3	I _O = -10μA	V _{LCD} -0.9			
	V _{OH} 2	COM1 to COM4	l _O = -100μA	V _{LCD} -0.9			V
	V _{OH} 3	P1 to P12 *3	I _O = -1mA	V _{LCD} -0.9			
Output low-level voltage	V _{OL} 1	S1 to S37 *3	I _O = 10μA			0.9	
	V _{OL} 2	COM1 to COM4	l _O = 100μA			0.9	v
	V _{OL} 3	P1 to P12 *3	I _O =1mA			0.9	
Output middle-level voltage	V _{MID} 1	S1 to S37 *3	$1/4 \text{ duty } I_{O} = \pm 10 \mu A$	2/3V _{LCD} -0.9		2/3V _{LCD} +0.9	
	V _{MID} 2	S1 to S37 *3	$1/4 \text{ duty I}_{O} = \pm 10 \mu \text{A}$	1/3V _{LCD} -0.9		1/3V _{LCD} +0.9	
	V _{MID} 3	COM1 to COM4	1/4 duty I _O = ±100µA	2/3V _{LCD} -0.9		2/3V _{LCD} +0.9	V
	V _{MID} 4	COM1 to COM4	1/4 duty I _O = ±100µA	1/3V _{LCD} -0.9		1/3V _{LCD} +0.9	
Oscillator frequency	fosc	Internal oscillator circuit	Internal oscillator operating mode	240	300	360	kHz
Current drain	I _{DD} 1	V _{DD}	Power-saving mode			2	
	I _{DD} 2	V _{DD}	V _{DD} = 3.3V, Normal mode, External clock operating mode *4		5	10	
	I _{DD} 3	V _{DD}	V _{DD} = 3.3V, Normal mode, External clock operating mode *4 Serial data transfer *5		90	180	
	I _{DD} 4	V _{DD}	V _{DD} = 3.3V, Normal mode, Internal oscilloator operating mode		50	100	
	I _{DD} 5	V _{DD}	V _{DD} = 3.3V, Normal mode, Internal oscilloator operating mode, Serial data transfer *5		135	270	μΑ
	I _{LCD} 1	V _{LCD}	Power-saving mode			2	
	I _{LCD} 2	V _{LCD}	V _{LCD} = 3.3V, Output open, Normal mode, Static drive		8	16	1
	I _{LCD} 3	V _{LCD}	V _{LCD} = 3.3V, Output open, Normal mode, 1/4 duty drive		70	140	
	ILCD ⁴	V _{LCD}	V _{LCD} = 5.0V, Output open, Normal mode, Static drive		10	20	
	I _{LCD} 5	V _{LCD}	V _{LCD} = 5.0V, Output open, Normal mode, 1/4 duty drive		90	180	

Note : *3 In the case of the LC75890E(QIP44M), the output pins are effective for only S1 to S11, S13 to S23, S25 to S34, and S37 pins.

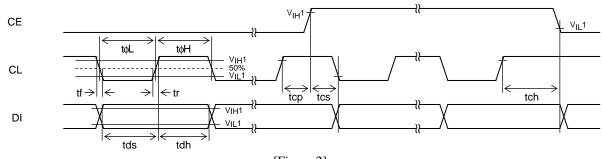
*4 External clock operating mode (f_{CK}=38kHz, V_{IH}2=V_{DD}, V_{IL}2=0V, rise/fall time=20ns)

*5 Serial data transfer (data transfer frequency 2MHz, V_{II}1=V_{DD}, V_{II}1=0V, rise/fall time=20ns)

1. When CL is stopped at the low level

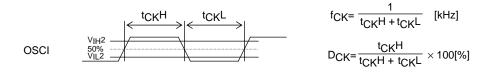


2. When CL is stopped at the high level



[Figure 2]

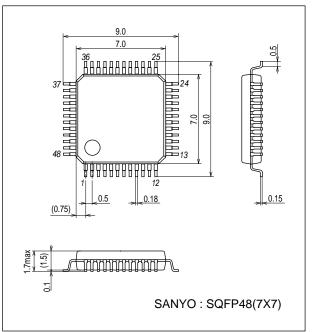
3. OSCI pin clock timing in external clock operating mode



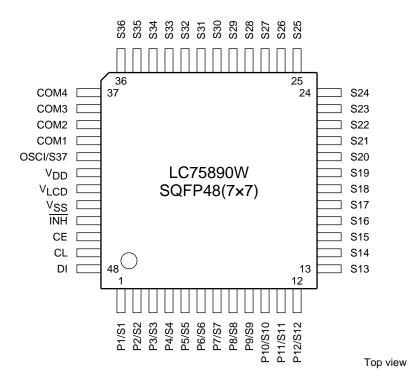
[Figure 3]

Package Dimensions

unit : mm (typ) 3163B

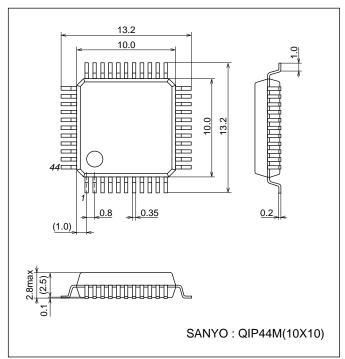


Pin Assignment

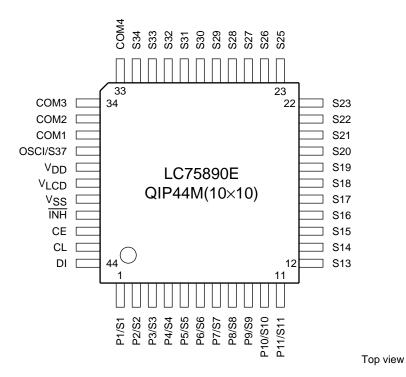


Package Dimensions

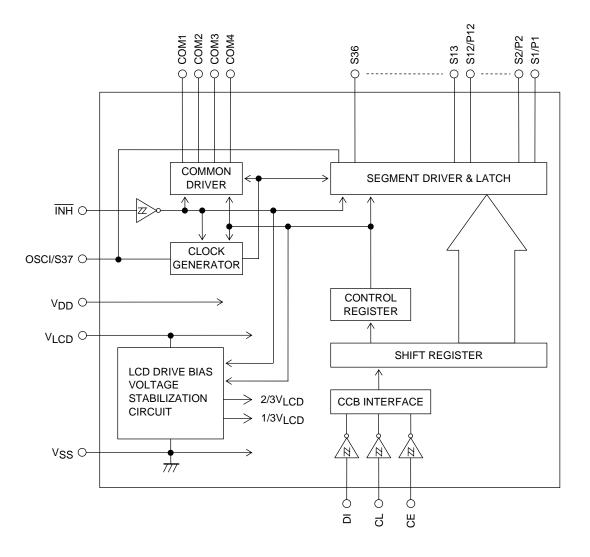
unit : mm (typ) 3148A



Pin Assignment



Block Diagram



Pin Functions

		No.	4			Handling
Symbol	LC75890W (SQFP48)	LC75890E (QIP44M)	Function	Active	I/O	when unused
S1/P1	1	1				
S2/P2	2	2				
S3/P3	3	3				
S4/P4	4	4				
S5/P5	5	5				
S6/P6	6	6				
S7/P7	7	7				
S8/P8	8	8				
S9/P9	9	9				
S10/P10	10	10				
S11/P11	11	11				
S12/P12	12	-				
S13	13	12				
S14	14	13				
S15	15	14	Segment outputs for displaying the display data			
S16	16	15	transferred by serial data input.			
S17	17	16	The S1/P1 to S12/P12 pins can be used as general-			
S18	18	17	purpose output ports under serial data control.			0.0551
S19	19	18		-	0	OPEN
S20	20	19	Note :			
S21	21	20	In the case of the LC75890E (QIP44M), the output pins			
S22	22	21	are effective for only S1 to S11, S13 to S23, and S25 to			
S23	23	22	S34 pins.			
S24	24	-				
S25	25	23				
S26	26	24				
S27	27	25				
S28	28	26				
S29	29	27				
S30	30	28				
S31	31	29				
S32	32	30				
S33	33	31				
S34	34	32				
S35	35	-				
S36	36	-				
COM4	37	33				
COM3	38	34	Common driver outputs The frame fragments is fall to 1			OPEN
COM2	39	35	Common driver outputs The frame frequency is fo[Hz].	-	0	OPEN
COM1	40	36				
			Segment output.			
S37/OSCI	41	37	This pin can also be used as the external clock input pin	-	I/O	OPEN
			when the external clock operating mode is selected by			
CE	46	42	control data. Serial data transfer inputs. Must be connected to the	н	1	
			controller.			
CL	47	43	CE : Chip enable CL : Synchronization clock		I	GND
DI	48	44	DI : Transfer data	-	I	

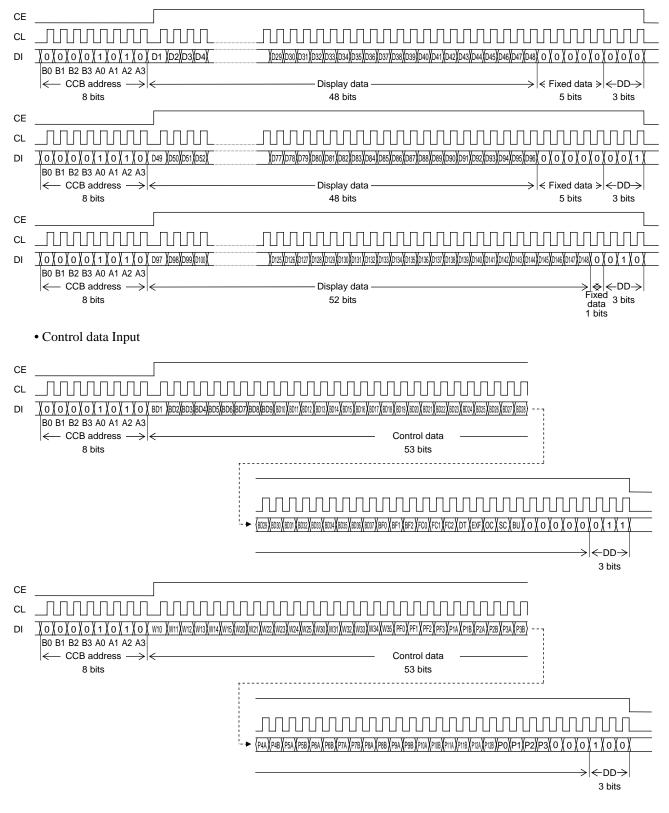
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Pin No. Symbol LC75890W LC75890E		No.				Handling
			Function	Active	I/O	when
	(SQFP48)	(QIP44M)				unused
			Display off control input			
			• INH = low (V _{SS})Display forced off			
			S1/P1 to S12/P12=low (V _{SS})			
			(These pins are forcibly set to the general-purpose			
			output port function and held at the V_{SS} level.)			
			S13 to S36=low (V _{SS})			
			COM1 to COM4=low (V _{SS})			
			S37/OSCI=low (V _{SS})			
			(This pin is forcibly set to the segment output port			
		function and held at the V_{SS} level.)				
ĪNĦ	45	41	LCD drive bias voltage stabilization circuit stopped.	L		GND
			Stops the internal oscillator.			
			Inhibits external clock input.			
			• INH = high (V _{DD})Display on			
			LCD drive bias voltage stabilization circuit is enabled.			
			Enables the internal oscillator circuit.			
			(Internal oscillator operating mode)			
			Enables external clock input.			
			(External clock operating mode)			
			However, serial data transfer is possible when the			
			display is forced off.			
VDD	42	38	Logic block power supply pin. A power voltage of 2.7 to	-	-	-
ייי			3.6V must be applied to this pin.		ļ	
VLCD	43	39	LCD driver block power supply pin. A power voltage of	-	-	-
*LCD	0		2.7 to 5.5V must be applied to this pin.			
VSS	44	40	Ground pin. Must be connected to ground.	-	-	-

Serial Data Input

1. 1/4 duty drive

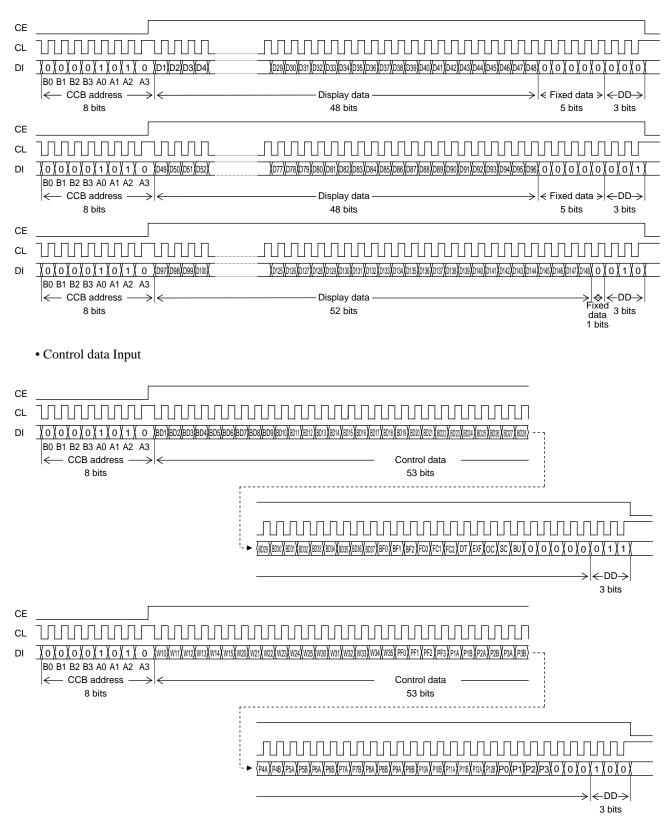
- (1) When CL is stopped at the low level
- Display data Input



Note: DD is the direction data.

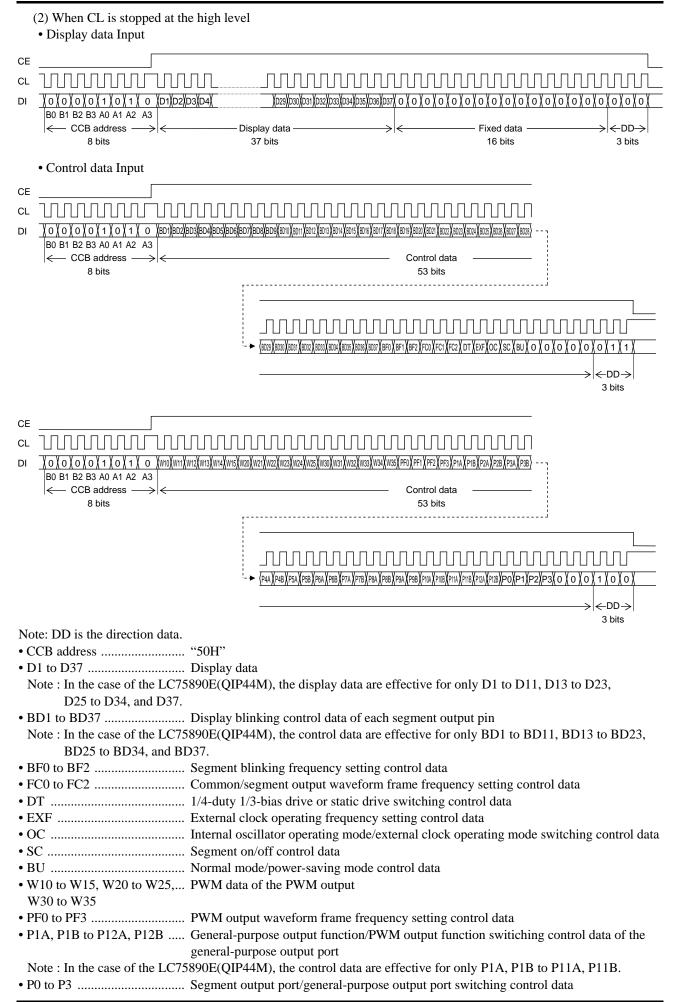
(2) When CL is stopped at the high level

• Display data Input



Note: DD is the direction data.

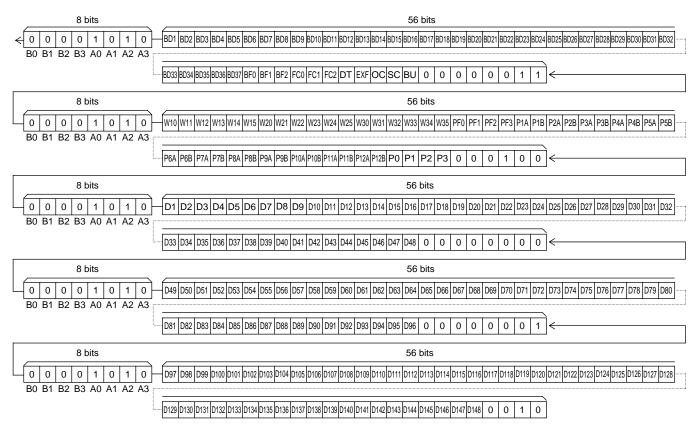
• CCB address	"50H"
• D1 to D148	
	5890E(QIP44M), the display data are effective for only D1 to D44, D49 to D92,
D97 to D136, and D14 • BD1 to BD37	Display blinking control data of each segment output pin
	5890E(QIP44M), the control data are effective for only BD1 to BD11, BD13 to BD23,
BD25 to BD34, and Bl	· · ·
	Segment blinking frequency setting control data
	Common/segment output waveform frame frequency setting control data
	1/4-duty 1/3-bias drive or static drive switching control data External clock operating frequency setting control data
	Internal oscillator operating mode/external clock operating mode switching control data
• SC	•
	Normal mode/power-saving mode control data
• w10 to w15, w20 to w25, W30 to W35	PWM data of the PWM output
	PWM output waveform frame frequency setting control data
• P1A, P1B to P12A, P12B	General-purpose output function/PWM output function switiching control data of the
	general-purpose output port
	5890E(QIP44M), the control data are effective for only P1A, P1B to P11A, P11B. Segment output port/general-purpose output port switching control data
10.015	segment output por general-pulpose output por switching control data
2. Static drive	
(1) When CL is stopped at the	ne low level
• Display data Input	
DI <u>X 0 X 0 X 0 X 0 X 1 X 0 X 1 X 0 X D1 XD2</u> B0 B1 B2 B3 A0 A1 A2 A3	
\leftarrow CCB address \rightarrow \leftarrow 8 bits	Display data Fixed data // C-DD->
o bits	
Control data Input	
CE	
	BO3/BD4/BD5/BD6/BD7/BD8/BD9/80/W X80/1 X80/2 X80/4 X80/4 X80/4 X80/4 X80/4 X80/4 X80/2 X
\leftarrow CCB address \rightarrow	Control data
8 bits	53 bits
CE.	$\xrightarrow{\text{Im}_{A} \to A} \xrightarrow{\text{Im}_{A} \to A} \text{$
се	$\xrightarrow{\text{Im}_{A} \to A} \xrightarrow{\text{Im}_{A} \to A} \text{$
CE	
CL	
CL	
CL $10^{0} \times 10^{1} $	<u> </u>
CL $10^{0} \times 10^{1} $	<u> </u>
CL $10^{0} \times 10^{1} $	<u> </u>
CL $10^{0} \times 10^{1} $	<u> </u>
CL $10^{0} \times 10^{1} $	Image: A _ A _ A _ A _ A _ A _ A _ A _ A _ A



Serial Data Transfer Example

1. 1/4 duty drive

• LC75890W(SQFP48) : When 97 or more segments are used LC75890E(QIP44M) : When 89 or more segments are used All 320 bits of serial data (including CCB address) must be sent.



• LC75890W(SQFP48) : When fewer than 97 segments are used

LC75890E(QIP44M) : When fewer than 89 segments are used

Depending on the number of segments used, 192 bits or 256 bits (including CCB address) must be sent as serial data. However, the serial data (control data) shown in the figure below must be sent without fail.

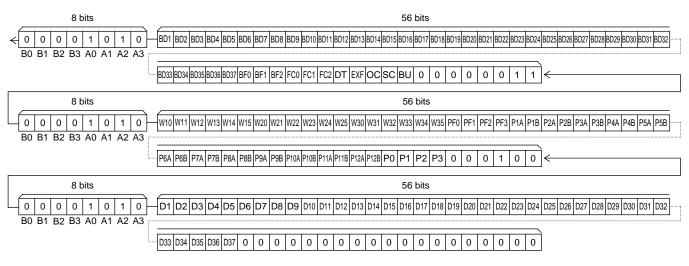


Note : After the above serial data is sent, the contents of the display data can be changed by transferring only the serial data (CCB address, display data, fixed data, and direction data) including the display data to be changed in 64-bit units.

In addition, in the case of the LC75890E(QIP44M), the display data are effective for only D1 to D44, D49 to D92, D97 to D136, and D145 to D148, the control data are effective for only BD1 to BD11, BD13 to BD23, BD25 to BD34, BD37, and P1A, P1B to P11A, P11B.

2. Static drive

• All 192 bits of serial data (including CCB address) must be sent.



Note : In the case of the LC75890E(QIP44M), the display data are effective for only D1 to D11, D13 to D23, D25 to D34, and D37, the control data are effective for only BD1 to BD11, BD13 to BD23, BD25 to BD34, BD37, and P1A, P1B to P11A, P11B.

Control Data Functions

(1) BD1 to BD37 ... Display blinking control data of each segment output pin

These control data bits are used to set the display segment blinking corresponding to each segment output pin.

BDn	Display segment blinking states of segment output pin Sn
0	The display segments are not blinked.
1	The display segments corresponding to the segment output pin Sn that the contents of display data are "1" are blinked.

Note: The BDn (n=1 to 37) are the control data setting the blinking state of the display segments for segment output pins Sn (n=1 to 37). However, in the case of the LC75890E(QIP44M), the control data are effective for only BD1 to BD11, BD13 to BD23, BD25 to BD34, and BD37.

For example, the display state of segment output pin S21 becomes as follows when the contents of display data are (D81, D82, D83, D84)=(1, 0, 1, 0) in 1/4 duty drive

DD04		Displa	y data		Display states of segment output pin S21			
BD21	D81	D82	D83	D84	COM1	COM2	COM3	COM4
0	1	0	1	0	on	off	on	off
1	1	0	1	0	blink	off	blink	off

(2) BF0 to BF2 ... Segment blinking frequency setting control data

These control data bits are used to set the display segment blinking frequency

C	Control data		Segment blinking frequency fb[Hz]				
BF0	BF1	BF2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 0, f _{CK} 1=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 1, f _{CK} 2=38[kHz]typ)		
0	0	0	fosc/600000	f _{CK} 1/600000	f _{CK} 2/75000		
1	0	0	fosc/360000	f _{CK} 1/360000	f _{CK} 2/45000		
0	1	0	fosc/300000	f _{CK} 1/300000	f _{CK} 2/37500		
1	1	0	fosc/240000	f _{CK} 1/240000	f _{CK} 2/30000		
0	0	1	fosc/180000	f _{CK} 1/180000	f _{CK} 2/22500		
1	0	1	fosc/150000	f _{CK} 1/150000	f _{CK} 2/18750		
0	1	1	fosc/120000	f _{CK} 1/120000	f _{CK} 2/15000		
1	1	1	fosc/100000	f _{CK} 1/100000	f _{CK} 2/12500		

(3) FC0 to FC2 ... Common/segment output waveform frame frequency setting control data These control data bits set the frame frequency of the common and segment output waveforms.

C	Control dat	a	Common/segment output waveform frame frequency fo[Hz]				
FC0	FC1	FC2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 0, f _{CK} 1=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 1, f _{CK} 2=38[kHz]typ)		
0	0	0	fosc/4608	f _{CK} 1/4608	f _{CK} 2/576		
0	0	1	fosc/3456	f _{CK} 1/3456	fCK2/432		
0	1	0	fosc/3072	fCK1/3072	f _{CK} 2/384		
0	1	1	fosc/2304	f _{CK} 1/2304	f _{CK} 2/288		
1	0	0	fosc/1536	fCK ^{1/1536}	f _{CK} 2/192		
1	0	1	fosc/1152	fCK ^{1/1152}	fCK2/144		
1	1	0	fosc/768	f _{CK} 1/768	f _{CK} 2/96		

Note: When is setting (FC0, FC1, FC2)=(1, 1, 1), the frame frequency is same as frame frequency at the time of the (FC0, FC1, FC2)=(0, 1, 0) setting (fosc/3072, f_{CK}1/3072, f_{CK}2/384).

(4) DT ... 1/4-duty 1/3-bias drive or static drive switching control data

This control data bit selects either 1/4-duty 1/3-bias drive or static drive.

DT		Common output pins states			
	Drive scheme	COM2	COM3	COM4	
0	1/4 duty 1/3 bias drive	COM2	COM3	COM4	
1	Static drive	"L" (V _{SS})	"L" (V _{SS})	"L" (V _{SS})	

Note: COM2, COM3, COM4 : Common output

"L" (V_{SS}) : "L" (V_{SS}) level output

(5) EXF ... External clock operating frequency setting control data

This control data bit sets the operating frequency of the external clock which input into the OSCI pin, when the external clock operating mode (OC="1") is set. However, this control data is effective only when external clock operating mode (OC="1") is set.

EXF	External clock operating frequency f _{CK} [kHz]			
0	f _{CK} 1=300[kHz]typ			
1	f _{CK} 2=38[kHz]typ			

(6) OC ... Internal oscillator operating mode/external clock operating mode switching control data

This control data bit selects either the internal oscillator operating mode or external clock operating mode.

OC	Fundamental clock operating mode	I/O pin (S37/OSCI) state		
0	Internal oscillator operating mode	S37		
1	External clock operating mode	OSCI		

Note: S37: Segment output

OSCI: External clock input

(7) SC ... Segment on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

Note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

(8) BU ... Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power saving mode In this mode, the internal oscillator circuit stops oscillation (the S37/OSCI pin is configured for segment output) if the IC is in the internal oscillator operating mode (OC=0) and the IC stops receiving external clock signals (the S37/OSCI pin is configured for external clock input) if the IC is in the external clock operating mode (OC=1). In addition, the common and segment output pins go to the V _{SS} level and the operation of LCD drive bias voltage stabilization circuit stops. However, the S1/P1 to S12/P12 output pins can be used as general-purpose output ports under the control of the data bits P0 to P3. (The general-purpose output port P1 to P12 can not be used as PWM output).

(9) W10 to W15, W20 to W25, W30 to W35 \ldots PWM data of the PWM output

These control data bits set the pulse width of the PWM output P1 to P12. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the $f_{CK}2=38[kHz]typ$ (EXF="1") in external clock operating mode (OC= "1"), these control data bits become invalid.

				,		Pulse width of	
Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	PWM output	
0	0	0	0	0	0	(1/64)×Tp	
1	0	0	0	0	0	(2/64)×Tp	
0	1	0	0	0	0	(3/64)×Tp	
1	1	0	0	0	0	(4/64)×Tp	
0	0	1	0	0	0	(5/64)×Tp	
1	0	1	0	0	0	(6/64)×Tp	
0	1	1	0	0	0	(7/64)×Tp	
1	1	1	0	0	0	(8/64)×Tp	
0	0	0	1	0	0	(9/64)×Tp	
1	0	0	1	0	0	(10/64)×Tp	
0	1	0	1	0	0	(11/64)×Tp	
1	1	0	1	0	0	(12/64)×Tp	
0	0	1	1	0	0	(13/64)×Tp	
1	0	1	1	0	0	(14/64)×Tp	
0	1	1	1	0	0	(15/64)×Tp	
1	1	1	1	0	0	(16/64)×Tp	
0	0	0	0	1	0	(17/64)×Tp	
1	0	0	0	1	0	(18/64)×Tp	
0	1	0	0	1	0	(19/64)×Tp	
1	1	0	0	1	0	(20/64)×Tp	
0	0	1	0	1	0	(21/64)×Tp	
1	0	1	0	1	0	(22/64)×Tp	
0	1	1	0	1	0	(23/64)×Tp	
1	1	1	0	1	0	(24/64)×Tp	
0	0	0	1	1	0	(25/64)×Tp	
1	0	0	1	1	0	(26/64)×Tp	
0	1	0	1	1	0	(27/64)×Tp	
1	1	0	1	1	0	(28/64)×Tp	
0	0	1	1	1	0	(29/64)×Tp	
1	0	1	1	1	0	(30/64)×Tp	
0	1	1	1	1	0	(31/64)×Tp	
1	1	1	1	1	0	(32/64)×Tp	

mode (OC= "1"), these control data bits become invalid.									
Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Pulse width of			
WIIO	••••	WIIZ	WIIO	****	WIIS	PWM output			
0	0	0	0	0	1	(33/64)×Tp			
1	0	0	0	0	1	(34/64)×Tp			
0	1	0	0	0	1	(35/64)×Tp			
1	1	0	0	0	1	(36/64)×Tp			
0	0	1	0	0	1	(37/64)×Tp			
1	0	1	0	0	1	(38/64)×Tp			
0	1	1	0	0	1	(39/64)×Tp			
1	1	1	0	0	1	(40/64)×Tp			
0	0	0	1	0	1	(41/64)×Tp			
1	0	0	1	0	1	(42/64)×Tp			
0	1	0	1	0	1	(43/64)×Tp			
1	1	0	1	0	1	(44/64)×Tp			
0	0	1	1	0	1	(45/64)×Tp			
1	0	1	1	0	1	(46/64)×Tp			
0	1	1	1	0 1		(47/64)×Tp			
1	1	1	1	0	1	(48/64)×Tp			
0	0	0	0	1	1	(49/64)×Tp			
1	0	0	0	1	1	(50/64)×Tp			
0	1	0	0	1	1	(51/64)×Tp			
1	1	0	0	1	1	(52/64)×Tp			
0	0	1	0	1	1	(53/64)×Tp			
1	0	1	0	1	1	(54/64)×Tp			
0	1	1	0	1	1	(55/64)×Tp			
1	1	1	0	1	1	(56/64)×Tp			
0	0	0	1	1	1	(57/64)×Tp			
1	0	0	1	1	1	(58/64)×Tp			
0	1	0	1	1	1	(59/64)×Tp			
1	1	0	1	1	1	(60/64)×Tp			
0	0	1	1	1	1	(61/64)×Tp			
1	0	1	1	1	1	(62/64)×Tp			
0	1	1	1	1	1	(63/64)×Tp			
1	1	1	1	((64/64)×Tp			

$$Tp = \frac{1}{fp}$$

Note:	W10 to	W15.	PWM	data of	the PW	M output (Ch1)
	W20 to	W25.	PWM	data of	the PW	M output (Ch2)
	W30 to	W35 .	PWM	data of	the PW	M output (Ch3)

(10) PF0 to PF3 ... PWM output waveform frame frequency setting control data

These control data bits set the frame frequency of the PWM output waveforms. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the $f_{CK}2=38[kHz]typ$ (EXF="1") in external clock operating mode (OC= "1"), these control data bits become invalid.

	Contro	ol data		PWM output wave	form frame frequency fp[Hz]
PF0	PF1	PF2	PF3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, f _{CK} 1=300[kHz] typ)
0	0	0	0	fosc/1536	f _{CK} 1/1536
1	0	0	0	fosc/1408	f _{CK} 1/1408
0	1	0	0	fosc/1280	f _{CK} 1/1280
1	1	0	0	fosc/1152	f _{CK} 1/1152
0	0	1	0	fosc/1024	f _{CK} 1/1024
1	0	1	0	fosc/896	f _{CK} 1/896
0	1	1	0	fosc/768	f _{CK} 1/768
1	1	1	0	fosc/640	f _{CK} 1/640
0	0	0	1	fosc/512	f _{CK} 1/512
1	0	0	1	fosc/384	fCK1/384
0	1	0	1	fosc/256	f _{CK} 1/256

Note: When are setting (PF0, PF1, PF2, PF3)=(1, 1, 0, 1) and (X, X, 1, 1), the frame frequency is same as frame frequency at the time of the (PF0, PF1, PF2, PF3)=(1, 0, 1, 0) setting (fosc/896, f_{CK1/896}).

X: don't care

(11) P1A, P1B to P12A, P12B ... General-purpose output function/PWM output function switiching control data of the general-purpose output port

These control data bits set the general-purpose output function (High or low level output) or PWM output function of the general-purpose output ports P1 to P12. However, when the S1/P1 to S12/P12 output pins arn't set the general-purpose output port, these control data bits become invalid. In addition, be careful of being unable to set a PWM output function when the external clock operating frequency is set the $f_{CK}2=38[kHz]typ$ (EXF="1") in external clock operating mode (OC= "1").

PnA	PnB	Functions of the general-purpose output port (Pn)
0	0	General-purpose output function (High or low level output)
1	0	PWM output function (Ch1)
0	1	PWM output function (Ch2)
1	1	PWM output function (Ch3)

Note: The data PnA, PnB (n=1 to 12) are the control data switching the general-purpose output function or PWM output function of the general-purpose output ports P1 to p12. For example, if the S10/P10 output pin is set the general-purpose output port, the general-purpose output port P10 pin is selected the PWM output function (Ch1) when (P10A, P10B)=(1, 0). However, in the case of the LC75890E(QIP44M), the control data are effective for only P1A, P1B to P11A, P11B.

(12) P0 to P3 ... Segment output port/general-purpose output port switching control data

These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S12/P12 output pins.

512/1	12 0	uipui	pino.												
	Contro	ol data			Output pin state										
P0	P1	P2	P3	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8	S9/P9	S10/P10	S11/P11	S12/P12
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	0	1	P1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	0	P1	P2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	1	P1	P2	P3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	1	0	0	P1	P2	P3	P4	S5	S6	S7	S8	S9	S10	S11	S12
0	1	0	1	P1	P2	P3	P4	P5	S6	S7	S8	S9	S10	S11	S12
0	1	1	0	P1	P2	P3	P4	P5	P6	S7	S8	S9	S10	S11	S12
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	S8	S9	S10	S11	S12
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8	S9	S10	S11	S12
1	0	0	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	S10	S11	S12
1	0	1	0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	S11	S12
1	0	1	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	S12
1	1	0	0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12

Note1: Sn (n=1 to 12)...Segment output port Pn (n=1 to 12)...General-purpose output port

Note2: In the case of the LC75890E(QIP44M), the output pins are effective for only S1/P1 to S11/P11 pins.

Note3: When are setting (P0, P1, P2, P3)=(1, 1, 0, 1), (1, 1, 1, 0) and (1, 1, 1, 1), the all S1/P1 to S12/P12 output pins are selected the segment output port.

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports (general-purpose output function).

Output air	Corresponden	ce display data		
Output pin	1/4 duty drive	Static drive		
S1/P1	D1	D1		
S2/P2	D5	D2		
S3/P3	D9	D3		
S4/P4	D13	D4		
S5/P5	D17	D5		
S6/P6	D21	D6		
S7/P7	D25	D7		
S8/P8	D29	D8		
S9/P9	D33	D9		
S10/P10	D37	D10		
S11/P11	D41	D11		
S12/P12	D45	D12		

For example, if the circuit is operated in 1/4 duty and the S4/P4 output pin is selected to be a general-purpose output port and is set general-purpose output function, the S4/P4 output pin will output a high (V_{LCD}) level when the display data D13 is 1, and will output a low (V_{SS}) level when D13 is 0.

Display Data and Display Blinking Control Data and Output Pin Correspondence (1/4 Duty Drive)

Output pin	COM1	COM2	COM3	COM4	Blinking control data	Output pin	COM1	COM2	COM3	COM4	Blinking control data
S1/P1	D1	D2	D3	D4	BD1	S19	D73	D74	D75	D76	BD19
S2/P2	D5	D6	D7	D8	BD2	S20	D77	D78	D79	D80	BD20
S3/P3	D9	D10	D11	D12	BD3	S21	D81	D82	D83	D84	BD21
S4/P4	D13	D14	D15	D16	BD4	S22	D85	D86	D87	D88	BD22
S5/P5	D17	D18	D19	D20	BD5	S23	D89	D90	D91	D92	BD23
S6/P6	D21	D22	D23	D24	BD6	S24	D93	D94	D95	D96	BD24
S7/P7	D25	D26	D27	D28	BD7	S25	D97	D98	D99	D100	BD25
S8/P8	D29	D30	D31	D32	BD8	S26	D101	D102	D103	D104	BD26
S9/P9	D33	D34	D35	D36	BD9	S27	D105	D106	D107	D108	BD27
S10/P10	D37	D38	D39	D40	BD10	S28	D109	D110	D111	D112	BD28
S11/P11	D41	D42	D43	D44	BD11	S29	D113	D114	D115	D116	BD29
S12/P12	D45	D46	D47	D48	BD12	S30	D117	D118	D119	D120	BD30
S13	D49	D50	D51	D52	BD13	S31	D121	D122	D123	D124	BD31
S14	D53	D54	D55	D56	BD14	S32	D125	D126	D127	D128	BD32
S15	D57	D58	D59	D60	BD15	S33	D129	D130	D131	D132	BD33
S16	D61	D62	D63	D64	BD16	S34	D133	D134	D135	D136	BD34
S17	D65	D66	D67	D68	BD17	S35	D137	D138	D139	D140	BD35
S18	D69	D70	D71	D72	BD18	S36	D141	D142	D143	D144	BD36
						S37/OSCI	D145	D146	D147	D148	BD37

Note: This table assumes that pins S1/P1 to S12/P12 and S37/OSCI are configured for segment output.

In addition, in the case of the LC75890E(QIP44M), the display data are effective for only D1 to D44, D49 to D92, D97 to D136, and D145 to D148, the display blinking control data are effective for only BD1 to BD11, BD13 to BD23, BD25 to BD34, and BD37. (In the case of the LC75890E(QIP44M), the output pins are effective for only S1/P1 to S11/P11, S13 to S23, S25 to S34, and S37/OSCI pins.)

For example, the table below lists the output states for the S21 output pin.

	Displa	y data		Blinking control data	
D81	D82	D83	D84	BD21	Output pin (S21) state
0	0	0	0	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	0	0	1	0	The LCD segment corresponding to COM4 is on.
0	0	1	0	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	0	The LCD segments corresponding to COM3 and COM4 are on.
0	1	0	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	0	The LCD segments corresponding to COM2 and COM4 are on.
0	1	1	0	0	The LCD segments corresponding to COM2 and COM3 are on.
0	1	1	1	0	The LCD segments corresponding to COM2, COM3, and COM4 are on.
1	0	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	0	The LCD segments corresponding to COM1 and COM4 are on.
1	0	1	0	0	The LCD segments corresponding to COM1 and COM3 are on.
1	0	1	1	0	The LCD segments corresponding to COM1, COM3, and COM4 are on.
1	1	0	0	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	0	1	0	The LCD segments corresponding to COM1, COM2, and COM4 are on.
1	1	1	0	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
1	1	1	1	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.
0	0	0	0	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	1	0	1	1	The LCD segments corresponding to COM2 and COM4 are blinking.
1	0	1	0	1	The LCD segments corresponding to COM1 and COM3 are blinking.
1	1	1	1	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are blinking.

Display Data and Display Blinking Control Data and Output Pin Correspondence (Static Drive)

Output pin	COM1	Blinking control data	Output pin	COM1	Blinking control data
S1/P1	D1	BD1	S19	D19	BD19
S2/P2	D2	BD2	S20	D20	BD20
S3/P3	D3	BD3	S21	D21	BD21
S4/P4	D4	BD4	S22	D22	BD22
S5/P5	D5	BD5	S23	D23	BD23
S6/P6	D6	BD6	S24	D24	BD24
S7/P7	D7	BD7	S25	D25	BD25
S8/P8	D8	BD8	S26	D26	BD26
S9/P9	D9	BD9	S27	D27	BD27
S10/P10	D10	BD10	S28	D28	BD28
S11/P11	D11	BD11	S29	D29	BD29
S12/P12	D12	BD12	S30	D30	BD30
S13	D13	BD13	S31	D31	BD31
S14	D14	BD14	\$32	D32	BD32
S15	D15	BD15	S33	D33	BD33
S16	D16	BD16	S34	D34	BD34
S17	D17	BD17	S35	D35	BD35
S18	D18	BD18	S36	D36	BD36
			S37/OSCI	D37	BD37

Note: This table assumes that pins S1/P1 to S12/P12 and S37/OSCI are configured for segment output. In addition, in the case of the LC75890E(QIP44M), the display data are effective for only D1 to D11, D13 to D23, D25 to D34, and D37, the display blinking control data are effective for only BD1 to BD11, BD13 to BD23, BD25 to BD34, and BD37. (In the case of the LC75890E(QIP44M), the output pins are effective for only S1/P1 to S11/P11, S13 to S23, S25 to S34, and S37/OSCI pins.)

For example, the table below lists the output states for the S21 output pin.

Display data	Blinking control data	Output pin (CO4) state
D21	BD21	Output pin (S21) state
0	0	The LCD segment corresponding to COM1 is off.
1	0	The LCD segment corresponding to COM1 is on.
0	1	The LCD segment corresponding to COM1 is off.
1	1	The LCD segment corresponding to COM1 is blinking.

Output waveforms (1/4-Duty 1/3-Bias Drive Scheme)

•						fo[Hz]										
С	OM1								≥	┍	┧┟					 VLCD 2/3VLCD 1/3VLCD 0V VLCD 	
С	OM2	┦			П	┢	Π	┟┦			F		2/3VLCD 1/3VLCD 0V				
С	OM3	1_1									<u>_</u>	_	 VLCD 2/3VLCD 1/3VLCD 0V VLCD 				
С	OM4				┶				┢	Ľ	┶┟			┢┑		2/3VLCD 1/3VLCD	
CC		ding to C	when all LCD segments COM1, COM2, COM3, and			_									1	0V VLCD 2/3VLCD 1/3VLCD 0V VLCD	
			when only LCD segments COM1 are on.			-								F -			
			when only LCD segments COM2 are on.		┪			IJ		ſ							
			when LCD segments COM1 and COM2 are on.											\square			
	LCD driver output when only LCD segments corresponding to COM3 are on.							IJ			╢						
			when LCD segments COM1 and COM3 are on.			1_					╢					2/3VLCD 1/3VLCD 0V	
L(co	CD drive orrespon	r output v ding to C	when LCD segments COM2 and COM3 are on.		┧			Ľ		ſ						VLCD 2/3VLCD 1/3VLCD 0V	
CC		•	when LCD segments COM1, COM2, and COM3													VLCD 2/3VLCD 1/3VLCD 0V	
	LCD driver output when only LCD segments corresponding to COM4 are on.					-		Γ				┓				VLCD 2/3VLCD 1/3VLCD 0V	
	LCD driver output when LCD segments corresponding to COM2 and COM4 are on.							Γ		J						VLCD 2/3VLCD 1/3VLCD 0V	
LCD driver output when all LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.					IJ			Г	ſ		IJ					VLCD 2/3VLCD 1/3VLCD 0V	
С	control dat	a	Com	nmon/	/segm	nent o	outpu	t wav	/efor	m fra	me fr	eque	ncy fo	o[Hz]			
FC0	FC1	FC2	Internal oscillator operating mod (The control data OC is 0, fosc=300[kHz]typ)	/segment output waveform frame frequer External clock operating mode (The control data OC is 1 and EXF is 0, f _{CK} 1=300[kHz]typ)						External clock operating mode (The control data OC is 1 and EXF is 1, f _{CK} 2=38[kHz]typ)							
0	0	0	fosc/4608			f _{CK} 1/4608						f _{CK} 2/576					
0	0	1	fosc/3456			f _{CK} 1/3456						fCK ^{2/432}					
0	1	0	fosc/3072	_	f _{CK} 1/3072						f _{CK} 2/384						
0	1	1	fosc/2304				f	CK1	/230	4			f _{CK} 2/288				
1	0	0	fosc/1536										f _{CK} 2/192				
	-			f _{CK} 1/1536													

Note: When is setting (FC0, FC1, FC2)=(1, 1, 1), the frame frequency is same as frame frequency at the time of the (FC0, FC1, FC2)=(0, 1, 0) setting (fosc/3072, f_{CK}1/3072, f_{CK}2/384).

fosc/1152

fosc/768

0

1

1

0

1

1

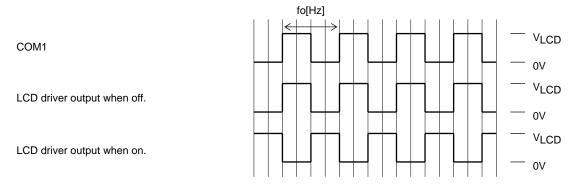
f_{CK}1/1152

fCK1/768

f_{CK}2/144

f_{CK}2/96

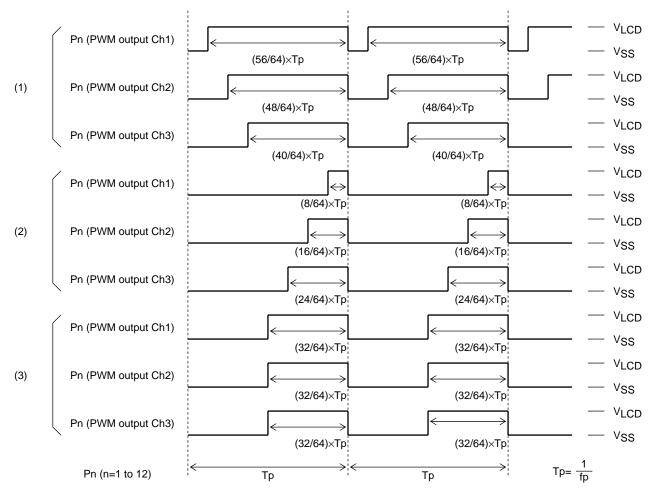
Output waveforms (Static Drive Scheme)



C	Control dat	a	Common/segment output waveform frame frequency fo[Hz]							
FC0	FC1	FC2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 1, f _{CK} 2=38[kHz]typ)						
0	0	0	fosc/4608	f _{CK} 1/4608	f _{CK} 2/576					
0	0	1	fosc/3456	f _{CK} 1/3456	f _{CK} 2/432					
0	1	0	fosc/3072	f _{CK} 1/3072	f _{CK} 2/384					
0	1	1	fosc/2304	f _{CK} 1/2304	f _{CK} 2/288					
1	0	0	fosc/1536	f _{CK} 1/1536	f _{CK} 2/192					
1	0	1	fosc/1152	fCK ^{1/1152}	fCK ^{2/144}					
1	1	0	fosc/768	f _{CK} 1/768	f _{CK} 2/96					

Note: When is setting (FC0, FC1, FC2)=(1, 1, 1), the frame frequency is same as frame frequency at the time of the (FC0, FC1, FC2)=(0, 1, 0) setting (fosc/3072, f_{CK}1/3072, f_{CK}2/384).

PWM output waveforms



Control data										PWM output								
W10	W11	W12	W13	W14	W15	W20	W21	W22	W23	W24	W25	W30	W31	W32	W33	W34	W35	waveforms
1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0	0	1	(1)
1	1	1	0	0	0	1	1	1	1	0	0	1	1	1	0	1	0	(2)
1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0	(3)

	Contro	ol data		PWM output waveform frame frequency fp[Hz]					
PF0	PF1	PF2	PF3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, f _{CK} 1=300[kHz] typ)				
0	0	0	0	fosc/1536	f _{CK} 1/1536				
1	0	0	0	fosc/1408	f _{CK} 1/1408				
0	1	0	0	fosc/1280	f _{CK} 1/1280				
1	1	0	0	fosc/1152	f _{CK} 1/1152				
0	0	1	0	fosc/1024	f _{CK} 1/1024				
1	0	1	0	fosc/896	f _{CK} 1/896				
0	1	1	0	fosc/768	f _{CK} 1/768				
1	1	1	0	fosc/640	f _{CK} 1/640				
0	0	0	1	fosc/512	f _{CK} 1/512				
1	0	0	1	fosc/384	f _{CK} 1/384				
0	1	0	1	fosc/256	f _{CK} 1/256				

Note1: When is setting (PF0, PF1, PF2, PF3)=(1, 1, 0, 1) and (X, X, 1, 1), the frame frequency is same as frame frequency at the time of the (PF0, PF1, PF2, PF3)=(1, 0, 1, 0) setting (fosc/896, f_{CK}1/896). X: don't care Note2: In the case of the LC75890E(QIP44M), the output pins are effective for only P1 to P11 pins.

Display Control and the INH Pin

Since the LSI internal data (1/4 duty drive : the display data D1 to D148 and the control data, Static drive : the display data D1 to D37 and the control data) is undefined when power is first applied, applications should set the INH pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S12/P12, S13 to S36, COM4 to COM1, and S37/OSCI pins to the VSS level.) and during this period send serial data from the controller. The controller should then set the INH pin high after the data transfer has completed. This procedure prevents meaningless display at power on.

(See Figure 4 and Figure 5.)

Notes on the Power On/Off Sequences

Applications should observe the following sequences when turning the LC75890 power on and off. (See Figures 4 and Figure 5.)

• At power on : Logic block power supply (V_DD) on \rightarrow LCD driver block power supply (V_LCD) on

• At power off : LCD driver block power supply (V_{LCD}) off \rightarrow Logic block power supply (V_{DD}) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

(1)1/4 duty drive				t2	
V _{DD}				$ \longleftrightarrow $	t3
V _{LCD}					
ĪNH			≁VIL1		
CE	Display da	ata and control	← ⊫1		
Internal data BD1 to BD37,BF0 to BF2, FC0 to FC2,DT,EXF,OC,SC,BU	Undefined	ransferred	Defined		Undefined
Internal data W10 to W15,W20 to W25, W30 to W35,PF0 to PF3,P1A, P1B to P12A,P12B,P0 to P3	Undefined		Defined ∦	X	Undefined
Internal data (D1 to D48)	Undefined		Defined		Undefined
Internal data (D49 to D96)	Undefined	χ	Defined ∦		Undefined
Internal data (D97 to D148)	Undefined	χ	 Defined	X	Undefined

Note1 : t1≥0 t2>0

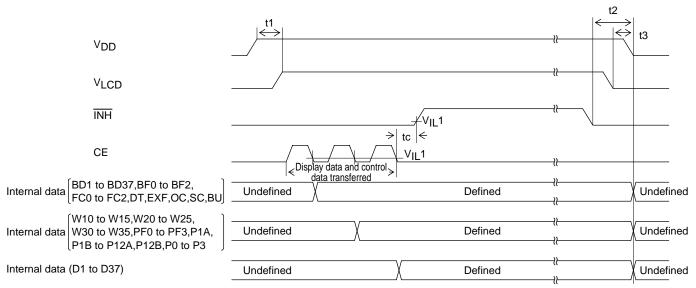
t3≥0 (t2>t3)

tc ... 10µs min

Note2 : In the case of the LC75890E(QIP44M), the display data are effective for only D1 to D44, D49 to D92, D97 to D136, and D145 to D148, the display blinking control data are effective for only BD1 to BD11, BD13 to BD23, BD25 to BD34, and BD37, and the general-purpose output function/PWM output function switching control data of the general-purpose output port are effective for only P1A, P1B to P11A, P11B.

[Figure 4]

(2)Static drive



Note1 : t1≥0

t2>0

t3≥0 (t2>t3)

tc ... 10µs min

Note2 : In the case of the LC75890E(QIP44M), the display data are effective for only D1 to D11, D13 to D23, D25 to D34, and D37, the display blinking control data is effective for only BD1 to BD11, BD13 to BD23, BD25 to BD34, and BD37, and the general-purpose output function/PWM output function switching control data of the general-purpose output port are effective for only P1A, P1B to P11A, P11B.

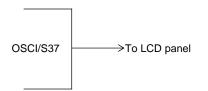
[Figure 5]

Notes on Controller Transfer of Display Data

When using the LC75890 in 1/4 duty, applications transfer the display data (D1 to D148) in three operations. In either case, applications should transfer all of the display data within 30 ms to maintain the quality of displayed image.

S37/OSCI Pin Peripheral Circuit

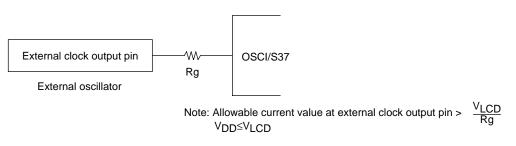
Internal oscillator operating mode (control data OC=0)
 Connect the S37/OSCI pin to the LCD panel when the internal oscillator operating mode is selected.



(2) External clock operating mode (control data OC=1)

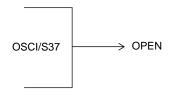
When the external clock operating mode is selected, insert a current protection resistor Rg (2.2 to $22k\Omega$) between the S37/OSCI pin and external clock output pin (external oscillator). Determine the value of the resistance according to the allowable current value at the external clock output pin. Also make sure that the waveform of the external clock is not heavily distorted.

In addition, the following conditions must be met : $V_{DD} \leq V_{LCD}$.



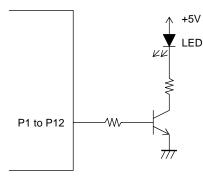
(3) Unused pin treatment

When the S37/OSCI pin is not to be used, select the internal oscillator operating mode (setting control data OC to 0) to keep the pin open.



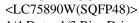
P1 to P12 pin peripheral circuit

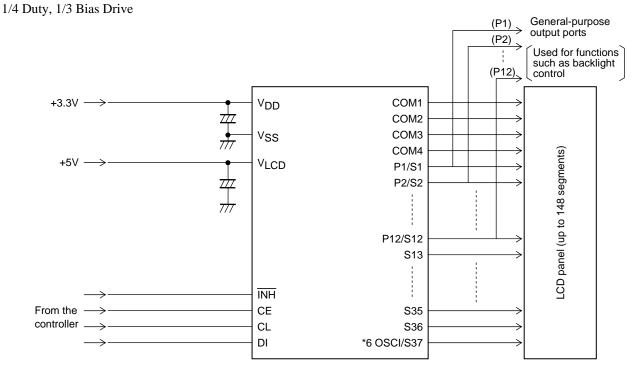
It is recommended the circuit shown below be used to adjust the brightness of the LED backlight using the PWM output P1 to P12



Note : In the case of the LC75890E(QIP44M), the output pins are effective for only P1 to P11 pins.

Sample Applications Circuit 1

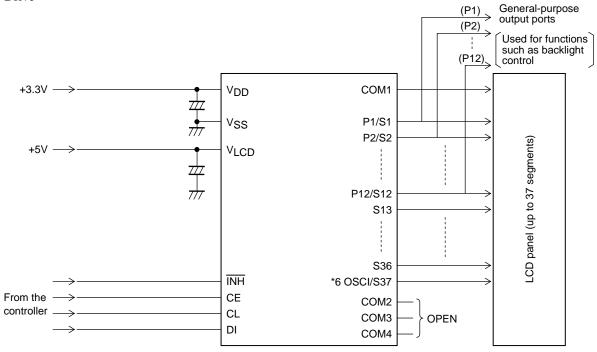




*6 Connect the S37/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor Rg(2.2 to 22kΩ) between the S37/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode. (See "S37/OSCI Pin Peripheral Circuit")

Sample Applications Circuit 2

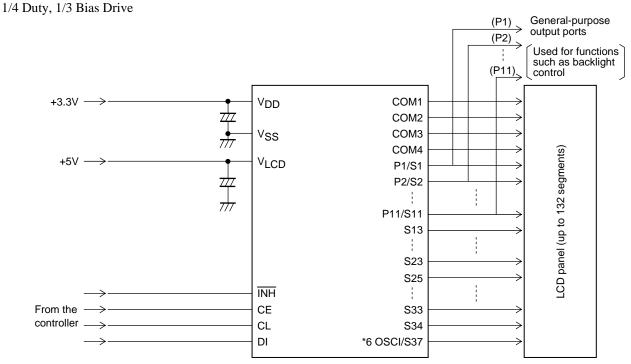
<LC75890W(SQFP48)> Static Drive



*6 Connect the S37/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor $Rg(2.2 \text{ to } 22k\Omega)$ between the S37/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode. (See "S37/OSCI Pin Peripheral Circuit")

Sample Applications Circuit 3

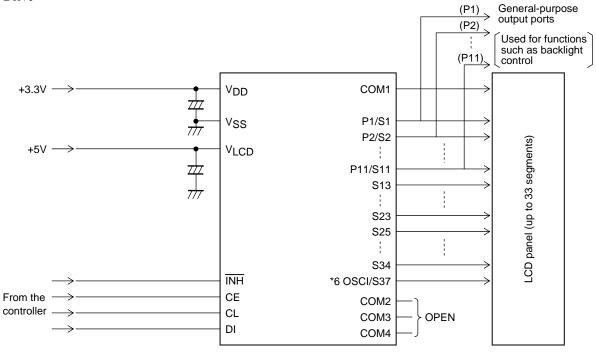
<LC75890E(QIP44M)>



*6 Connect the S37/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor Rg(2.2 to 22kΩ) between the S37/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode. (See "S37/OSCI Pin Peripheral Circuit")

Sample Applications Circuit 4

<LC75890E(QIP44M)> Static Drive



*6 Connect the S37/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor $Rg(2.2 \text{ to } 22k\Omega)$ between the S37/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode. (See "S37/OSCI Pin Peripheral Circuit")

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