Ordering number : EN*5937

CMOS IC

LC75386NE

Electronic Volume and Tone Control for Car Stereo Systems

Preliminary

Overview

The LC75386NE is an electronic volume and tone control IC that can implement a wide range of functions including volume, balance, fader, bass and treble controls, loudness, input switching, and input gain control with a minimal number of external components.

Functions

- Volume: 0 to –79 dB (in 1-dB steps) and –∞ for a total of 81 settings.
  A balance function can be implemented by controlling the left and right channel volume settings independently.
- Fader: The rear or the front outputs can be attenuated over 16 settings.
  (0 to –2 dB in 1-dB steps, –2 to –20 dB in 2 dB steps, –20 to –30 dB in 10-dB steps, –45 dB, -60 dB, and –∞ for a total of 16 settings.)
- Bass and treble: Control over a ±12-dB range in 2-dB steps in each band.
- Input gain: The input signal can be amplified from 0 to +18.75 dB (in 1.25-dB steps).
- Input switching: One of 6 inputs can be selected for each of the left and right channels. (Five are single-ended inputs, and one is a differential input.)
- Loudness: Taps are output from the –32-dB positions of the 2-dB step volume ladder resistors, and loudness operation can be implemented by attaching external capacitors.

Features

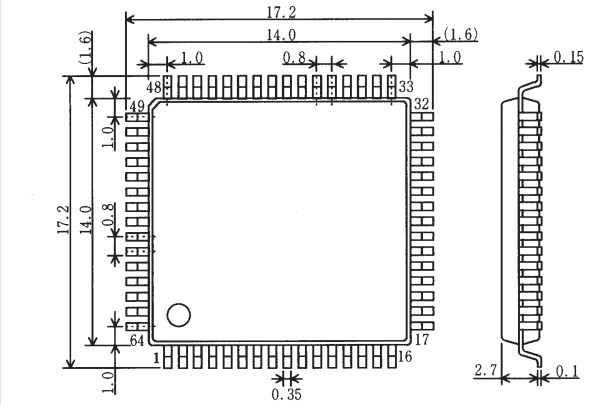
- On-chip buffer amplifiers minimize the number of external components required.
- The low level of switching noise generated from internal switches due to fabrication in a CMOS process minimizes switching noise when no input signals are present.
- The use of built-in zero-cross switching circuits minimizes switching noise when input signals are present.
- Built-in VDD/2 reference voltage generation circuit
- All controls are controlled from CCB serial data input.

Package Dimensions

unit: mm

3159-QFP64E

[LC75386NE]

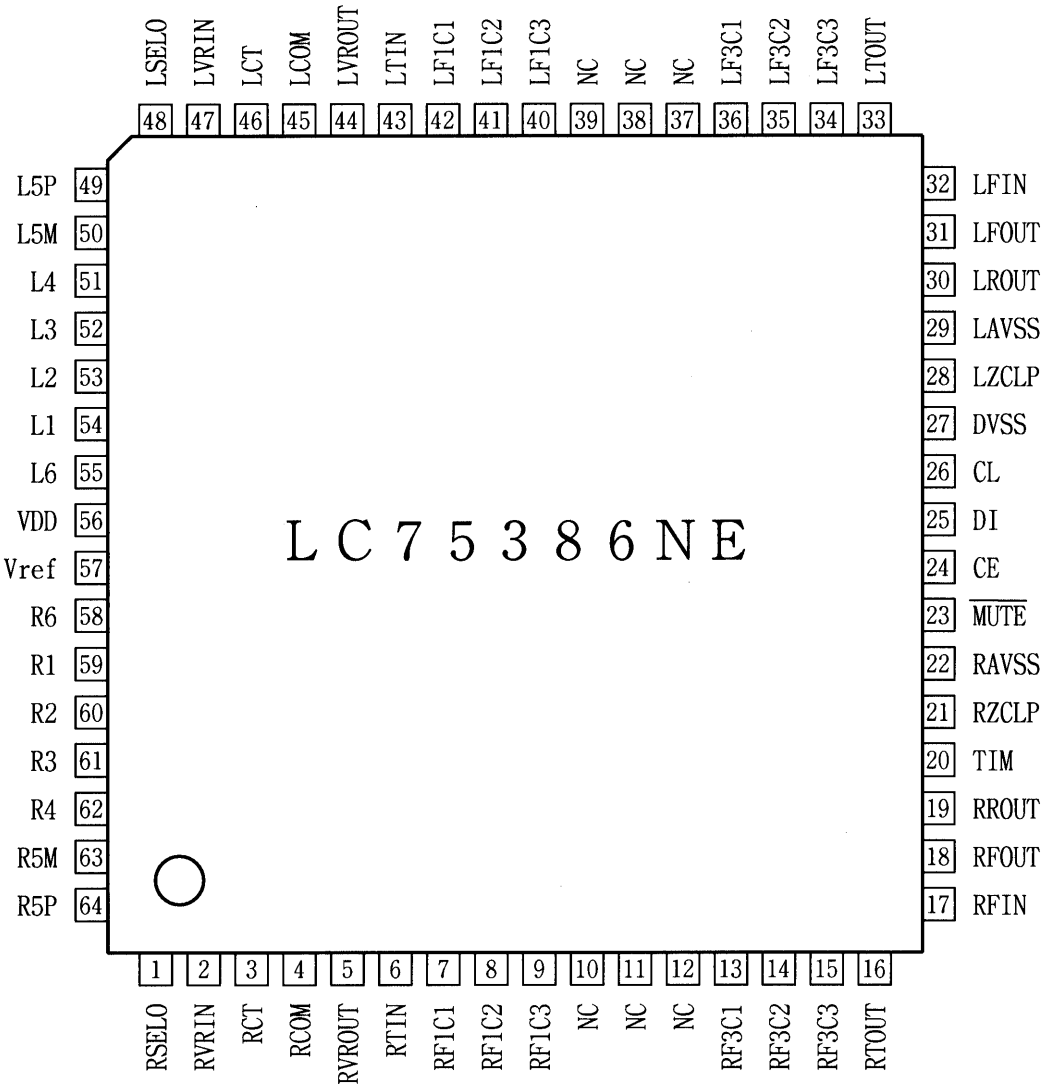


SANYO: QFP64E

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

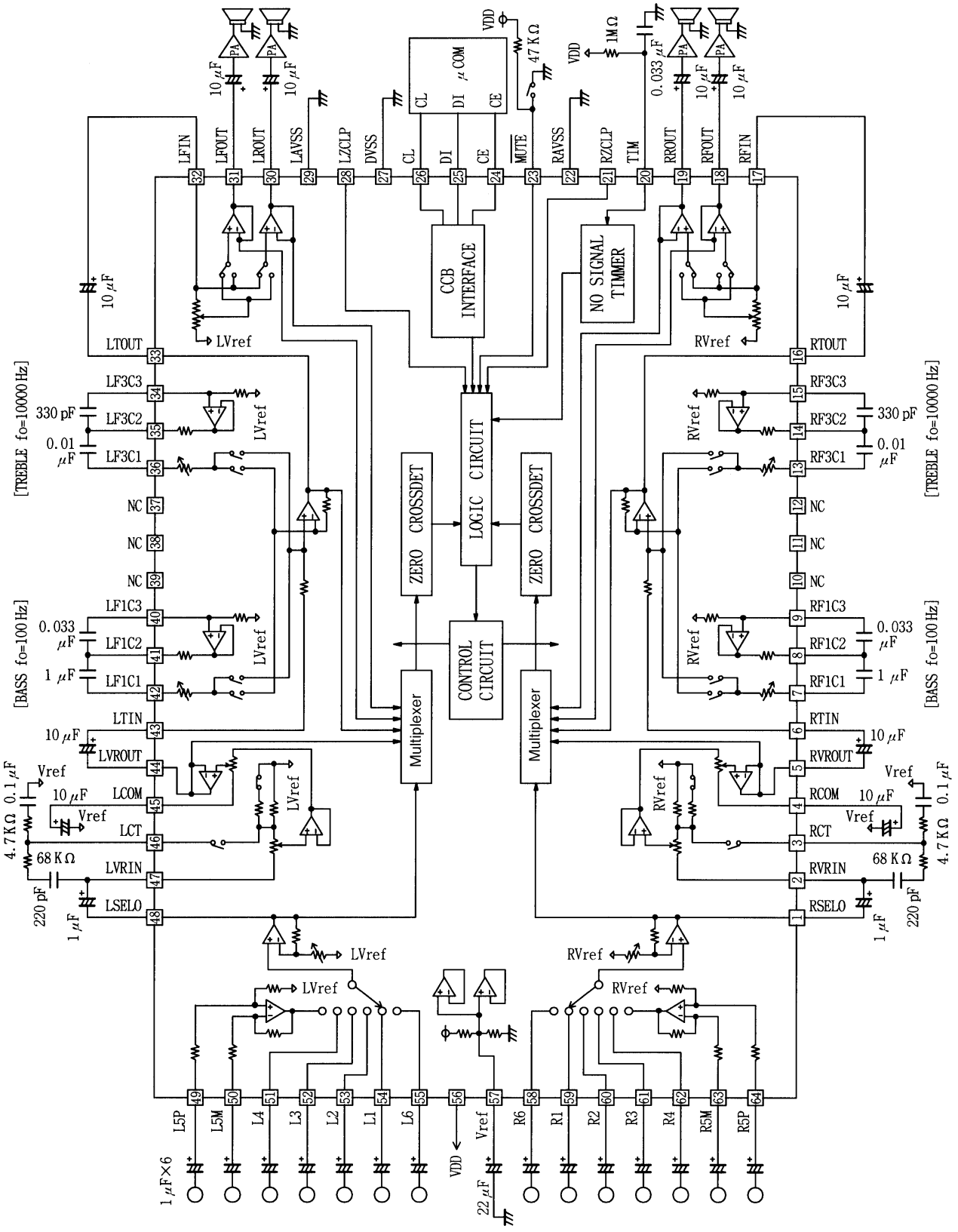
SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Pin Assignment



Top view

Equivalent Circuit and Application Circuit Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	11	V
Maximum input voltage	V_{IN} max	All input pins	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	6.0		10.5	V
High-level input voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Low-level input voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input amplitude	V_{IN}		V_{SS}		V_{DD}	Vp-p
Input pulse width	TøW	CL	1			µs
Setup time	Tsetup	CL, DI, CE	1			µs
Hold time	Thold	CL, DI, CE	1			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 9 V, V_{SS} = 0 V

Input Block

Parameter	Symbol	Applicable pins	Conditions	Ratings			Unit
				min	typ	max	
Input resistance	Rin	L1 to L4, L6, R1 to R4, R6		35	50	65	kΩ
Minimum input gain	Ginmin	L1 to L4, L6, R1 to R4, R6		–1	0	+1	dB
Maximum input gain	Ginmax			+16.5	+18.75	+21	dB
Inter-step setting error	ATerr					±0.6	dB
Left/right balance	BAL					±0.5	dB

Volume Control Block

Parameter	Symbol	Applicable pins	Conditions	Ratings			Unit
				min	typ	max	
Input resistance	Rvr	LVRIN, RVRIN, Loudness off		158	226	294	kΩ
Inter-step setting error	ATerr					±0.5	dB
Left/right balance	BAL					±0.5	dB

Tone Control Block

Parameter	Symbol	Applicable pins	Conditions	Ratings			Unit
				min	typ	max	
Inter-step setting error	ATerr					±1.0	dB
Bass control range	Gbass		max. boost/cut	±9	±12	±15	dB
Treble control range	Gtre		max. boost/cut	±9	±12	±15	dB
Left/right balance	BAL					±0.5	dB

Fader Control Block

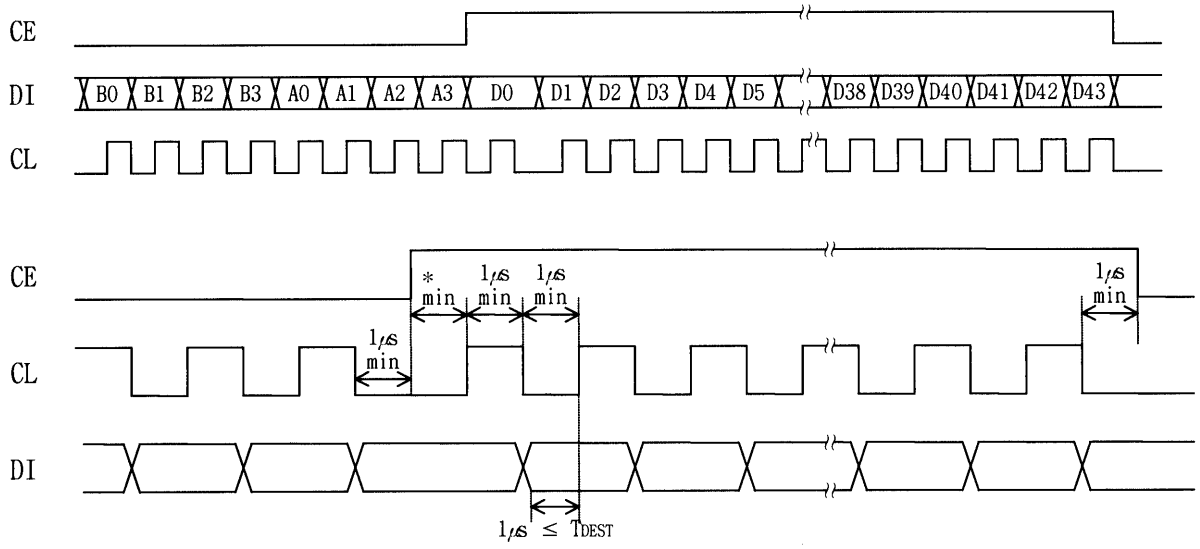
Parameter	Symbol	Applicable pins	Conditions	Ratings			Unit
				min	typ	max	
Input resistance	Rfed	LFIN, RFIN		25	50	100	kΩ
Inter-step setting error	ATerr		0 dB to –2 dB			±0.5	dB
			–2 dB to –20 dB			±1	dB
			–20 dB to –30 dB			±2	dB
			–30 dB to –60 dB			±3	dB
Left/right balance	BAL					±0.5	dB

Overall Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD1	V_{IN} = –10 dBV, f = 1 kHz		0.004	0.01	%
	THD2	V_{IN} = –10 dBV, f = 10 kHz		0.006	0.01	%
Inter-input crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz	80	88		dB
Left/right crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz	80	88		dB
Maximum attenuation	Vomin1	V_{IN} = 1 Vrms, f = 1 kHz	80	88		dB
	Vomin2	V_{IN} = 1 Vrms, f = 1 kHz, INMUTE, Fader: –∞	90	95		dB
Output noise voltage	VN1	All flat, IHF-A filter		5	10	μV
	VN2	All flat, 20 Hz to 20 kHz bandpass filter		7	15	μV
Current drain	I_{DD}			33	40	mA
High-level input current	I_{IH}	CL, DI, CE, V_{IN} = 9 V			10	μA
Low-level input current	I_{IL}	CL, DI, CE, V_{IN} = 0V	–10			μA
Maximum input voltage	V_{CL}	THD = 1%, RL = 10 kΩ, All flat, f_{IN} = 1 kHz	2.5	2.9		Vrms

Control System Timing and Data Format

The LC75386NE is controlled by inputting stipulated data serially to the CL, DI, and CE pins. The data consists of a total of 52 bits, of which 8 bits are the address and 44 bits are the actual control data.



Note*: The minimum value is determined by the value of the capacitor connected to the TIM pin (pin 20).

If the value of the capacitor is C_{TIM} and the minimum value is $T_D$min, then:

$T_D\text{min} = 3 \times 10^3 \times C_{TIM}$

If C_{TIM} is 0.033 μF, then:

$T_D\text{min} = 3 \times 10^3 \times 0.033 \times 10^{-6} \approx 100$ μs

• Address Code (B0 to A3)
The LC75386NE has an 8-bit address code and can be used on a bus shared with other Sanyo ICs.
Address Code

(LSB)

B0	B1	B2	B3	A0	A1	A2	A3
1	0	0	0	0	0	0	1

(81HEX)

• Control code allocation
Input Switching Control

D0	D1	D2		
0	0	0	L1 (R1)	
1	0	0	L2 (R2)	
0	1	0	L3 (R3)	
1	1	0	L4 (R4)	
0	0	1	L5 (R5)	
1	0	1	L6 (R6)	
0	1	1		IC test values: These values must not be used during normal operation.
1	1	1		

D3	IC test bit: This bit must be set to 0.

Input Gain Control

D4	D5	D6	D7	
0	0	0	0	0 dB
1	0	0	0	+1.25 dB
0	1	0	0	+2.50 dB
1	1	0	0	+3.75 dB
0	0	1	0	+5.00 dB
1	0	1	0	+6.25 dB
0	1	1	0	+7.50 dB
1	1	1	0	+8.75 dB
0	0	0	1	+10.0 dB
1	0	0	1	+11.25 dB
0	1	0	1	+12.5 dB
1	1	0	1	+13.75 dB
0	0	1	1	+15.0 dB
1	0	1	1	+16.25 dB
0	1	1	1	+17.5 dB
1	1	1	1	+18.75 dB

Volume Control

D8	D9	D10	D11	D12	D13	D14	D15	
								1 dB step
0								0 dB
1								–1 dB
								2 dB step
	0	0	0	0	0	0	0	0 dB
	1	0	0	0	0	0	0	–2 dB
	0	1	0	0	0	0	0	–4 dB
	1	1	0	0	0	0	0	–6 dB
	0	0	1	0	0	0	0	–8 dB
	1	0	1	0	0	0	0	–10 dB
	0	1	1	0	0	0	0	–12 dB
	1	1	1	0	0	0	0	–14 dB
	0	0	0	1	0	0	0	–16 dB
	1	0	0	1	0	0	0	–18 dB
	0	1	0	1	0	0	0	–20 dB
	1	1	0	1	0	0	0	–22 dB
	0	0	1	1	0	0	0	–24 dB
	1	0	1	1	0	0	0	–26 dB
	0	1	1	1	0	0	0	–28 dB
	1	1	1	1	0	0	0	–30 dB
	0	0	0	0	1	0	0	–32 dB
	1	0	0	0	1	0	0	–34 dB
	0	1	0	0	1	0	0	–36 dB
	1	1	0	0	1	0	0	–38 dB
	0	0	1	0	1	0	0	–40 dB
	1	0	1	0	1	0	0	–42 dB
	0	1	1	0	1	0	0	–44 dB
	1	1	1	0	1	0	0	–46 dB
	0	0	0	1	1	0	0	–48 dB
	1	0	0	1	1	0	0	–50 dB
	0	1	0	1	1	0	0	–52 dB
	1	1	0	1	1	0	0	–54 dB
	0	0	1	1	1	0	0	–56 dB
	1	0	1	1	1	0	0	–58 dB
	0	1	1	1	1	0	0	–60 dB
	1	1	1	1	1	0	0	–62 dB
	0	0	0	0	0	1	0	–64 dB
	1	0	0	0	0	1	0	–66 dB
	0	1	0	0	0	1	0	–68 dB
	1	1	0	0	0	1	0	–70 dB
	0	0	1	0	0	1	0	–72 dB
	1	0	1	0	0	1	0	–74 dB
	0	1	1	0	0	1	0	–76 dB
	1	1	1	0	0	1	0	–78 dB
								Mute
	1	1	1	1	1	1	0	–∞
	0	1	1	1	1	1	0	Inmute

Tone Control

D16	D17	D18	D19	Bass
D24	D25	D26	D27	Treble
0	1	1	0	+12 dB
1	0	1	0	+10 dB
0	0	1	0	+8 dB
1	1	0	0	+6 dB
0	1	0	0	+4 dB
1	0	0	0	+2 dB
0	0	0	0	0 dB
1	0	0	1	–2 dB
0	1	0	1	–4 dB
1	1	0	1	–6 dB
0	0	1	1	–8 dB
1	0	1	1	–10 dB
0	1	1	1	–12 dB

D20	D21	D22	D23	
0	0	0	0	These bits must be set to 0

Fader Volume Control

D28	D29	D30	D31	
0	0	0	0	0 dB
1	0	0	0	–1 dB
0	1	0	0	–2 dB
1	1	0	0	–4 dB
0	0	1	0	–6 dB
1	0	1	0	–8 dB
0	1	1	0	–10 dB
1	1	1	0	–12 dB
0	0	0	1	–14 dB
1	0	0	1	–16 dB
0	1	0	1	–18 dB
1	1	0	1	–20 dB
0	0	1	1	–30 dB
1	0	1	1	–45 dB
0	1	1	1	–60 dB
1	1	1	1	–∞

Channel Selection Control

D32	D33	
0	0	Initial setup mode: rapid charging
1	0	RCH
0	1	LCH
1	1	Left and right together

Fader Rear/Front Control

D34	
0	Rear
1	Front

Loudness Control

D35	
0	Off
1	On

Zero Cross Control

D36	D37	
0	0	Data written when a zero crossing is detected
1	1	Zero cross detection disabled (Data is written when CE falls)

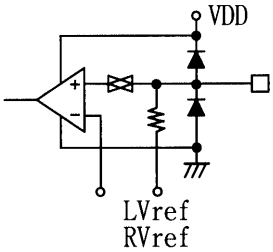
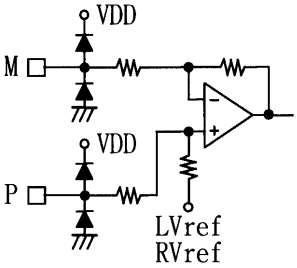
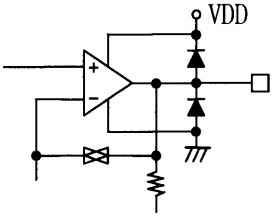
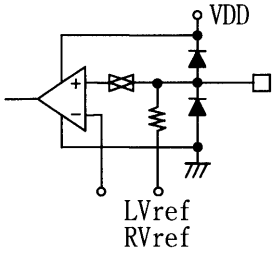
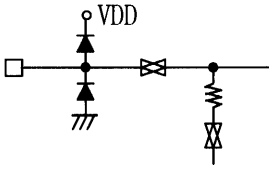
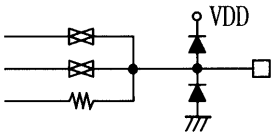
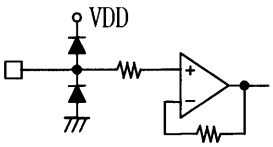
Zero Cross Signal Detection Block Control

D38	D39	D40	D41	
0	0	0	0	Selector
1	0	0	0	Volume
0	1	0	0	Tone
1	1	0	0	Fader

Test Mode Control

D42	D43	
0	0	This bit is used for IC testing and must be set to 0

Pin Descriptions

Pin No.	Pin name	Function	Notes
54 53 52 51 55 59 60 61 62 58	L1 L2 L3 L4 L6 R1 R2 R3 R4 R6	• Single-ended inputs	
50 49 63 64	L5M L5P R5M R5P	• Differential inputs	
48 1	LSEL0 RSEL0	• Input selector outputs	
47 2	LVRIN RVRIN	• 2-dB step volume control inputs • Input signals must be provided from a low-impedance circuit.	
46 3	LCT RCT	• Loudness connections. Connect the high-band compensation CR circuit between LCT (RCT) and LVRIN (RVRIN), and connect the low-band compensation CR circuit between LCT (RCT) and Vref.	
45 4	LCOM RCOM	• 2-dB step volume control outputs • Connect these pins to Vref through coupling capacitors to reduce switching noise.	
43 6	LTIN RTIN	• Equalizer inputs	

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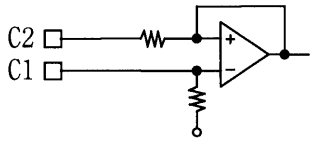
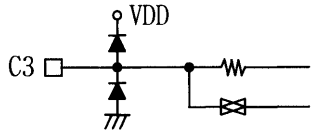
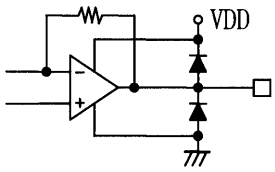
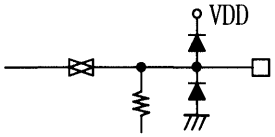
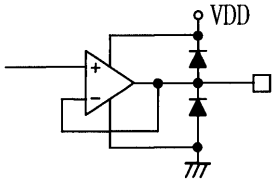
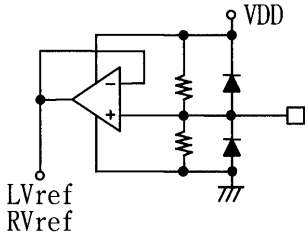
Pin No.	Pin name	Function	Notes
42 41 40 7 8 9	LF1C1 LF1C2 LF1C3 RF1C1 RF1C2 RF1C3	• Connections for the capacitors that form the filters used for tone circuit low band. Connect capacitors between: LF1C1 (RF1C1) and LF1C2 (RF1C2), and between LF1C2 (RF1C2) and LF1C3 (RF1C3).	
36 35 34 13 14 15	LF3C1 LF3C2 LF3C3 RF3C1 RF3C2 RF3C3	• Connections for the capacitors that form the filters used for tone circuit high band. Connect capacitors between: LF3C1 (RF3C1) and LF3C2 (RF3C2), and between LF3C2 (RF3C2) and LF3C3 (RF3C3).	
39 38 37 10 11 12	NC NC NC NC NC NC	• Unused pins. These pins are not connected to any part of the IC.	
33 16	LTOUT RTOUT	• Equalizer outputs	
32 17	LFIN RFIN	• Fader block inputs • These pins must be driven by low-impedance circuits.	
31 30 18 19	LFOUT LROUT RFOUT RROUT	• Fader outputs. The front and rear signals are attenuated separately. The amount of the attenuation is the same in the left and right channels.	
57	Vref	• A capacitor with a value of a few tens of µF must be connected between Vref and AV_{SS} (V_{SS}) to reduce power supply ripple in the V_{DD}/2 voltage generation block.	
56	V_{DD}	• Power supply	
27	DV_{SS}	• Logic system ground	
29 22	LAV_{SS} RAV_{SS}	• Analog system ground	

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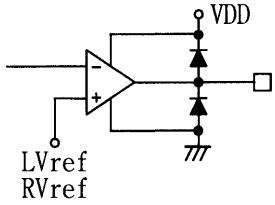
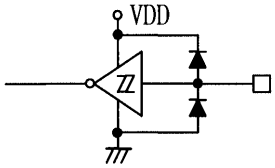
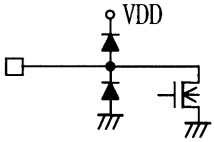
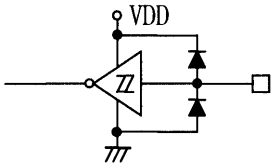
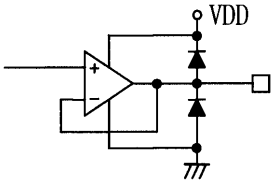
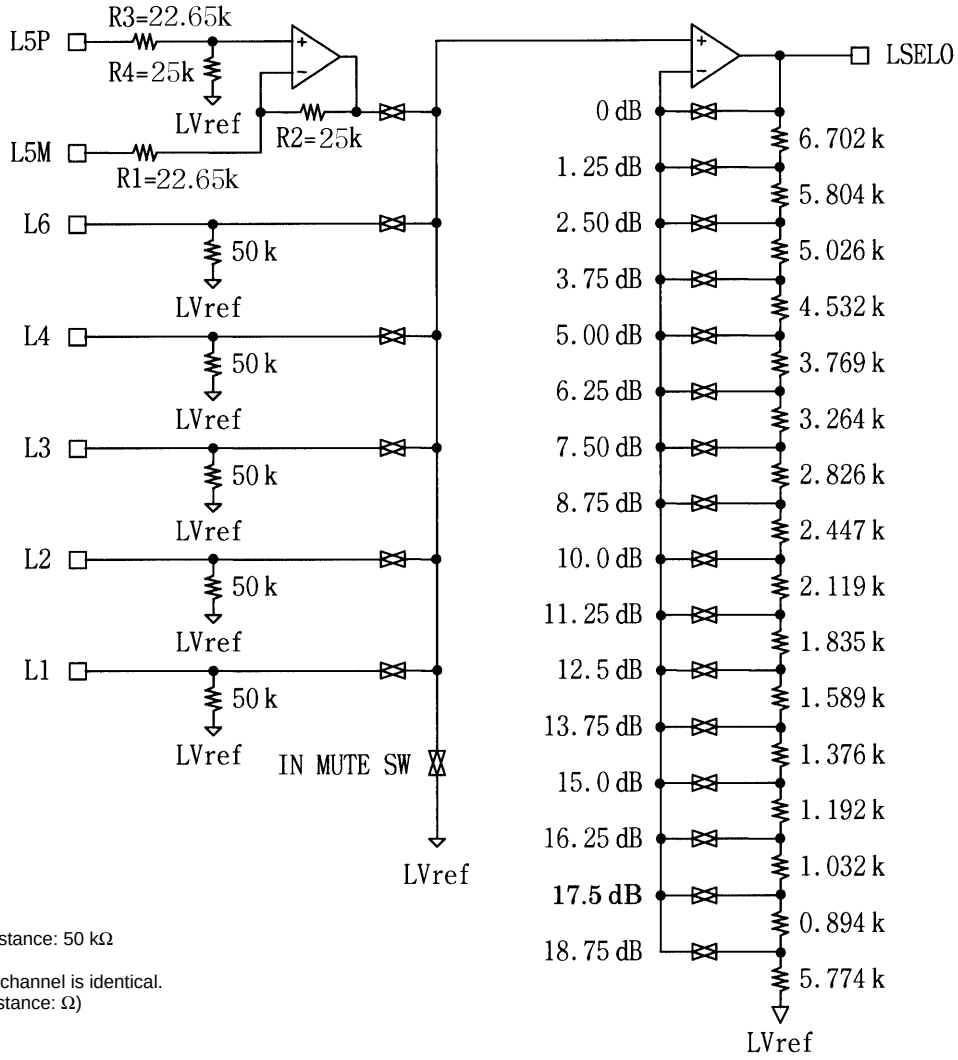
Pin No.	Pin	Function	Notes
28 21	LZCLP RZCLP	• Zero cross detector circuit band control	
23	$\overline{\text{MUTE}}$	• Externally controlled muting input • Setting this pin to the V_{SS} level forcibly sets the fader volume block to the –∞ setting.	
20	TIM	• Time control for the zero cross circuit when no signal is present If there is no zero cross signal between the point the data is loaded and the point the time defined by this pin elapses, the data is loaded forcibly.	
26 25	CL DI	• Serial data and clock input for chip control	
24	CE	• Chip enable. Data is written to the internal latch when this pin is switched from high to low, and the analog switches operate.Transfer data becomes enable when this pin is at high level.	
44 5	LVROUT RVROUT	• 1-dB step volume control outputs	

Internal Equivalent Circuits

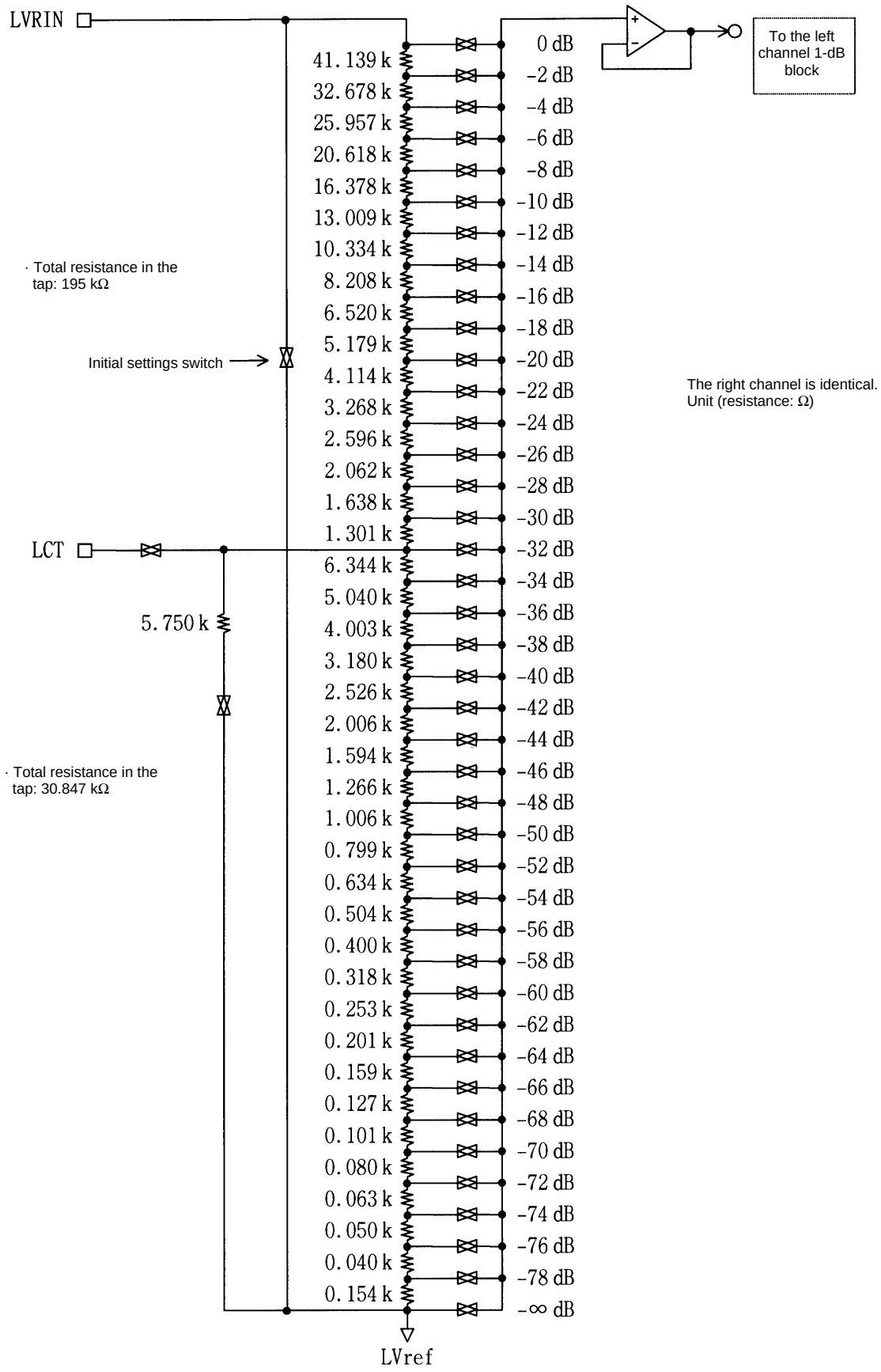
Selector Block Equivalent Circuit



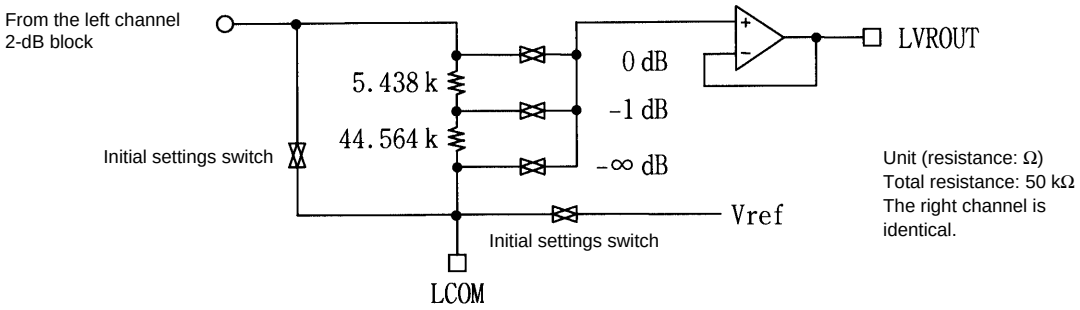
Total resistance: 50 kΩ

The right channel is identical.
Unit (resistance: Ω)

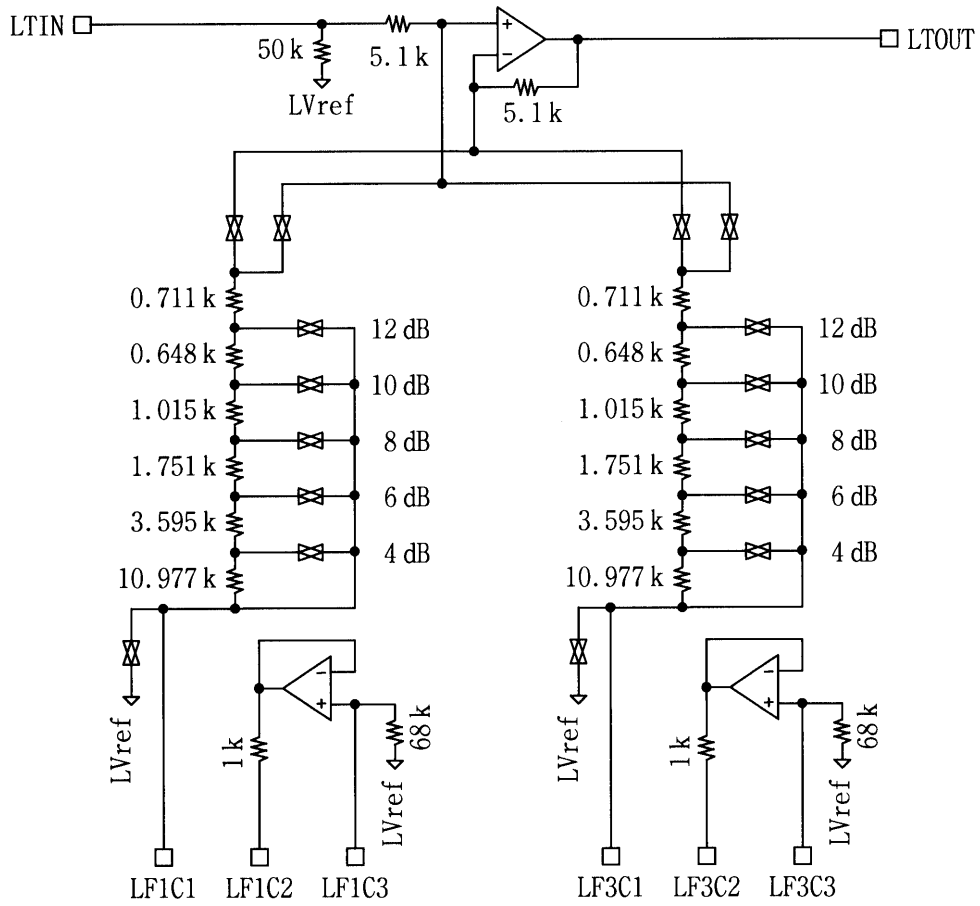
2-dB Volume Control Block Equivalent Circuit



1-dB Volume Control Block Equivalent Circuit



Tone Control Block Equivalent Circuit

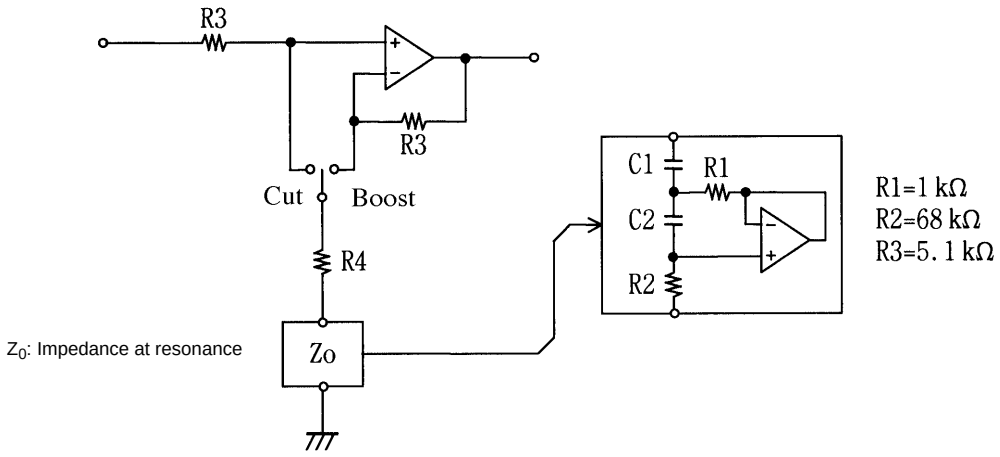


Unit (resistance: Ω)

External Capacitor Calculations

The LC75386NE external capacitors are the structural components in semiconductor inductors, i.e. simulated inductors. This section presents the equivalent circuit and the formulas used to calculate the desired center frequencies.

Semiconductor inductor equivalent circuit



Sample calculation

Specifications: 1. Center frequency: F_0 = 100 Hz

2. Q at maximum boost: Q_{+12dB} = 0.9

• Determine the sharpness, Q_0, of the semiconductor inductor.

$$Q_0 = \frac{(R1 + R4)}{R1} \times Q_{+12dB} \approx 1.53999$$

• Determine C1.

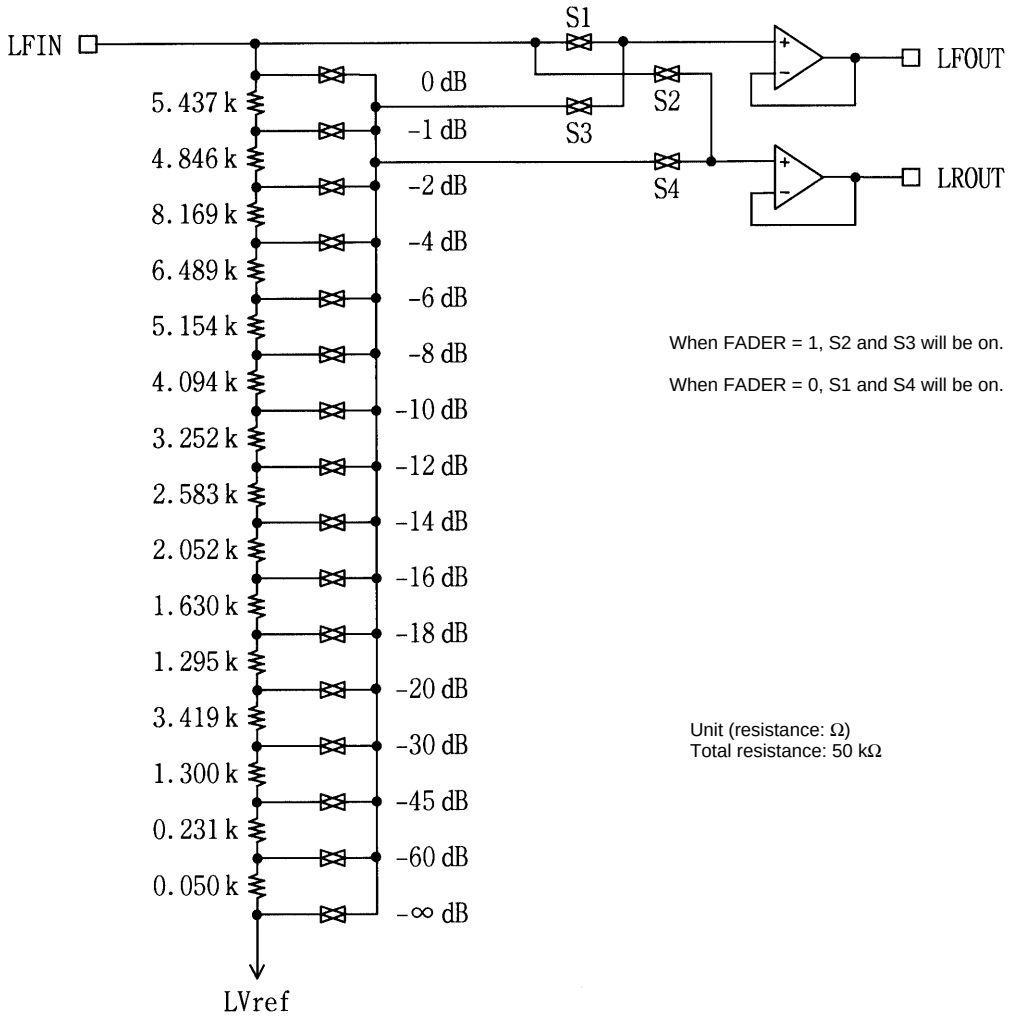
$$C1 = 1/2\pi\, F_O R1 Q_O \neq 1\ (\mu F)$$

• Determine C2.

$$C2 = Q_O/2\pi\, F_O R2 \neq 0.036\ (\mu F)$$

Note: See the tone control block equivalent circuit diagram in page 15 for the internal resistance.

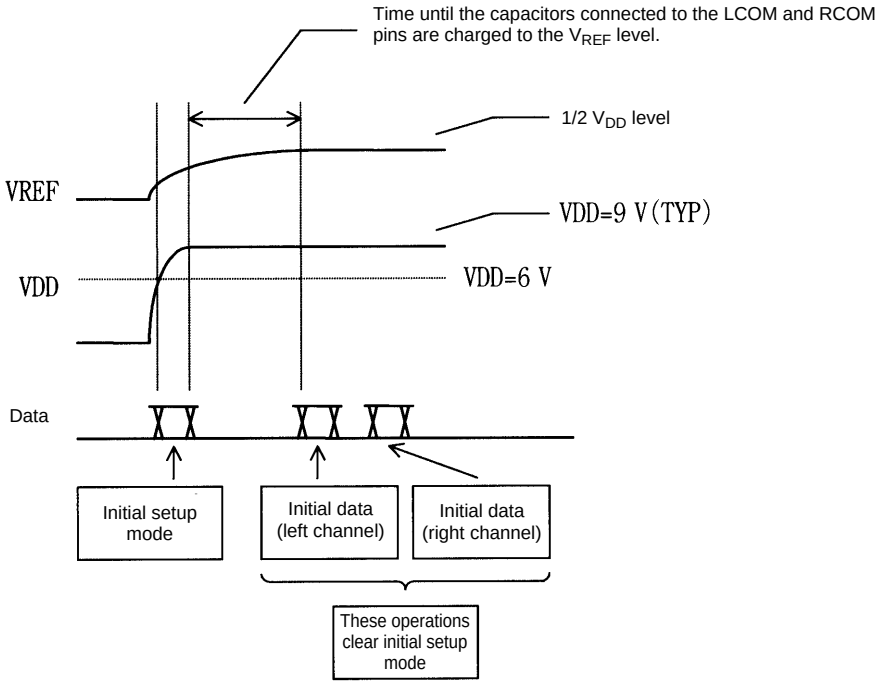
Fader Volume Control Block Equivalent Circuit



If data corresponding to a –∞ is send to the 1-dB step main volume, S1 and S2 will be set open and S3 and S4 will be turned on at the same time.

Usage Notes

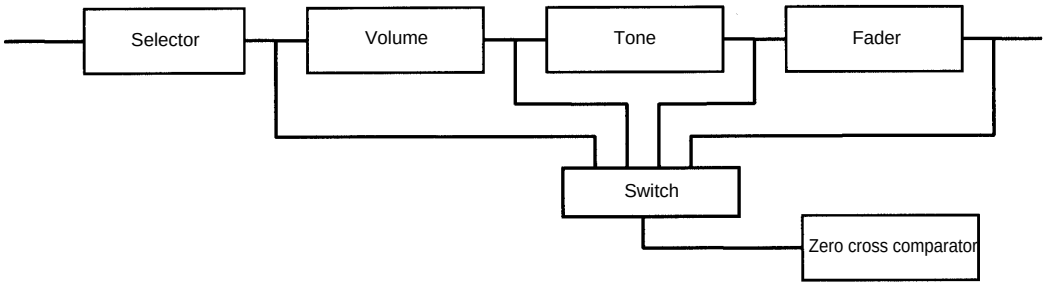
- Notes on data transfer when power is first applied
  - The states of the internal analog switches are undefined when power is first applied. Until the control data has been set up, applications must mute signals appropriately.
  - Applications should send initial setup data to quickly stabilize the bias levels in each block when power is first applied.
- The period between initial setup mode and initial data setup
  - Applications should transfer the initial setup data after the power-supply voltage V_{DD} exceeds 6 V.
  - Send initial data (that turns the rapid charging switches off) after the LCOM, RCOM, and VREF pin levels have stabilized.



- Procedure for transferring the initial setup data
  Quick charge mode is set up when D32 and D33 are set to 00. Since the other data (D0 to D31, and D34 to D43) is set up for the left and right channels at the same time, the states of the other blocks can be set at the same time.
- Procedure for clearing the initial setup data
  Quick charge mode is cleared when D32 and D33 are set to a value other than 00, that is when normal left/right channel operation is specified.

Operating Principles of the Zero Cross Switching Circuit

The LC75386NE provides a function that switches the signal detection location of the zero cross comparator. This means an optimal location for block for data update can be selected. Basically, switching noise can be minimized by inputting the signal from immediately after the block that modifies the data to the zero cross comparator. Therefore, the detection location needs to be changed each time the IC control settings are changed.



Zero Cross Detection Circuit

Zero Cross Switching Control

Zero cross switching is controlled by setting the zero cross control bits to zero cross detection mode (by setting both D36 and D37 to 0), specifying the detection block (with bits D38, D39, D40, and D41), and transferring the data. Since these control bits are latched immediately after the data is transferred, that is, on the falling edge of the CE signal, when volume and other setting data is changed, it is possible to also set the mode and the zero cross operation at the same time in a single data transfer operation. The example below shows a control pattern that can be used at the same time as the volume setting data is updated.

D36	D37	D38	D39	D40	D41
0	0	1	0	0	0

Zero cross detection mode setting

Volume block setting

Zero Cross Timer Setting

When the level of the input signal is lower than the zero cross detector sensitivity setting, or when the input signal is a low-frequency signal, the system will remain in a state where it cannot detect a zero cross event for an extended period, and the IC will not be able to latch data during that period. The zero cross timer sets a period for forcibly latching the data when the IC is in a state such as this where a zero cross cannot be detected.

For example, to set a time of 25 ms:

$T = 0.69 \times C \times R$

If C = 0.033 μF, then:

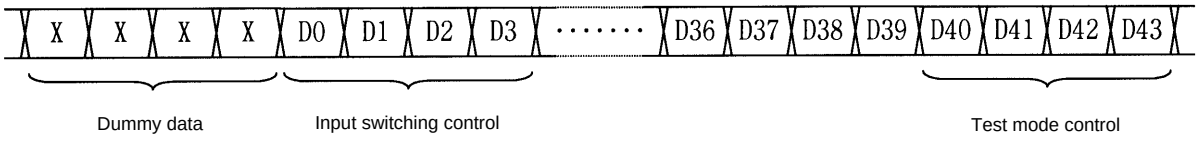
$$R = \frac{25 \times 10^{-3}}{0.69 \times 0.033 \times 10^{-6}} \approx 1.1\ M\Omega$$

This time is normally set to be in the range 10 to 50 ms.

Notes on Serial Data Transfer

- The CL, DI, and CE pin signal lines must be covered by the ground pattern, or shielded cables must be used for these lines, to prevent high-frequency noise from these signals from entering the audio signal.
- The LC75386NE data format consists of 8 bits of address and 44 bits of data. Use the data transfer format shown in the figure below when transmitting data in multiples of 8 bits (i.e. when sending 48 bits of data).

Data Transfer to the LC75386NE in 8-Bit Units



X : don't care