

# LC74900PT-8B15H

## LCD Processor LSI for Small Size Display

### Overview

LC74900 is a highly integrated multi-purpose LCD panel (up to WVGA) controller processing analog and digital video signal.

It contains A/D converter, video decoder, De-interlacer/Scaler, and picture improvement.

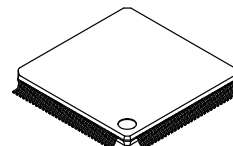
### Features

- Video Input/Output
  - ◆ Analog Input: 4ch CVBS (NTSC, PAL, and SECAM) with 1ch 10 bit A/D converter
  - ◆ Digital Input: 24 bit RGB and YCbCr, 16bit YCbCr (4:2:2), and 8 bit YC (BT.656)
  - ◆ Digital Output: 8 bit Video Decoder Output (BT.656)
- Video Decoder
  - ◆ Adaptive 3line Comb Filter, Automatic Gain and Chrominance Control
- De-interlacer and Scaler
  - ◆ Horizontal and Vertical Programmable Scaler Separately, and Supports Panels up to WVGA Resolutions
- Picture Improvements
  - ◆ CDEX (Color Depth Expander): High Quality Expansion for Low-resolution Graphics
  - ◆ Dynamic Gamma Correction: Picture Adapted Automatic Luminance Control
  - ◆ Sharpness Control, LTI and CTI: Peaking Enhancement without Glares
  - ◆ Color Exciter: 6 Phases RGBYMC Gain Control Separately
- Panel Interface
  - ◆ 24 bit RGB Output and 18 bit RGB Output with Dithering Process
  - ◆ Pulse Width Modulation for Automatic LED Backlight Control
  - ◆ Timing Controller for LCD Driver with Horizontal or Vertical Reversing Signals
  - ◆ Pin Swapping: Replace Output Pin Assignment of the RGB Channel or Bit
- On Screen Display
  - ◆ Built-in OSD Controller with Integrated Font ROM, which Contains 501 Fonts, and Font RAM, which contains 8 Fonts
  - ◆ Character Numbers Displayed on the Screen: 24 Characters by 8 Rows, 24 Characters by 10 Rows, or 32 Characters by 8 Rows
  - ◆ Character Size: 16 Pixels Wide by 20 Pixels High
  - ◆ Character Colors: 8 Font Colors for each Character, 8 Back Colors for each Character, and 8 Font Border Colors for each Row
  - ◆ Inverting Font Colors and Back Colors each Character, Blinking Fonts each Character, and Fringing each Row
  - ◆ Pin Assignment for an Optional External OSD Controller: 24 bit, 18 bit, 12 bit, and 6 bit RGB



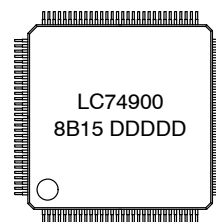
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TQFP120 14x14  
CASE 932AZ

### MARKING DIAGRAM



DDDDD = Lot No

### ORDERING INFORMATION

Device	Package	Shipping
LC74900PT-8B15H	TQFP120 (Pb-Free)	450 Units / JTRAY

# LC74900PT-8B15H

- EEPROM Booting
  - ◆ Quick Boot from an External EEPROM in Power on Sequence before Starting a System Controller
  - ◆ Waiting Timer between Data Transfers
  - ◆ Verifying Boot Data
  - ◆ EEPROM Size: Up to 512K bits with I<sup>2</sup>C or SPI Interface
- Parallel Data Outputs, Panel Interface and Video Decoder Output
  - ◆ Reentering Video Decoder Outputs, which are Processed by an External Graphic Engine as Digital Inputs
- System Controller Interface
  - ◆ SPI (Max 1 Mbit/s) or I<sup>2</sup>C bus (100 kbit/s or 400 kbit/s)

## LSI Specification

- Supply Voltage: 1.5 V (Core), 3.3 V (IO)
- Maximum Operation Frequency: 60 MHz (Video Processing)
- Package: 120 pin TQFP

## Applications

- For Medium or Small Size LCD Panel
- Automobile Use: Car TV, Portable Navigation, etc.
- Home Use: Photo Frame, Portable DVD, Door Phone, etc.

This specification could be modified because of improvement.

## BLOCK DIAGRAM

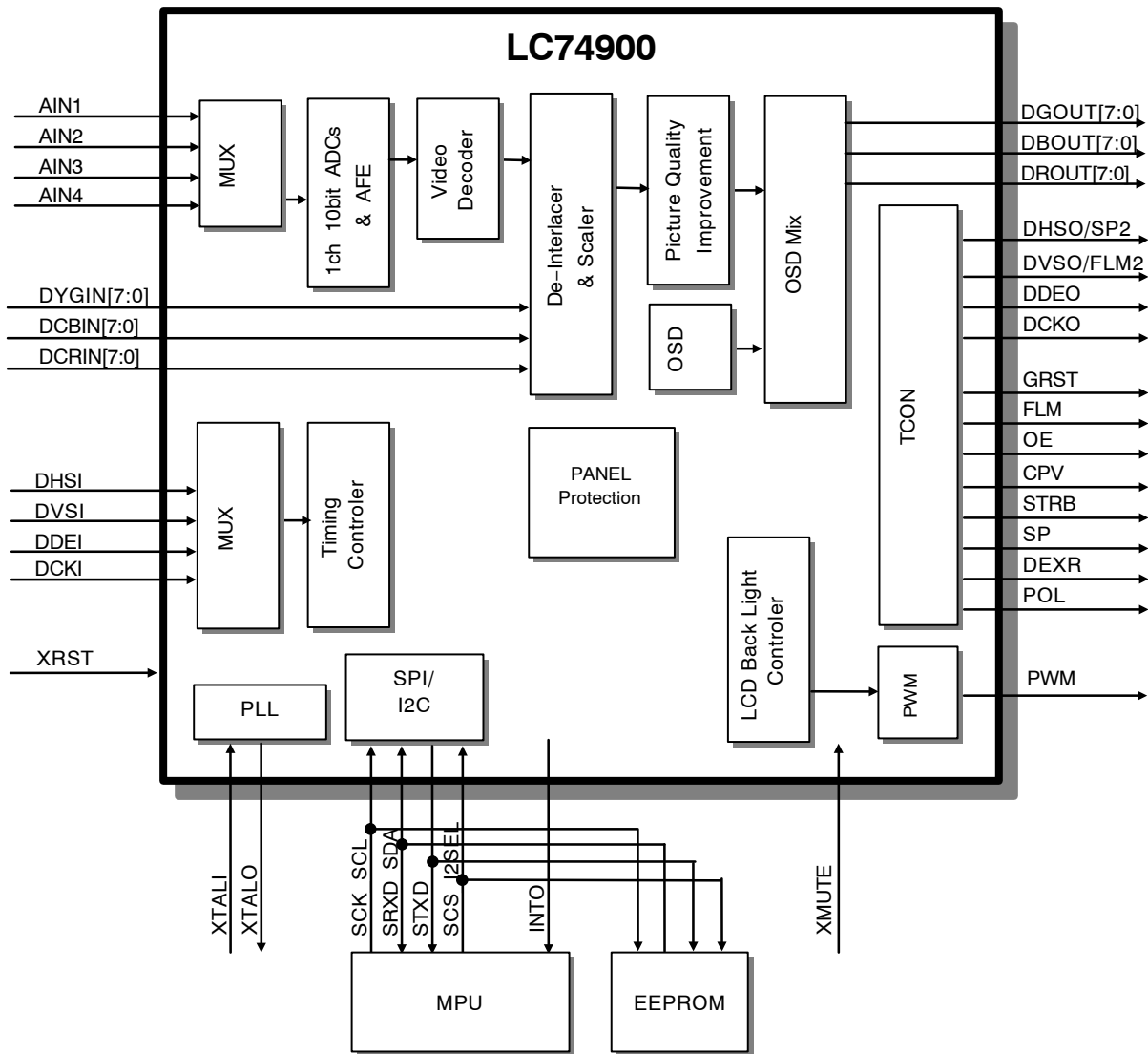


Figure 1. Block Diagram

# LC749000PT-8B15H

## SPECIFICATIONS

**Table 1. ABSOLUTE MAXIMUM RATINGS**

( $T_a = 25^\circ\text{C}$ ,  $DV_{SS} = 0\text{ V}$ ,  $ADC0AV_{SS} = 0\text{ V}$ ,  $ADC1AV_{SS} = 0\text{ V}$ ,  $PLLAV_{SS} = 0\text{ V}$ ,  $XV_{SS} = 0\text{ V}$ )

Symbol	Parameter	Ratings	Unit
$DV_{DD33}$ $XV_{DD33}$ $DV_{DD3318}$	Maximum Supply Voltage (I/O)	-0.3 to + 3.96	V
$ADC0AV_{DD33}$ $ADC1AV_{DD33}$ $PLLAV_{DD33}$	Maximum Supply Voltage (Analog)	-0.3 to + 3.96	V
$DV_{DD15}$	Maximum Supply Voltage (Core)	-0.3 to + 1.8	V
$V_I$	Digital Input Voltage	-0.3 to $DV_{DD33} + 0.3$	V
		-0.3 to $DV_{DD3318} + 0.3$	
$V_I$ (5V Tolerant)		-0.3 to + 5.6	
$V_O$	Digital Output Voltage	-0.3 to $DV_{DD33} + 0.3$	V
		-0.3 to $DV_{DD3318} + 0.3$	
$T_{opr}$	Operating Temperature	-40 to + 85	$^\circ\text{C}$
$T_{stg}$	Storage Temperature	-55 to + 125	$^\circ\text{C}$
$P_d \text{ max}$	Maximum Allowable Loss	0.7 ( $T_a = 85^\circ\text{C}$ , with Evaluation Board*) *Board Size: 150 mm $\times$ 50 mm $\times$ 1.6 mm, FR-4, 6 layers	W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 2. ALLOWABLE OPERATION RANGES**

( $T_a = -40^\circ\text{C}$  to + 85 $^\circ\text{C}$ ,  $DV_{SS} = 0\text{ V}$ ,  $ADC0AV_{SS} = 0\text{ V}$ ,  $ADC1AV_{SS} = 0\text{ V}$ ,  $PLLAV_{SS} = 0\text{ V}$ ,  $XV_{SS} = 0\text{ V}$ )

Symbol	Parameter	Min	Typ	Max	Unit
$DV_{DD33}$ $XV_{DD33}$	Supply Voltage (I/O)	3.15	3.3	3.45	V
$DV_{DD3318}$		3.15	3.3	3.45	V
		1.7	1.8	1.9	V
$ADC0AV_{DD33}$ $ADC1AV_{DD33}$ $PLLAV_{DD33}$	Supply Voltage (Analog)	3.15	3.3	3.45	V
$DV_{DD15}$	Supply Voltage (Core)	1.4	1.5	1.6	V
$V_{IN}$	Input Voltage Range	0	-	$DV_{DD33}$ $DV_{DD3318}$	V
$V_{IN5}$	Input Voltage Range (5 V Tolerant)	0	-	5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# LC749000PT-8B15H

**Table 3. DC CHARACTERISTICS**

( $T_a = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $DV_{SS} = 0\text{ V}$ ,  $ADC0AV_{SS} = 0\text{ V}$ ,  $ADC1AV_{SS} = 0\text{ V}$ ,  $PLLAV_{SS} = 0\text{ V}$ ,  $XV_{SS} = 0\text{ V}$ ,  $DV_{DD33} = 3.15\text{ V}$  to  $3.45\text{ V}$ ,  $DV_{DD3318} = 3.15\text{ V}$  to  $3.45\text{ V}$  or  $1.7\text{ V}$  to  $1.9\text{ V}$ ,  $DV_{DD15} = 1.42\text{ V}$  to  $1.58\text{ V}$ ,  $XV_{DD33} = 3.15\text{ V}$  to  $3.45\text{ V}$ ,  $ADC0AV_{DD} = 3.15\text{ V}$  to  $3.45\text{ V}$ ,  $ADC1AV_{DD} = 3.15\text{ V}$  to  $3.45\text{ V}$ ,  $PLLAV_{DD} = 3.15\text{ V}$  to  $3.45\text{ V}$ )

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	Input High-level Voltage	CMOS level inputs	$0.7 DV_{DD33}$ $0.7 DV_{DD3318}$	–		V
		CMOS level Schmitt inputs	$0.7 DV_{DD33}$	–		V
$V_{IL}$	Input Low-level Voltage	CMOS level inputs		–	$0.3 DV_{DD33}$ $0.3 DV_{DD3318}$	V
		CMOS level Schmitt inputs		–	$0.3 DV_{DD33}$	V
$I_{IH}$	Input High-level Current	$V_I = DV_{DD33}$	–	–	–	$\mu\text{A}$
		$V_I = DV_{DD3318}$	–	–	–	$\mu\text{A}$
$I_{IL}$	Input Low-level Current	$V_I = DV_{SS}$	–	–	–	$\mu\text{A}$
$V_{OH}$	Output High-level Voltage	Type B: $I_{OH} = -4\text{ mA}$ Type G: $I_{OH} = -6\text{ mA}$	$DV_{DD33} - 0.6$	–	–	V
		$DV_{DD3318} = 3.15\text{ V}$ to $3.45\text{ V}$ Type J: $I_{OH} = -4\text{ mA}$ Type K: $I_{OH} = -6\text{ mA}$	$DV_{DD3318} - 0.6$	–	–	V
		$DV_{DD3318} = 1.7\text{ V}$ to $1.9\text{ V}$ Type J: $I_{OH} = -3\text{ mA}$ Type K: $I_{OH} = -5\text{ mA}$	$DV_{DD3318} - 0.4$	–	–	V
$V_{OL}$	Output Low-level Voltage	CMOS	–	–	0.4	V
$I_{OZ}$	Output Leakage Current	When in high-impedance output mode	–10		10	$\mu\text{A}$
$I_{DDOP}$	Operating Current Drain	Output open, tck = 9 MHz, 10 steps $T_a = 25^\circ\text{C}$ $DV_{DD33} = 3.3\text{ V}$ $DV_{DD3318} = 3.3\text{ V}$ $XV_{DD} = 3.3\text{ V}$ $DV_{DD15} = 1.5\text{ V}$ $ADC0AV_{DD} = 3.3\text{ V}$ $ADC1AV_{DD} = 3.3\text{ V}$ $PLLAV_{DD} = 3.3\text{ V}$		95		$\text{mA}$
		Output open, tck = 33 MHz, 10 steps $T_a = 25^\circ\text{C}$ $DV_{DD33} = 3.3\text{ V}$ $DV_{DD3318} = 3.3\text{ V}$ $XV_{DD} = 3.3\text{ V}$ $DV_{DD15} = 1.5\text{ V}$ $ADC0AV_{DD} = 3.3\text{ V}$ $ADC1AV_{DD} = 3.3\text{ V}$ $PLLAV_{DD} = 3.3\text{ V}$		139		$\text{mA}$
$I_{DDST}$	Static Current Drain	Output open, tck: Stop $V_I = DV_{SS}$ $T_a = 25^\circ\text{C}$ $DV_{DD33} = 3.3\text{ V}$ $DV_{DD3318} = 1.8\text{ V}$ $XV_{DD} = 3.3\text{ V}$ $DV_{DD15} = 1.5\text{ V}$ $ADC0AV_{DD} = 3.3\text{ V}$ $ADC1AV_{DD} = 3.3\text{ V}$ $PLLAV_{DD} = 3.3\text{ V}$		34		$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# LC74900PT-8B15H

## PIN ASSIGNMENT

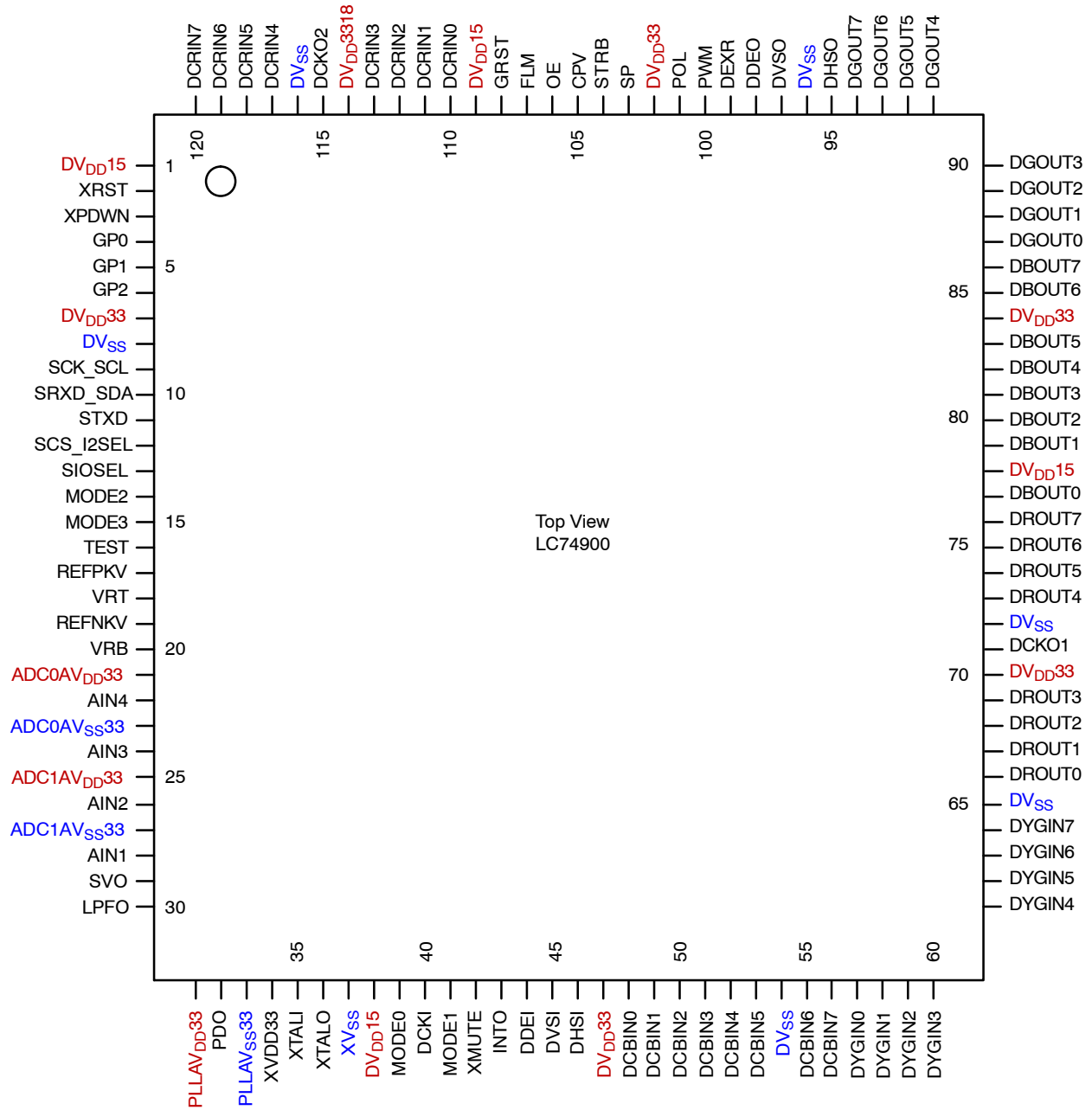


Figure 2. Pin Assignment

# LC749000PT-8B15H

**Table 4. PIN FUNCTIONS**

Pin No.	Pin Symbol	Pin Type		Signal Source		Digital Pins Supply Source	Description
		I/O	Type	Device Type	Digital or Analog		
1	DV <sub>DD</sub> 15	P	-	V <sub>DD</sub> (Core)	Digital		Power Supply for Core (1.5 V)
2	XRST	I	A	CMOS	Digital	DV <sub>DD</sub> 33	Reset pin (active at a low voltage level)
3	XPDOWN	I	A	CMOS	Digital	DV <sub>DD</sub> 33	Fixed at a high voltage level
4	GP0	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Input: Digital input/OSD enable (pull down if not used) Output: Global port/Video Decoder Vsync
5	GP1	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Input: Digital input/OSD half-tone (pull down if not used) Output: Global Port/Video Decoder Hsync
6	GP2	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Global Port Output
7	DV <sub>DD</sub> 33	P	-	V <sub>DD</sub> (IO)	Digital		Power Supply for IO (3.3 V)
8	DV <sub>SS</sub>	P	-	GND	Digital		GND for digital
9	SCK_SCL	I/O	C	CMOS	Digital	DV <sub>DD</sub> 33	I <sup>2</sup> C: I <sup>2</sup> C Clock Inout, SPI: Clock Input
10	SRXD_SDA	I/O	C	CMOS	Digital	DV <sub>DD</sub> 33	I <sup>2</sup> C: data Inout, SPI: data Input
11	STXD	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	SPI: data Output
12	SCS_I2SEL	I	A	CMOS	Digital	DV <sub>DD</sub> 33	I <sup>2</sup> C: Select I <sup>2</sup> C Slave Address, SPI: Chip Select
13	SIOSEL	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Select CPU I/F, "L": I <sup>2</sup> C, "H": SPI
14	MODE2	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Operation Mode control
15	MODE3	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Operation Mode control
16	TEST	I	D	CMOS	Digital	DV <sub>DD</sub> 33	For Production Test (Fixed at a low voltage level)
17	REFPKV	I	E		Analog		Top Reference level Buffer-AMP input for ADC
18	VRT	I	E		Analog		Top Reference level for ADC
19	REFNKV	I	E		Analog		Bottom Reference level Buffer-AMP input for ADC
20	VRB	I	E		Analog		Bottom Reference level for ADC
21	ADC0AV <sub>DD</sub> 33	P	-	V <sub>DD</sub> (Analog)	Analog		Power Supply for ADC (3.3 V)
22	AIN4	I	E		Analog		CVBS Input 4
23	ADC0AV <sub>SS</sub> 33	P	-	GND	Analog		GND for ADC
24	AIN3	I	E		Analog		CVBS Input 3
25	ADC1AV <sub>DD</sub> 33	P	-	V <sub>DD</sub> (Analog)	Analog		Power Supply for ADC (3.3 V)
26	AIN2	I	E		Analog		CVBS Input 2
27	ADC1AV <sub>SS</sub> 33	P	-	GND	Analog		GND for ADC
28	AIN1	I	E		Analog		CVBS Input 1
29	SVO	O	E		Analog		AFE Output
30	LPFO	O	E		Analog		External AGC Control Level
31	PLLAV <sub>DD</sub> 33	P	-	V <sub>DD</sub> (Analog)	Analog		Power Supply for PLL (3.3 V)
32	PDO	O	-		Analog		Test port for PLL (Open)
33	PLLAV <sub>SS</sub> 33	P	-	GND	Analog		GND for PLL
34	XV <sub>DD</sub> 33	P	-	V <sub>DD</sub> (IO)	Digital		Power Supply for 27 MHz X'tal (3.3 V)
35	XTALI	I	F	CMOS	Digital	XV <sub>DD</sub> 33	27 MHz X'tal Input
36	XTALO	O	F	CMOS	Digital	XV <sub>DD</sub> 33	27 MHz X'tal Output
37	XV <sub>SS</sub>	P	-	GND	Digital		GND for 27 MHz X'tal
38	DV <sub>DD</sub> 15	P	-	V <sub>DD</sub> (Core)	Digital		Power Supply for Core (1.5 V)
39	MODE0	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Operation Mode Control
40	DCKI	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video Clock
41	MODE1	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Operation Mode Control
42	XMUTE	I	A	CMOS	Digital	DV <sub>DD</sub> 33	Mute Control (active at a low voltage level)
43	INTO	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Interrupt Output
44	DDEI	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video Enable/OSD Enable
45	DVSI	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video Vsync/OSD Half Tone

# LC749000PT-8B15H

**Table 4. PIN FUNCTIONS** (continued)

Pin No.	Pin Symbol	Pin Type		Signal Source		Digital Pins Supply Source	Description
		I/O	Type	Device Type	Digital or Analog		
46	DHSI	I	D	CMOS	digital	DV <sub>DD</sub> 33	Digital Video Hsync
47	DV <sub>DD</sub> 33	P	-	V <sub>DD</sub> (IO)	digital		Power Supply for IO (3.3 V)
48	DCBIN0	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
49	DCBIN1	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
50	DCBIN2	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
51	DCBIN3	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
52	DCBIN4	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
53	DCBIN5	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
54	DV <sub>SS</sub>	P		GND	Digital		GND for digital
55	DCBIN6	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
56	DCBIN7	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
57	DYGIN0	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
58	DYGIN1	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
59	DYGIN2	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
60	DYGIN3	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD Input (pull down if not used)
61	DYGIN4	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD input (pull down if not used)
62	DYGIN5	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD input (pull down if not used)
63	DYGIN6	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD input (pull down if not used)
64	DYGIN7	I	D	CMOS	Digital	DV <sub>DD</sub> 33	Digital Video input/OSD input (pull down if not used)
65	DV <sub>SS</sub>	P		GND	Digital		GND for digital
66	DROUT0	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel R output (LSB) (input port in test mode)
67	DROUT1	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel R output (input port in test mode)
68	DROUT2	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel R output (input port in test mode)
69	DROUT3	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel R output (input port in test mode)
70	DV <sub>DD</sub> 33	P		V <sub>DD</sub> (IO)	Digital		Power Supply for IO (3.3 V)
71	DCKO1	O	G	CMOS	Digital	DV <sub>DD</sub> 33	Panel Clock output
72	DV <sub>SS</sub>	P		GND	Digital		GND for digital
73	DROUT4	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel R output (input port in test mode)
74	DROUT5	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel R output (input port in test mode)
75	DROUT6	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel R output (input port in test mode)
76	DROUT7	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel R output (MSB) (input port in test mode)
77	DBOUT0	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel B output (LSB) (input port in test mode)
78	DV <sub>DD</sub> 15	P		V <sub>DD</sub> (Core)	Digital		Power Supply for core (1.5 V)
79	DBOUT1	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel B output (input port in test mode)
80	DBOUT2	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel B output (input port in test mode)
81	DBOUT3	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel B output (input port in test mode)
82	DBOUT4	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel B output (input port in test mode)
83	DBOUT5	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel B output (input port in test mode)
84	DV <sub>DD</sub> 33	P		V <sub>DD</sub> (IO)	Digital		Power Supply for IO (3.3 V)
85	DBOUT6	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel B output (input port in test mode)
86	DBOUT7	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel B output (MSB) (input port in test mode)
87	DGOUT0	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel G output (LSB) (input port in test mode)
88	DGOUT1	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel G output (input port in test mode)
89	DGOUT2	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel G output (input port in test mode)
90	DGOUT3	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel G output (input port in test mode)
91	DGOUT4	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel G output (input port in test mode)

# LC749000PT-8B15H

**Table 4. PIN FUNCTIONS** (continued)

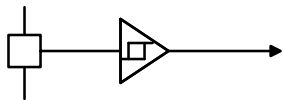
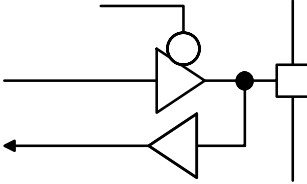
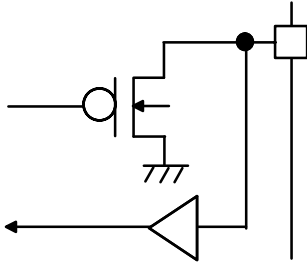
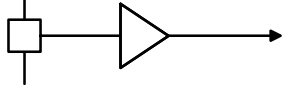
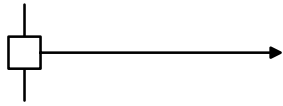
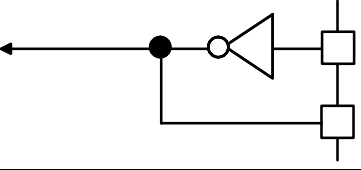
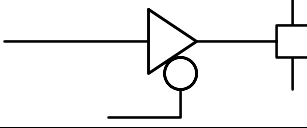
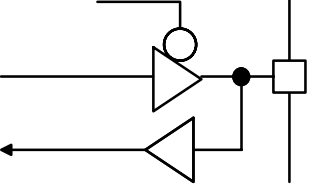
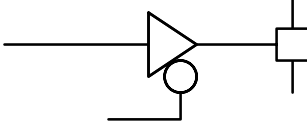
Pin No.	Pin Symbol	Pin Type		Signal Source		Digital Pins Supply Source	Description
		I/O	Type	Device Type	Digital or Analog		
92	DGOUT5	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel G output (input port in test mode)
93	DGOUT6	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel G output (input port in test mode)
94	DGOUT7	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel G output (MSB) (input port in test mode)
95	DHSO	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel Hsync/Start Pulse for source driver/ Video Decoder Hsync output (input port in test mode)
96	DV <sub>SS</sub>	P		GND	Digital		GND for digital
97	DVSO	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel Vsync/Start Pulse for gate driver/ Video Decoder Vsync output (input port in test mode)
98	DDEO	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Panel Enable output (input port in test mode)
99	DEXR	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Invert control signal for DTR/ Video Decoder output 1[7] (BT.656) (input port in test mode)
100	PWM	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Pulse Width Modulation (input port in test mode)
101	POL	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Polarity control for source driver/ Video Decoder output 1[6] (BT.656) (input port in test mode)
102	DV <sub>DD</sub> 33	P		V <sub>DD</sub> (IO)	Digital		Power Supply for IO (3.3 V)
103	SP	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Start pulse for source driver/ Video Decoder output 1[5] (BT.656) (input port in test mode)
104	STRB	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Data Stroboscope for source driver/ Video Decoder output 1[4] (BT.656) (input port in test mode)
105	CPV	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Clock for gate driver/ Video Decoder output 1[3] (BT.656) (input port in test mode)
106	OE	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Output enable for gate driver/ Video Decoder output 1[2] (BT.656) (input port in test mode)
107	FLM	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Start pulse for gate driver/ Video Decoder output 1[1] (BT.656) (input port in test mode)
108	GRST	I/O	B	CMOS	Digital	DV <sub>DD</sub> 33	Reset for gate driver/ Video Decoder output1[0] (BT.656) (input port in test mode)
109	DV <sub>DD</sub> 15	P		V <sub>DD</sub> (Core)	Digital		Power Supply for core (1.5 V)
110	DCRIN0	I/O	H	CMOS	Digital	DV <sub>DD</sub> 3318	Input: Digital Video input/OSD input (pull down if not used) Output: Video Decoder output 2[0] (BT.656)
111	DCRIN1	I/O	H	CMOS	Digital	DV <sub>DD</sub> 3318	Input: Digital Video input/OSD input (pull down if not used) Output: Video Decoder output 2[1] (BT.656)
112	DCRIN2	I/O	H	CMOS	Digital	DV <sub>DD</sub> 3318	Input: Digital Video input/OSD input (pull down if not used) Output: Video Decoder output 2[2] (BT.656)
113	DCRIN3	I/O	H	CMOS	Digital	DV <sub>DD</sub> 3318	Input: Digital Video input/OSD input (pull down if not used) Output: Video Decoder output 2[3] (BT.656)
114	DV <sub>DD</sub> 3318	P	-	V <sub>DD</sub> (IO)	Digital		Power Supply for IO (3.3 V/1.8 V)
115	DCKO2	O	J	CMOS	Digital	DV <sub>DD</sub> 3318	Video Decoder Clock output
116	DV <sub>SS</sub>	P	-	GND	Digital		GND for digital
117	DCRIN4	I/O	H	CMOS	Digital	DV <sub>DD</sub> 3318	Input: Digital Video input/OSD input (pull down if not used) Output: Video Decoder output 2[4] (BT.656)
118	DCRIN5	I/O	H	CMOS	Digital	DV <sub>DD</sub> 3318	Input: Digital Video input/OSD input (pull down if not used) Output: Video Decoder output 2[5] (BT.656)
119	DCRIN6	I/O	H	CMOS	Digital	DV <sub>DD</sub> 3318	Input: Digital Video input/OSD input (pull down if not used) Output: Video Decoder output 2[6] (BT.656)
120	DCRIN7	I/O	H	CMOS	Digital	DV <sub>DD</sub> 3318	Input: Digital Video input/OSD input (pull down if not used) Output: Video Decoder output 2[7] (BT.656)



# LC749000PT-8B15H

## Pin Type

**Table 5. PIN TYPE**

I/O Type	Function	Equivalent Circuit	Applicable Pins
A	Schmitt Trigger CMOS Input		XRST, XPDWN, SCS_I2SEL, XMUTE
B	8 mA 3-STATE Drive CMOS I/O		GP0, GP1, GP2, STXD, INTO, DROUT0, DROUT1, DROUT2, DROUT3, DROUT4, DROUT5, DROUT6, DROUT7, DBOUT0, DBOUT1, DBOUT2, DBOUT3, DBOUT4, DBOUT5, DBOUT6, DBOUT7, DGOUT0, DGOUT1, DGOUT2, DGOUT3, DGOUT4, DGOUT5, DGOUT6, DGOUT7 DVSO, DHSO, DDEO, DEXR, PWM, POL, SP, STRB, CPV, OE, FLM, GRST
C	8 mA OpenDrain Output CMOS Input (Note 1)		SCK_SCL, SRXD_SDA
D	CMOS Input		SIOSEL, MODE2, MODE3, TEST, MODE0, DCKI, MODE1, DDEI, DVSI, DHSI, DCBIN0, DCBIN1, DCBIN2, DCBIN3, DCBIN4, DCBIN5, DCBIN6, DCBIN7, DYGIN0, DYGIN1, DYGIN2, DYGIN3, DYGIN4, DYGIN5, DYGIN6, DYGIN7
E	Analog I/O		REFPKV, VRT, REFNKV, VRB, AIN4, AIN3, AIN2, AIN1, SVO, LPFO
F	Oscillator Circuit I/O		XTALI, XTALO
G	12 mA 3-STATE Drive CMOS Output		DCKO1
H	3-STATE Drive CMOS I/O 3.3 V: 8 mA 1.8 V: 3 mA		DCRIN0, DCRIN1, DCRIN2, DCRIN3, DCRIN4, DCRIN5, DCRIN6, DCRIN7
J	3-STATE Drive CMOS Output 3.3 V: 12 mA 1.8 V: 5 mA		DCKO2

1. 5 V Tolerant.

# LC749000PT-8B15H

## I/O DATA TIMING

### Input Data Timing

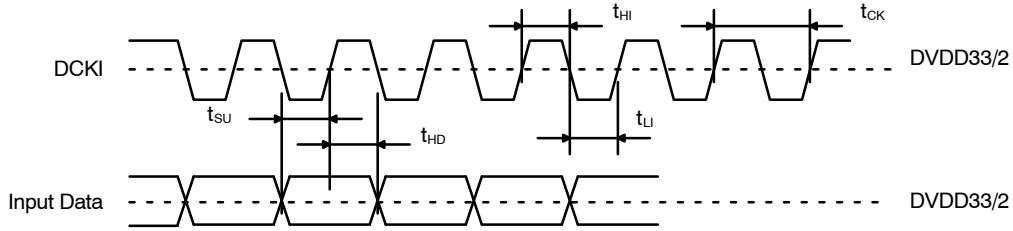


Figure 3.

Table 6.

Pin Name	Parameter	Symbol	Min	Typ	Max	Unit
DCKI	Clock Cycle	$t_{CK}$	16.7	-	-	ns
	Duty		-	50	-	%
DCRIN*, DYGIN*, DCBIN*, DVSI, DHSI, DDEI	Input Data Setup Time ( $DV_{DD33} = 3.15\text{ V to }3.45\text{ V}$ ) ( $DV_{DD3318} = 3.15\text{ V to }3.45\text{ V}$ )	$t_{SU}$	6.5	-	-	ns
	Input Data Hold Time ( $DV_{DD33} = 3.15\text{ V to }3.45\text{ V}$ ) ( $DV_{DD3318} = 3.15\text{ V to }3.45\text{ V}$ )	$t_{HD}$	-0.5	-	-	ns

\*The recommended duty ratio of input clock is 50%.

### Output Data Timing

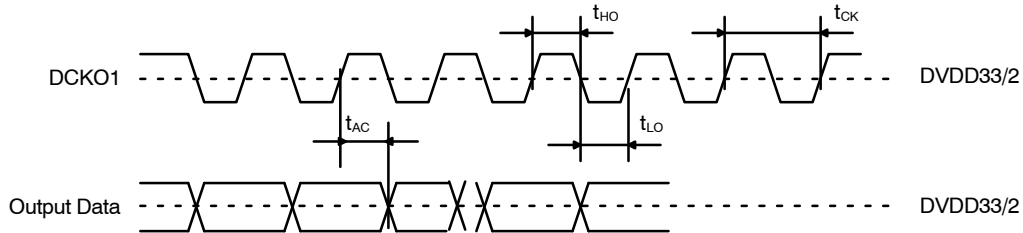


Figure 4.

Table 7.

Pin Name	Parameter	Symbol	Min	Typ	Max	Unit
DCKO1	Clock Cycle	$t_{CK}$	16.7	-	-	ns
	Duty		-	50	-	%
DROUT*, DGOUT*, DBOUT*, DVSO, DHSO, DDEO, DEXR, POL, SP, STRB, CPV, OE, FLM, GRST	Output Data Delay Time $DV_{DD33} = 3.15\text{ V to }3.45\text{ V}$	$t_{AC}$	-3	-	3	ns

\*DCKO1 output is not inverted. Output capacitance: 15 pF

# LC749000PT-8B15H

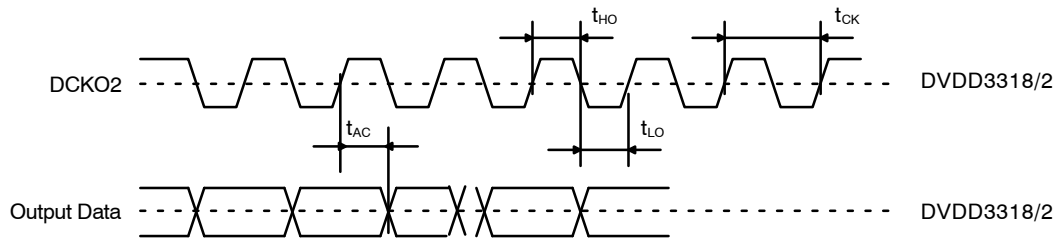


Figure 5.

Table 8.

Pin Name	Parameter	Symbol	Min	Typ	Max	Unit
DCKO2	Clock Cycle	$t_{CK}$	37		-	ns
	Duty			50		%
DCRIN*, DEXR, POL, SP, STRB, CPV, OE, FLM, GRST, GP0, GP1, DVSO, DHSO	Output Data Delay Time $DV_{DD3318} = 3.15\text{ V to }3.45\text{ V}$ $DV_{DD33} = 3.15\text{ V to }3.45\text{ V}$	$t_{AC}$	-3		3	ns
DCRIN*	Output Data Delay Time $DV_{DD3318} = 1.7\text{ V to }1.9\text{ V}$	$t_{AC}$	-6		6	ns

\*DCKO1 output is not inverted. Output capacitance: 15 pF

# LC749000PT-8B15H

## CONNECTION EXAMPLE OF PARALLEL OUTPUT MODE (PANEL/VIDEO DECODER)

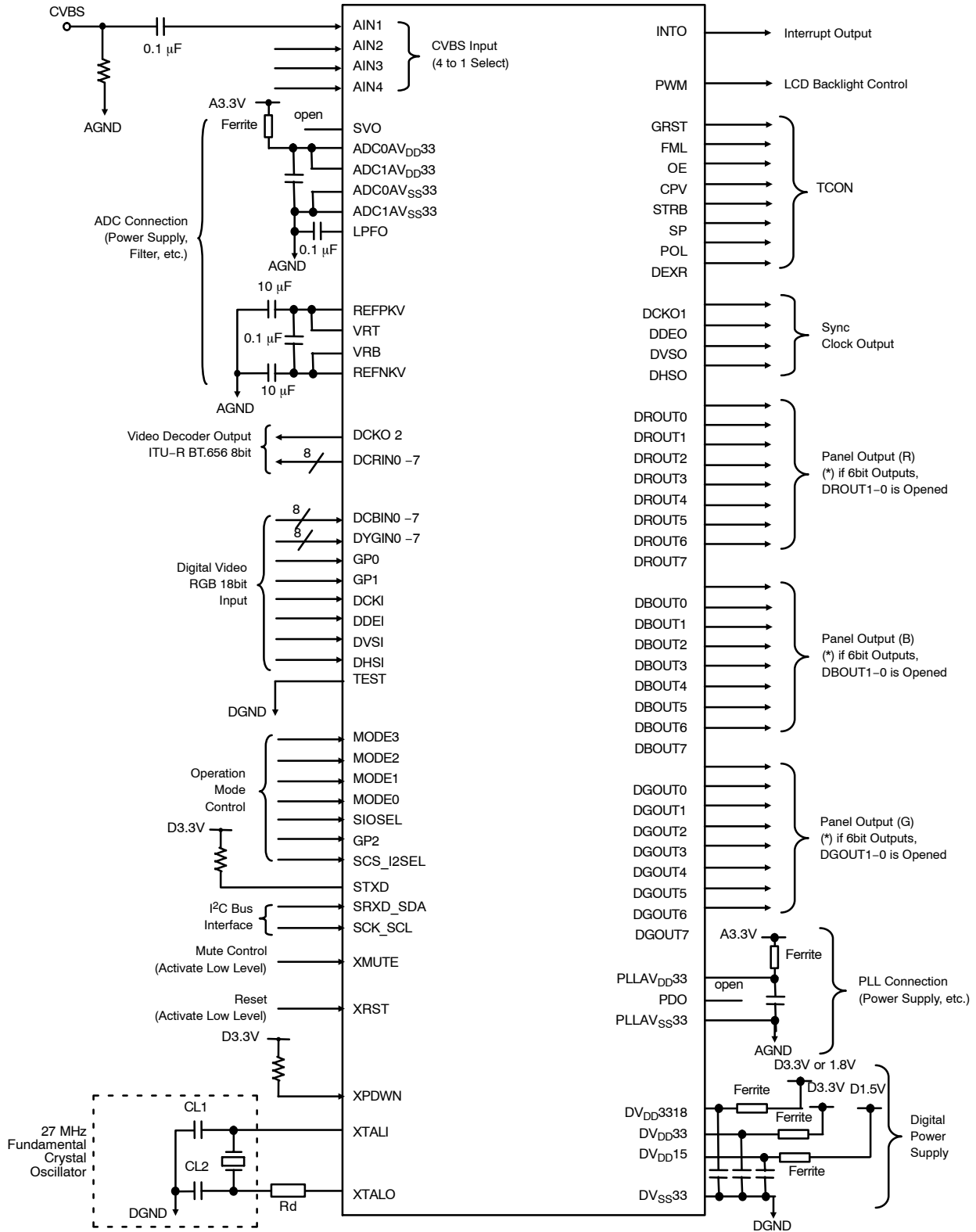
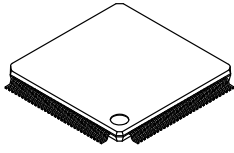


Figure 6. Connection Example of Parallel Output Mode

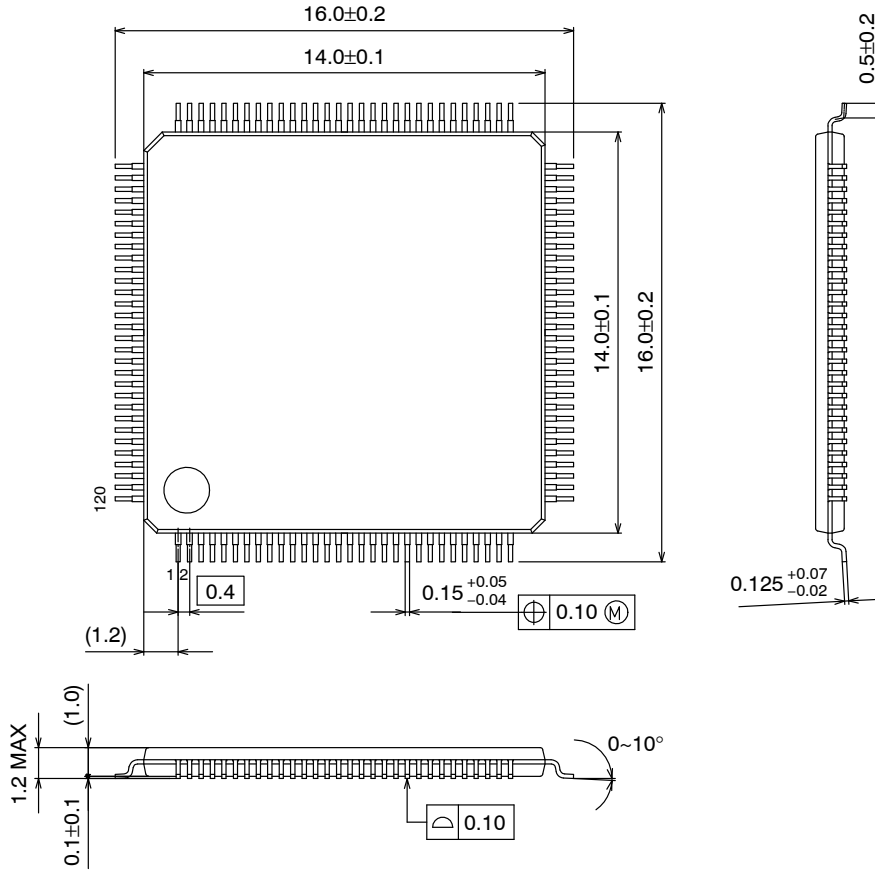
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**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

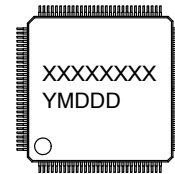


**TQFP120 14x14 / TQFP120**  
**CASE 932AZ**  
**ISSUE A**

DATE 07 NOV 2013



**GENERIC MARKING DIAGRAM\***

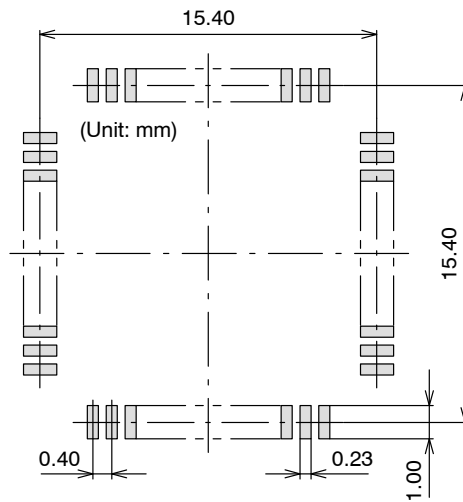


XXXXXX = Specific Device Code  
 Y = Year  
 M = Month  
 DDD = Additional Traceability Data

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

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**SOLDERING FOOTPRINT\***



NOTE: The measurements are not to guarantee but for reference only.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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