Ordering number : EN5213A

CMOS LSI

LC74725, 74725M

On-Screen Display Controller LSI

Overview

The LC74725 and LC74725M are built-in EDS on-screen display controller CMOS LSI products that display characters and patterns on a TV screen under microprocessor control. The characters displayed have an 8 × 8 dot format, and a dot interpolation function is provided. These LSIs can display ten lines of 24 characters each.

Features

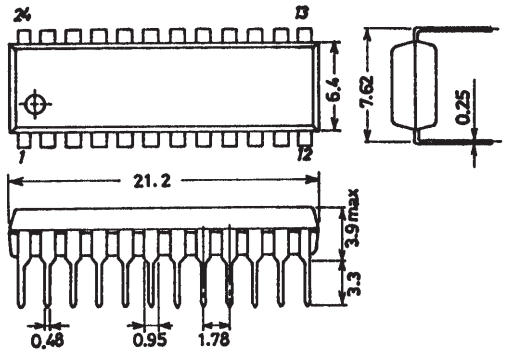
- Display format: 24 characters by 10 lines (up to 240 characters)
- Character format: 8 (horizontal) × 8 (vertical) dots (interpolation function provided)
- Character sizes: Two horizontal and two vertical sizes
- Characters in font: 64 characters
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Blinking: Specifiable on a per-character basis
- Blinking types: Two periods, 1.0 second and 0.5 second
- Blue background screen display: Available in internal synchronization mode
- External control input: 8-bit serial input format
- Built-in sync separator circuit
- EDS support
- Video outputs: Composite video signal output in either NTSC or PAL-M
- Package: 24-pin plastic DIP (300 mil)
  24-pin plastic MFP (375 mil)

Package Dimensions

unit: mm

3067-DIP24S

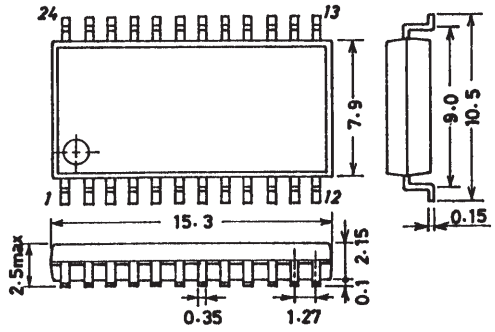
[LC7425]



SANYO: DIP24S

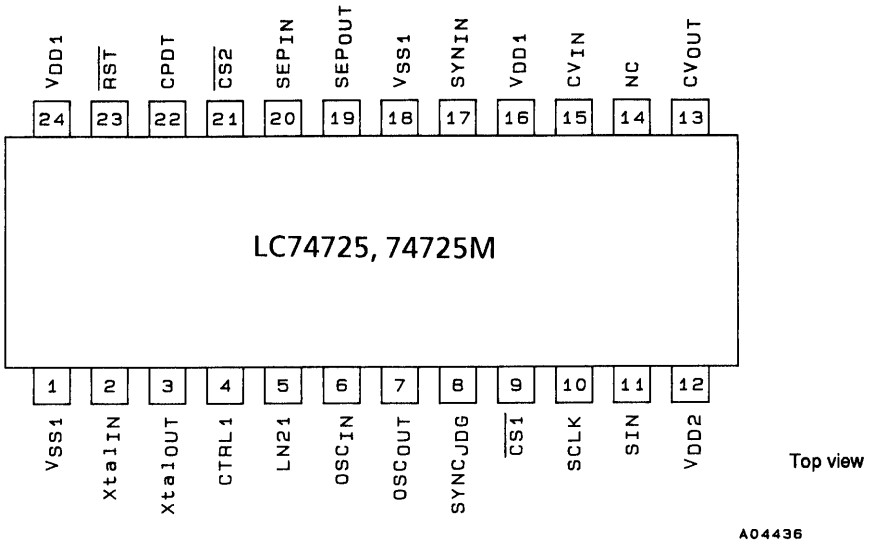
3045B-MFP24

[LC7425M]



SANYO: MFP24

Pin Assignment



Pin Functions

Pin No.	Symbol	Function	Description
1	$V_{SS}1$	Ground	Ground connection (digital system ground)
2	$Xtal_{IN}$	Crystal oscillator	Connections for the external crystal and capacitors used to form a crystal oscillator for internal synchronizing signal generation. Alternatively, these pins can be used for external clock input (2fsc or 4fsc).
3	$Xtal_{OUT}$		
4	CTRL1	Crystal oscillator input switching	Switches between external clock input mode and crystal oscillator mode. Low: crystal oscillator mode, high: external clock input mode.
5	LN21	Data output	Line 21H pulse output (MOD0 = low: even field, MOD0 = high: both fields output)
6	OSC_{IN}	LC oscillator	Connections for the external coil and capacitor used to form the character output dot clock generation oscillator.
7	OSC_{OUT}		
8	$SYNC_{JDG}$	External synchronizing signal judgment output	Outputs the judgment as to where there are or are not external synchronizing signals present. Outputs a high level when there are synchronizing signals. SEL0 = high: Outputs field discrimination pulses (O/E pulses) Outputs the dot clock (LC oscillator) when the $\overline{CS1}$ pin is high and the $\overline{RST}$ pin is low. A command is provided that turns this output off. Outputs the crystal oscillator clock when the $\overline{CS1}$ pin is low and the $\overline{RST}$ pin is low. A command is provided that turns this output off.
9	$\overline{CS1}$	Enable input	Enable input for OSD serial data input. Serial data input is enabled when this pin is low. A pull-up resistor is built in (hysteresis input).
10	SCLK	Clock input	Serial data input clock input. A pull-up resistor is built in (hysteresis input).
11	SIN	Data input	Serial data input. A pull-up resistor is built in (hysteresis input).
12	$V_{DD}2$	Power supply	Composite video signal level adjustment power supply (analog system power supply)
13	CV_{OUT}	Video signal output	Composite video signal output pin
14	NC		Must be either connected to ground or left open.
15	CV_{IN}	Video signal input	Composite video signal input pin
16	$V_{DD}1$	Power supply	Power supply (+5 V: digital system power supply)
17	SYN_{IN}	Sync separator circuit input	Video signal input to the built-in sync separator circuit
18	$V_{SS}1$	Ground	Ground (digital system ground)
19	SEP_{OUT}	Composite synchronizing signal output	Video signal output from the built-in sync separator circuit
20	SEP_{IN}	Vertical synchronizing signal input	Inputs the vertical synchronizing signal generated by integrating the SEP_{OUT} pin output signal. An integrating circuit must be inserted between the SEP_{OUT} pin and this pin. This pin must be tied to $V_{DD}1$ if unused.
21	$\overline{CS2}$	Enable input	Enable input for EDS data output. EDS data output is enabled when this input is low. A pull-up resistor is built in (hysteresis input).
22	CPDT	Data output	EDS data output (either an n-channel open-drain or a CMOS output circuit)
23	$\overline{RST}$	Reset input	System reset input. A pull-up resistor is built in (hysteresis input).
24	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

Note: Both $V_{DD}1$ pins must be connected to the power supply.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	$V_{DD}1$, $V_{DD}2$	V_{SS} – 0.3 to V_{SS} + 7.0	V
Maximum input voltage	V_{IN} max	All input pins	V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max	LN21, CPDT, SEP_{OUT}, $SYNC_{JDG}$	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta = 25°C	350	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = –30 to +70°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}1$	$V_{DD}1$	4.5	5.0	5.5	V
	$V_{DD}2$	$V_{DD}2$	4.5	5.0	1.27 $V_{DD}1$	V
Input high level voltage	$V_{IH}1$	$\overline{RST}$, $\overline{CS1}$, $\overline{CS2}$, SIN, SCLK	0.8 $V_{DD}1$		$V_{DD}1$ + 0.3	V
	$V_{IH}2$	CTRL1, SEP_{IN}	0.7 $V_{DD}1$		$V_{DD}1$ + 0.3	V
Input low level voltage	$V_{IL}1$	$\overline{RST}$, $\overline{CS1}$, $\overline{CS2}$, SIN, SCLK	V_{SS} – 0.3		0.2 $V_{DD}1$	V
	$V_{IL}2$	CTRL1, SEP_{IN}	V_{SS} – 0.3		0.3 $V_{DD}1$	V
Pull-up resistance	R_{PU}	Applies to $\overline{RST}$, $\overline{CS1}$, $\overline{CS2}$, SIN, SCLK, and the pins specified as options.	25	50	90	kΩ
Composite video input voltage	$V_{IN}1$	CV_{IN}: $V_{DD}1$ = 5 V		2.0		Vp-p
	$V_{IN}2$	SYN_{IN}: $V_{DD}1$ = 5 V	1.5	2.0	2.5	Vp-p
Input voltage	$V_{IN}3$	$Xtal_{IN}$ (when external clock input is used), f_{IN} = 2fsc or 4fsc: $V_{DD}1$ = 5 V	0.1		5.0	Vp-p
Oscillator frequency	$f_{OSC}1$	$Xtal_{IN}$, $Xtal_{OUT}$ oscillator pins (2fsc: NTSC)		7.159		MHz
	$f_{OSC}1$	$Xtal_{IN}$, $Xtal_{OUT}$ oscillator pins (4fsc: NTSC)		14.318		MHz
	$f_{OSC}1$	$Xtal_{IN}$, $Xtal_{OUT}$ oscillator pins (2fsc: PAL-M)		7.151		MHz
	$f_{OSC}1$	$Xtal_{IN}$, $Xtal_{OUT}$ oscillator pins (4fsc: PAL-M)		14.302		MHz
	$f_{OSC}2$	OSC_{IN}, OSC_{OUT} oscillator pins (LC oscillator)	5		12	MHz

Note: Extreme care must be used to prevent noise when the $Xtal_{IN}$ pin is used in clock input mode.

Electrical Characteristics at Ta = –30 to +70°C, and unless otherwise specified, with $V_{DD}1$ = 5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input off leakage current	$I_{leak}1$	CV_{IN}			1	µA
Output off leakage current	$I_{leak}2$	CV_{OUT}			1	µA
Output high level voltage	$V_{OH}1$	LN21, $SYNC_{JDG}$, CPDT, SEP_{OUT}: $V_{DD}1$ = 4.5 V, I_{OH} = –1.0 mA	3.5			V
Output low level voltage	$V_{OL}1$	LN21, $SYNC_{JDG}$, CPDT, SEP_{OUT}: $V_{DD}1$ = 4.5 V, I_{OL} = 1.0 mA			1.0	V
Input current	I_{IH}	$\overline{RST}$, $\overline{CS1}$, $\overline{CS2}$, SIN, SCLK, CTRL1, SEP_{IN}: V_{IN} = $V_{DD}1$			1	µA
	I_{IL}	CTRL1, OSC_{IN}: V_{IN} = $V_{SS}1$	–1			µA
Operating current drain	$I_{DD}1$	$V_{DD}1$: All outputs open, crystal: 7.159 MHz, LC: 8 MHz			30	mA
	$I_{DD}2$	$V_{DD}2$: $V_{DD}2$ = 5 V			20	mA
Sync level	V_{SN}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	0.69	0.81	0.98	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	0.89	1.01	1.13	V
Pedestal level	V_{PD}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.28	1.40	1.52	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.47	1.59	1.71	V
Color burst low level	V_{CBL}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	0.97	1.09	1.21	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.16	1.28	1.40	V
Color burst high level	V_{CBH}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.60	1.72	1.84	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.79	1.91	2.03	V
Background color low level	V_{RSL}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.44	1.56	1.68	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.63	1.75	1.87	V
Background color high level	V_{RSH}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.96	2.08	2.20	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	2.16	2.28	2.40	V

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Parameter	Symbol	Conditions	min	typ	max	Unit
Border level 0	V_{BK0}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.43	1.55	1.67	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.61	1.73	1.85	V
Border level 1	V_{BK1}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	2.01	2.13	2.25	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	2.18	2.30	2.42	V
Character level	V_{CHA}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	2.57	2.69	2.81	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	2.76	2.88	3.00	V

Timing Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 V ± 0.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
OSD write (See Figure 1.)						
Minimum input pulse width	$t_{W\ (SCLK)}$	SCLK	200			ns
	$t_{W\ (CS1)}$	$\overline{CS1}$ (the period when $\overline{CS1}$ is high)	1			µs
Data setup time	$t_{SU\ (CS1)}$	$\overline{CS1}$	200			ns
	$t_{SU\ (SIN)}$	SIN	200			ns
Data hold time	$t_{h\ (CS1)}$	$\overline{CS1}$	2			µs
	$t_{h\ (SIN)}$	SIN	200			ns
One-word write time	t_{word}	The time to write 8 bits of data	4.2			µs
	t_{wt}	The RAM data write time	1			µs
ESD read (See Figure 2 for the n-channel open-drain circuit.)						
Minimum input pulse width	t_{CKCY}	SCLK	2			ns
	t_{CKL}	SCLK	1			µs
	t_{CKH}	SCLK	1			µs
Data setup time	t_{ICK}	SCLK	10			µs
Output delay time	t_{CKO}	CPDT			0.5	µs

Note: Follows the OSD timing for the CMOS output circuit type.

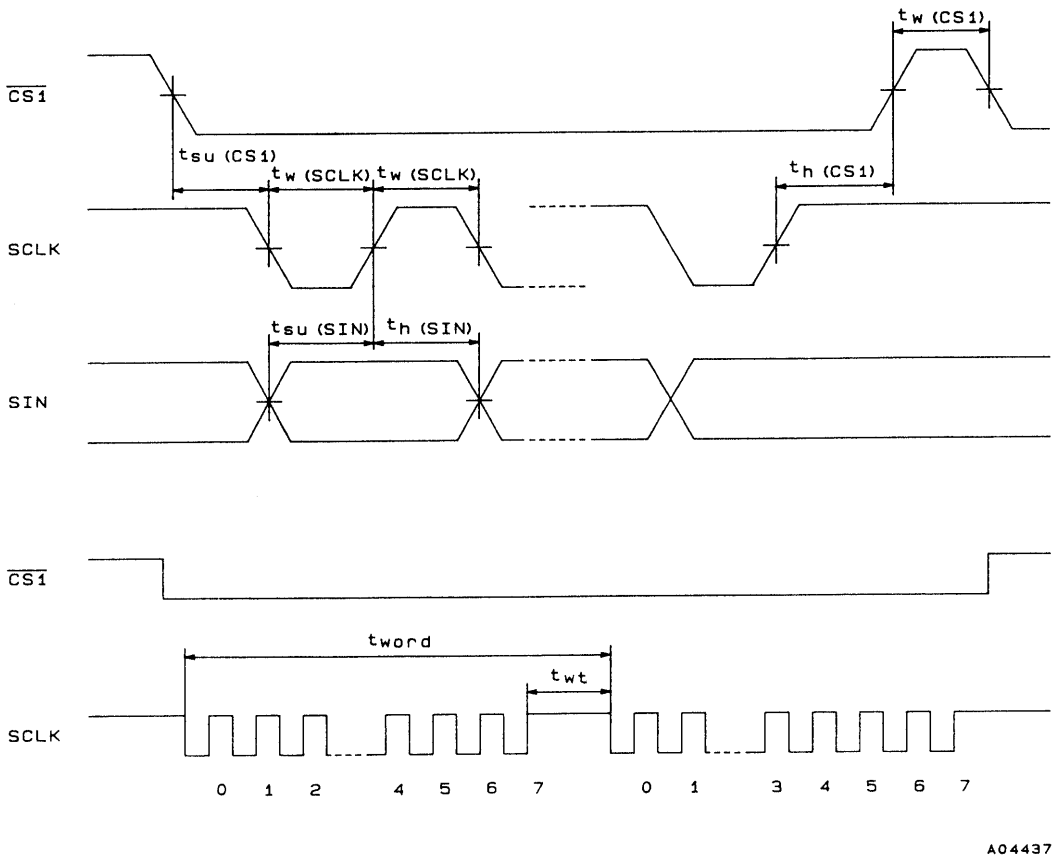
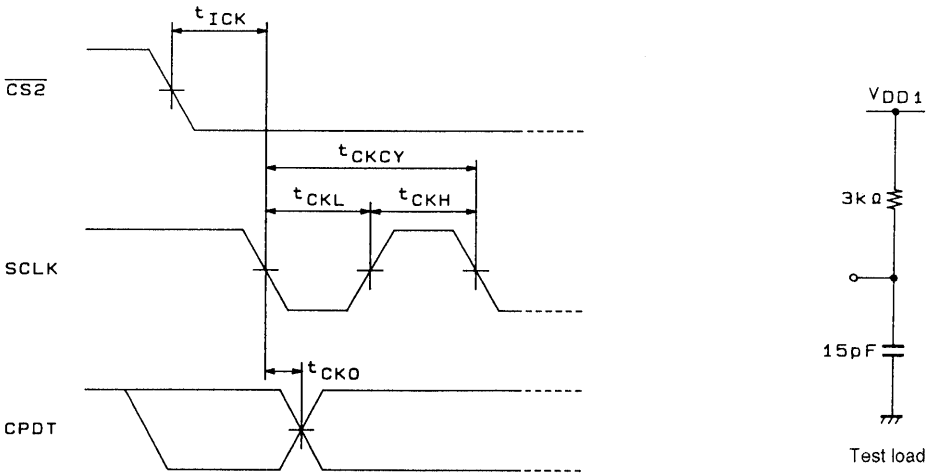


Figure 1 OSD Serial Data Input Timing



Note: CPDT goes to the high-impedance state when $\overline{CS2}$ is high.

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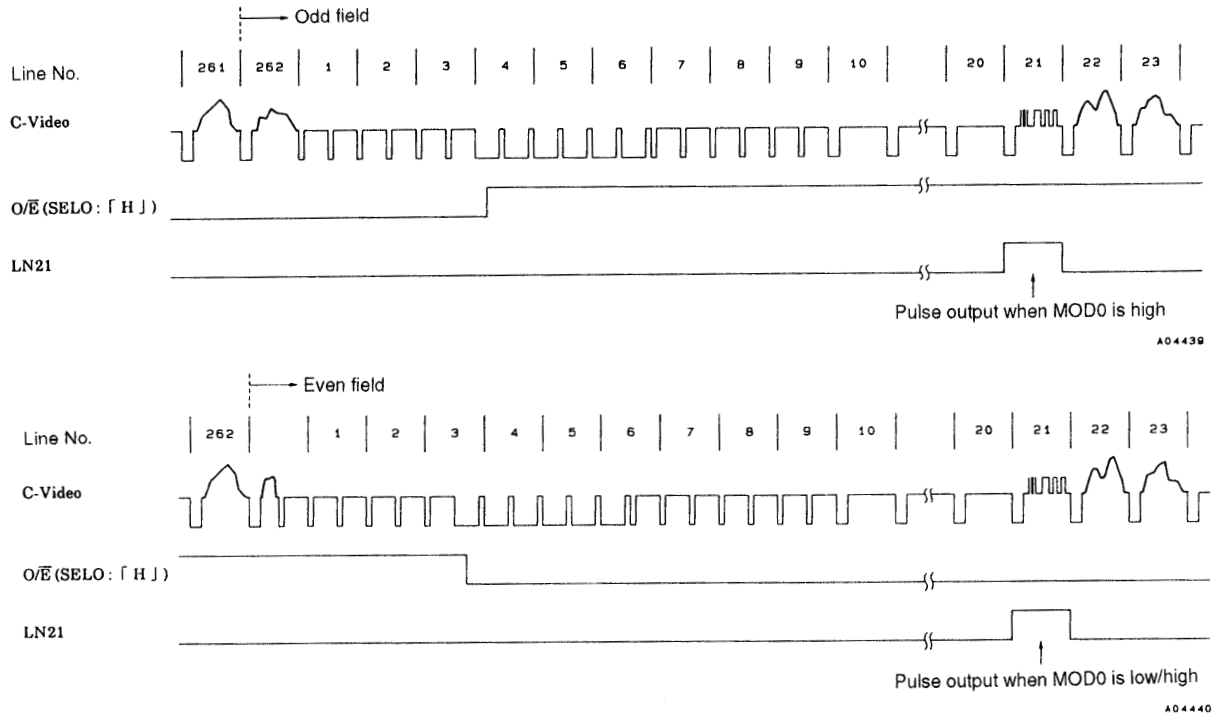
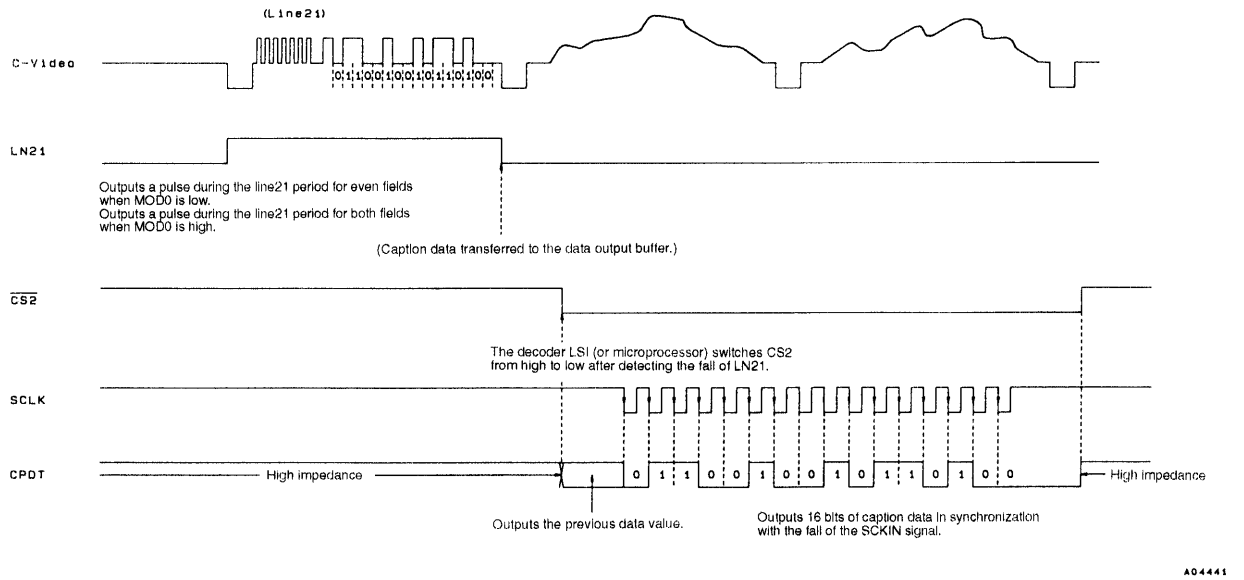
Figure 2 EDS Serial Output Test Conditions (N-Channel Open-Drain Circuit)



Note: The O/$\overline{E}$ signal is output from the $SYNC_{JDG}$ pin when SEL0 is high.
LN21 outputs the even field when MOD0 is low, and both fields when MOD0 is high.

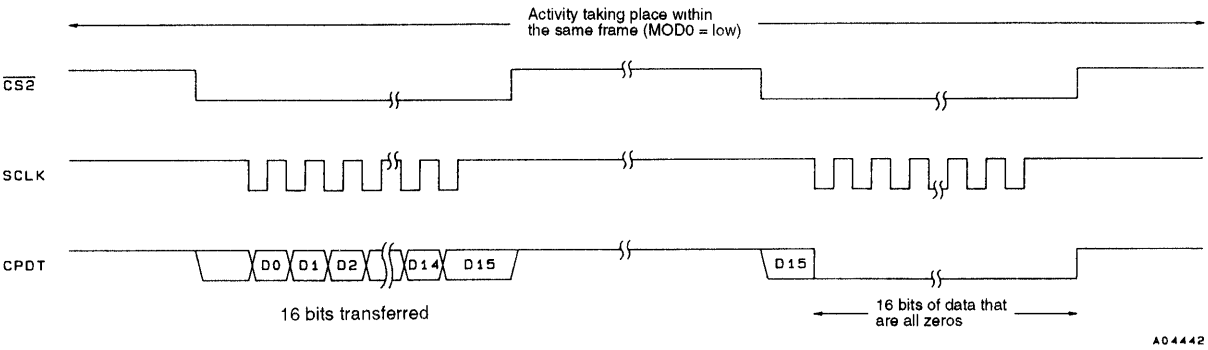
Figure 3 O/$\overline{E}$ and LN21 Output Timing



Note: When closed caption character data is extracted in NTSC-TV mode (MOD0 is high), the control microprocessor can determine whether the current field is an odd field or an even field by checking the signal level output by the $SYNC_{JDG}$ pin (when SEL0 is high) at the point it detects the rise of the LN21 signal.

Figure 4 LC74725/M to Decoder LSI (or Microprocessor) Caption Data Transfer Technique 1 (This is the basic usage mode for these LSIs.)

Caption data transfer to the data output buffer is synchronized with the falling edge of the pulse output from LN21. Therefore, the following software processing is required if the decoder LSI (or microprocessor) does not detect the fall of LN21.

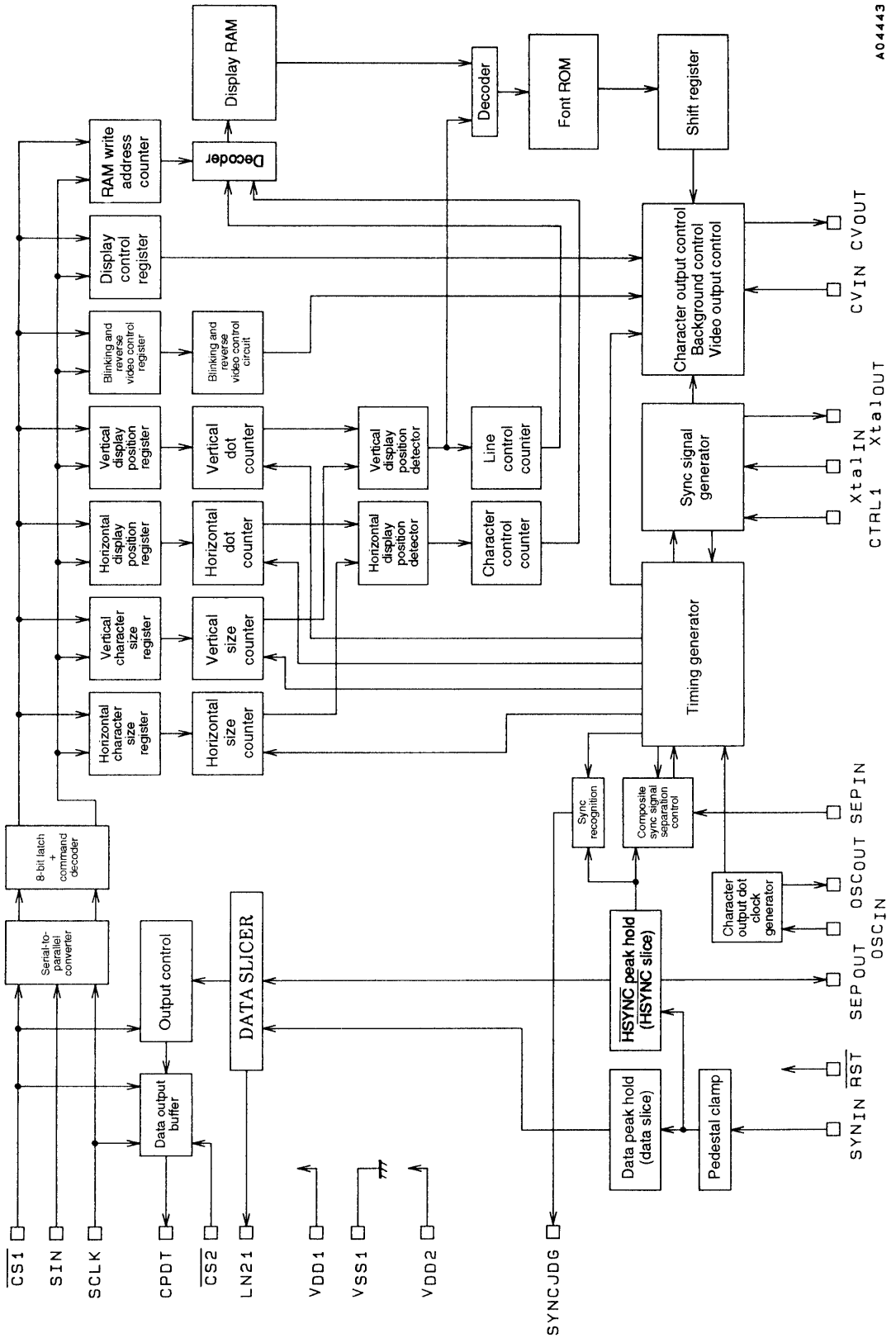


When MOD0 is low, since the data is output to the data buffer once (during the even field) in a single frame, the decoder LSI (or microprocessor) must perform the transfer control operation at least twice per frame (about 32 ms).
When the transfer control operation is performed twice in the same frame, the second CPDT 16 bits of output data are all zeros. Therefore, the microprocessor must determine that the data for the next frame had not been transferred to the output buffer in this case.

Note: The LC74725 hardware will not transfer data to the output buffer while $\overline{CS2}$ is low. Therefore the decoder LSI (or microprocessor) must restore $\overline{CS2}$ from the low level to the high level after completing a data transfer control cycle.
This transfer technique (technique 2) cannot be used in NTSC-TV mode, i.e., when MOD0 is high.

Figure 5 LC74725/M to Decoder LSI (or Microprocessor) Caption Data Transfer Technique 2 (When a port to detect the fall of LN21 cannot be allocated in the decoder LSI (or Microprocessor).)

System Block Diagram



Display Control Commands

Display control commands have an 8-bit format and are transferred using the serial input function. Commands consist of a command identification code in the first byte and command data in the following bytes. The following commands are supported.

① COMMAND0: Display memory (VRAM) write address setup command
② COMMAND1: Display character data write command
③ COMMAND2: Vertical display start position and vertical character size setup command
④ COMMAND3: Horizontal display start position and horizontal character size setup command
⑤ COMMAND4: Display control setup command
⑥ COMMAND5: Display control setup command

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Set write address	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Write character	1	0	0	1	0	0	0	0	at	0	c5	c4	c3	c2	c1	c0
COMMAND2 Set vertical display start position and vertical character size	1	0	1	0	0	VS 20	0	VS 10	0	FS	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 Set horizontal display start position and horizontal character size	1	0	1	1	EGP	HS 20	0	HS 10	0	LC	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 Display control	1	1	0	0	TST MOD	RAM ERS	OSC STP	SYS RST	0	EGL	NON	EG	BK 1	BK 0	RV	DSP ON
COMMAND5 Synchronizing signal control	1	1	0	1	BCL	PH	RSN	INT	0	0	0	MUT	MOD 0	CTL 3	CTL 2	SEL 0

Once written, the command identification code in the first byte is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74725/M locks into the display character data write mode, and another first byte cannot be written.
When a high level is input to the $\overline{CS}$ pin, the LC74725/M is set to COMMAND0 (display memory write address setup mode).

① COMMAND0 (Display memory write address setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 0 identification code Set the display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory row address (0 to 9 hexadecimal)	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	H4	0	Display memory column address (0 to 17 hexadecimal)	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

② COMMAND1 (Display character data write setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 1 identification code Set up display character data write.	When this command is input, the LC74725/M locks into the display character data write mode until the $\overline{CS1}$ pin goes high.
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	—	0		

Second byte

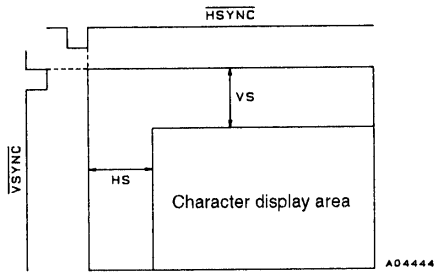
DA0 to DA7	Register name	Register content		Note
		State	Function	
7	at	0	Character attribute off	
		1	Character attribute on	
6	—	0		
5	c5	0	Character code (00 to 3F hexadecimal)	
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

③ COMMAND2 (Vertical display start position and vertical character size setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 2 identification code Set the vertical display start position and vertical character size.	
6	—	0		
5	—	1		
4	—	0		
3	—	0		
2	VS20	0	1H per dot	Second line vertical character size
		1	2H per dot	
1	—	0		
0	VS10	0	1H per dot	First line vertical character size
		1	2H per dot	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	FS	0	Crystal oscillator frequency: 2fsc	
		1	Crystal oscillator frequency: 4fsc	
5	VP5 (MSB)	0	If VS is the vertical display start position then: $VS = H \times (2\sum_{n=0}^{5} 2^n VP_n)$ H: the horizontal synchronization pulse period  	The vertical display start position is set by the 6 bits VP0 to VP5. The weight of bit 1 is 2H.
		1		
4	VP4	0		
		1		
3	VP3	0		
		1		
2	VP2	0		
		1		
1	VP1	0		
		1		
0	VP0 (LSB)	0		
		1		

④ COMMAND3 (Horizontal display start position and horizontal character size setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 3 identification code Set the horizontal display start position and horizontal character size.	
6	—	0		
5	—	1		
4	—	1		
3	EGP	0	Correction: off	Border specification when the horizontal double character size is used
		1	Correction: on	
2	HS20	0	1 Tc per dot	Second line horizontal character size
		1	2 Tc per dot	
1	—	0		
0	HS10	0	1 Tc per dot	First line horizontal character size
		1	2 Tc per dot	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	LC	0	An LC oscillator is used for the dot clock.	Selects the dot clock used in horizontal character display.
		1	A crystal oscillator is used for the dot clock.	
5	HP5 (MSB)	0	If HS is the horizontal start position then: $HS = Tc \times (2\sum_{n=0}^{5} 2^n HP_n)$ Tc: Period of the oscillator connected to OSCIN/OSCOUT in operating mode.	The horizontal display start position is set by the 6 bits HP0 to HP5. The weight of bit 1 is 2Tc.
		1		
4	HP4	0		
		1		
3	HP3	0		
		1		
2	HP2	0		
		1		
1	HP1	0		
		1		
0	HP0 (LSB)	0		
		1		

⑤ COMMAND4 (Display control setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 4 identification code Display control setup	
6	—	1		
5	—	0		
4	—	0		
3	TSTMOD	0	Normal operating mode	This bit must be zero.
		1	Test mode	
2	RAMERS	0		The RAM erase operation requires about 500 µs (It is executed in the DSPOFF state.)
		1	Erase display RAM (set to 3F hexadecimal)	
1	OSCSTP	0	Do not stop the crystal oscillator and LC oscillator circuits.	Valid when character display is off in external synchronization mode.
		1	Stop the crystal oscillator and LC oscillator circuits.	
0	SYSRST	0		Reset occurs when the $\overline{CS1}$ pin is low, and the reset is cleared when $\overline{CS1}$ goes high.
		1	Reset all registers and turn the display off.	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	EGL	0	Border level 0 (V_{BK0})	Switches the border level
		1	Border level 1 (V_{BK1})	
5	NON	0	Interlaced (262.5H per field)	Switches between interlaced and noninterlaced
		1	Noninterlaced (263H per field)	
4	EG	0	Border off	
		1	Border on	
3	BK1	0	Blinking period: about 0.5 s	Switches the blinking period.
		1	Blinking period: about 1.0 s	
2	BK0	0	Blinking off	When blinking is specified for reversed characters, the blinking will be between normal character and reversed character display.
		1	Blinking on	
1	RV	0	Reverse (character reversing) off	
		1	Reverse (character reversing) on	
0	DSPON	0	Character display off	
		1	Character display on	

⑥ COMMAND5 (Display control setup command)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 5 identification code Synchronizing signal control settings	
6	—	1		
5	—	0		
4	—	1		
3	BCL	0	Background color present	Only valid in internal synchronization mode
		1	No background color (only the background level is set)	
2	PH	0	Green background	Background color switching (Only valid in NTSC mode) (In PAL-M mode, only blue is available as the background color.)
		1	Blue background	
1	RSN	0	External synchronizing signal detection control: Off	External synchronizing signal detection control. Determines when the signal goes from detected to undetected, and from undetected to detected.
		1	External synchronizing signal detection control: On	
0	INT	0	External synchronization	Switches between external and internal synchronization
		1	Internal synchronization	

Second byte

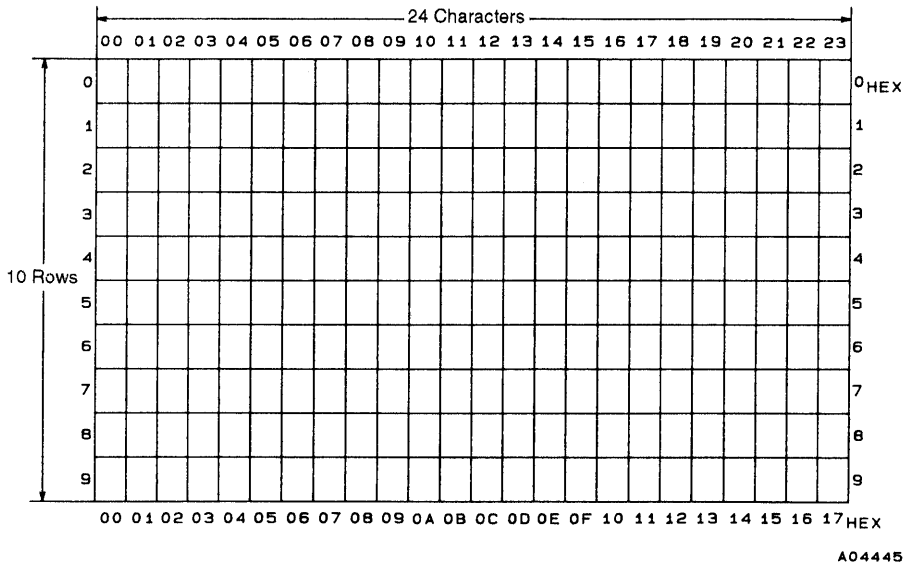
DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	MUT	0	Normal output	Switches CV_{OUT}.
		1	CV_{IN} is cut and CV_{OUT} is fixed at the pedestal level.	
3	MOD0	0	Even field line 21 data extraction (VCR)	Switches line 21 data extraction operation.
		1	Both even and odd field line 21 data extraction (NTSC-TV)	
2	CTL3	0	Internal V separation used.	Switches V separation usage.
		1	Internal V separation not used.	
1	CTL2	0	NTSC	Switches between generation of NTSC and PAL-M signals.
		1	PAL-M	
0	SEL0	0	External synchronizing signal detection output signal	Switches $SYNC_{JDG}$ (pin 21) output.
		1	$O/\overline{E}$ signal	

Note: The register states are all set to zero when the LC74725/M is reset with the $\overline{RST}$ pin.

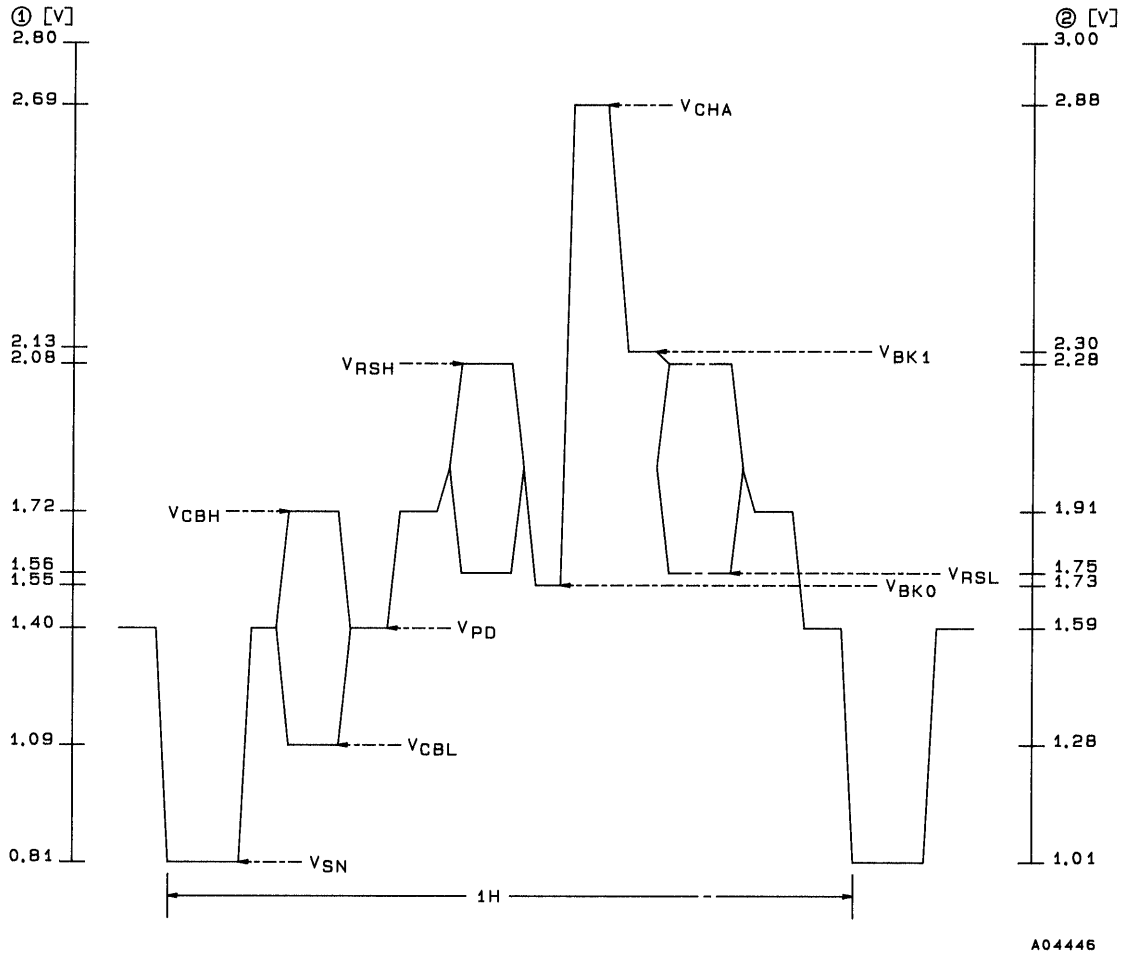
Display Screen Structure

The display consists of 10 lines of 24 characters each and thus up to 240 characters can be displayed. Enlarging the size of the characters reduces the number of characters that can be displayed to under 240 characters.
Display memory addresses are specified as row (0 to 9 decimal) and column (0 to 23 decimal) addresses.

Display Screen Structure (display memory addresses)



Composite Video Signal Output Level (internally generated level)



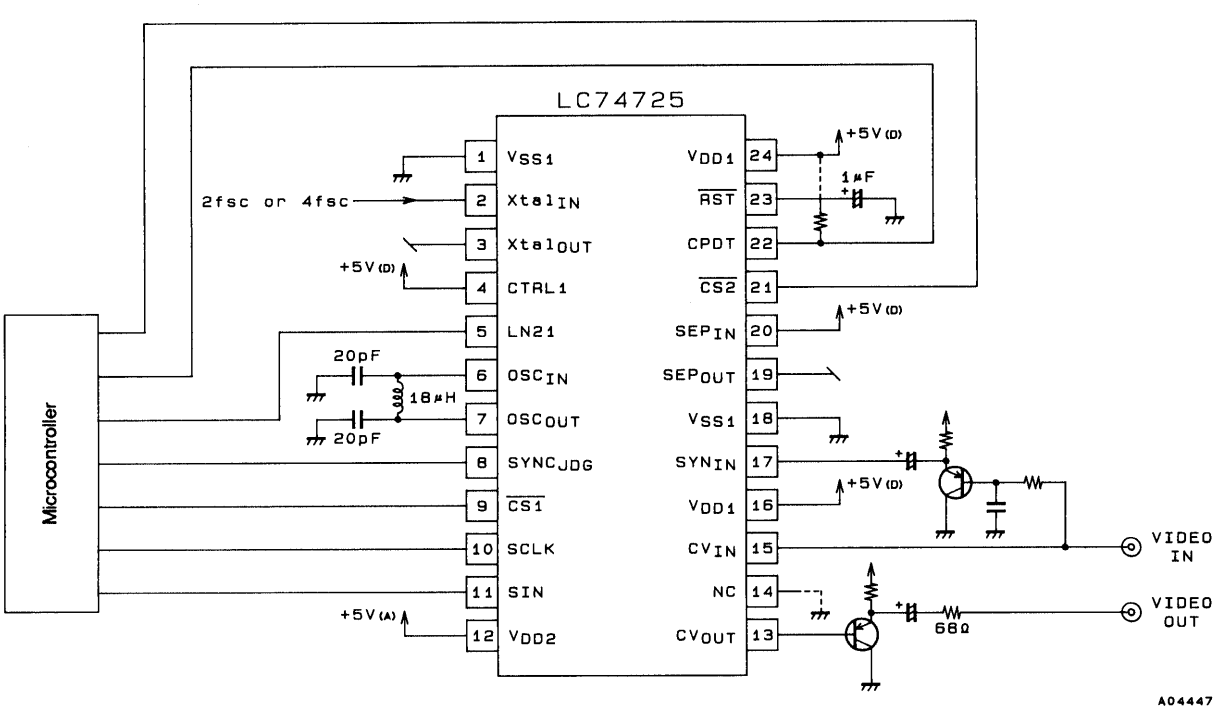
CV_{OUT} Output Level Waveform ($V_{DD}2$ = 5.00 V)

Output level	Output voltage ① [V]	Output voltage ② [V]
V_{CHA}: Character	2.69	2.88
V_{RSH}: Background color high	2.08	2.28
V_{CBH}: Color burst high	1.72	1.91
V_{RSL}: Background color low	1.56	1.75
V_{BK1}: Border	2.13	2.30
V_{BK0}: Border	1.55	1.73
V_{PD}: Pedestal	1.40	1.59
V_{CBL}: Color burst low	1.09	1.28
V_{SN}: Sync	0.81	1.01

$V_{DD}2$ = 5.00 V

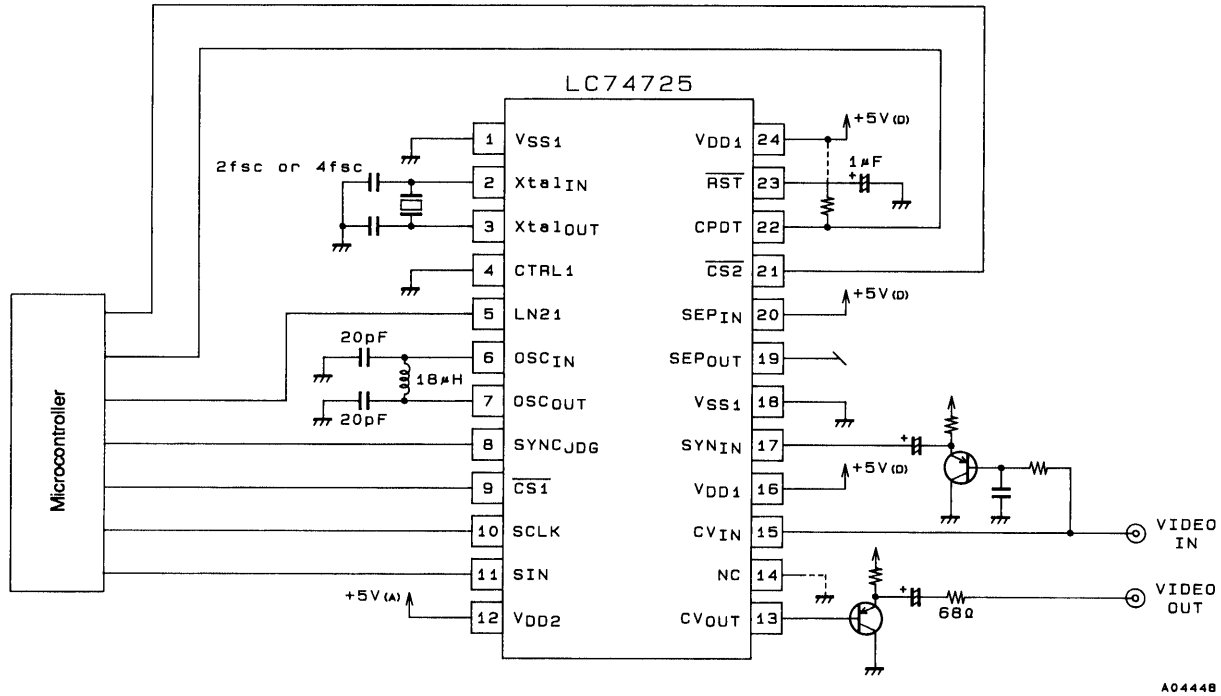
Application Circuit Examples (Connected to a Y/C1 chip)

1. External system clock input



Note: Values listed are reference values.

2. Crystal oscillator clock generation



Note: Values listed are reference values.