Ordering number : EN5680

CMOS IC

# LC7455A, 7455M

## Closed Caption Signal Extraction IC

## Overview

The LC7455A/M extracts the closed caption signal superimposed on a video signal during the vertical return period and, under the control of a clock signal provided by the decoder IC, transfers that signal to the IC (usually a microcontroller) that decodes the closed caption data. The LC7455A/M supports four operating modes. Modes 1 and 2 can be used for XDS. In these modes, the LC7455A/M, in combination with the decoder IC (microcontroller), extracts the caption signal superimposed on field 2 and uses it for NTSC VCR functions such as the automatic time and date setting function. In modes 3 and 4, the LC7455A/M, in combination with the decoder IC (microcontroller), extracts the caption signal superimposed on fields 1 and 2 and uses it for NTSC TV applications (mode 3) or PAL TV applications (mode 4).

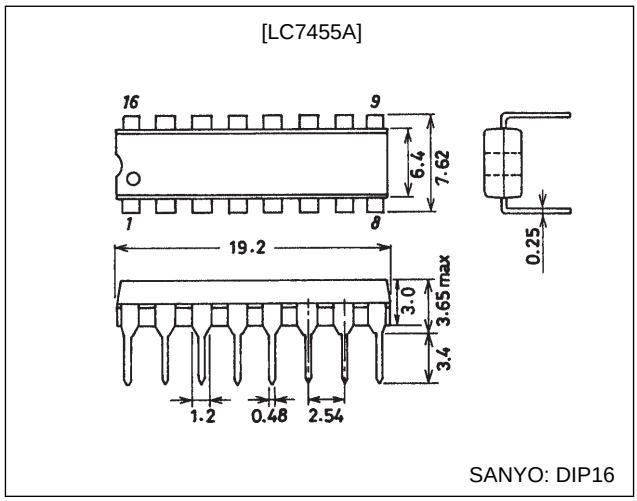
## Functions

- Low power dissipation achieved by fabrication in a CMOS process.
- Stable caption signal extraction achieved by a built-in peak hold circuit and the use of digital technology.
- Operating supply voltage: 5 V ±10%
- Package LC7455A: 16-pin DIP
  LC7455M: 18-pin MFP

## Package Dimensions

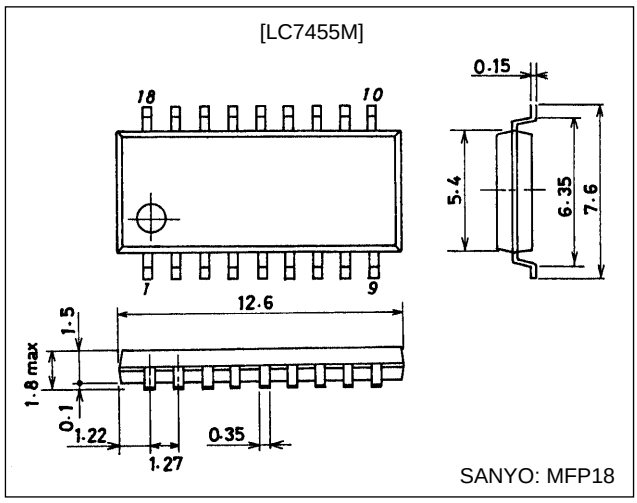
unit: mm

**3006B-DIP16**

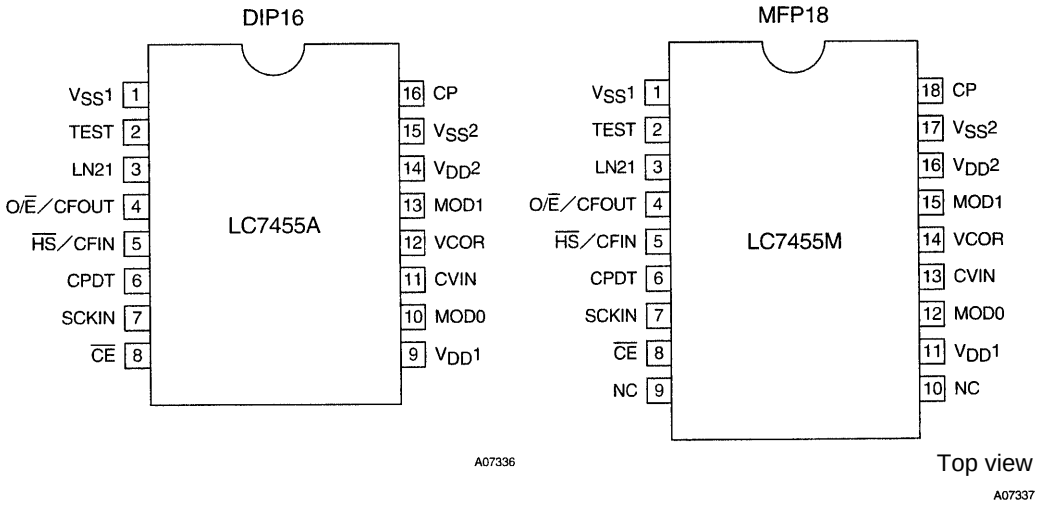



unit: mm

**3095-MFP18**



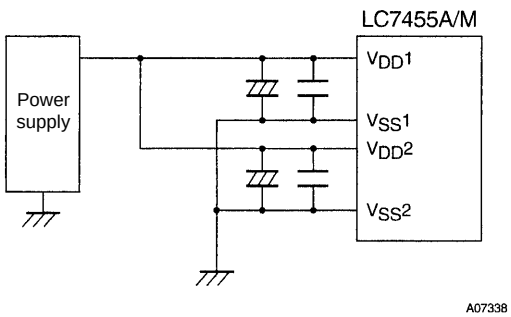
## Pin Assignments



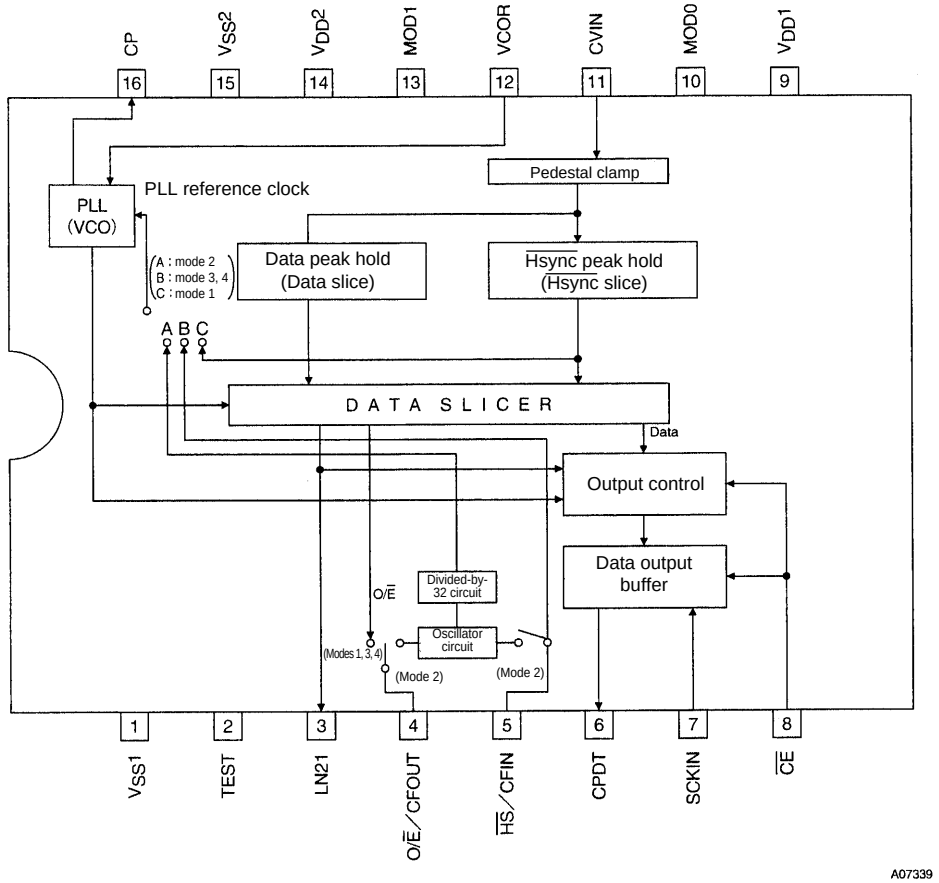

## Pin Functions

| Pin | Pin No. | | Pin function | | | |
|---|---|---|---|---|---|---|
| | DIP16 | MFP18 | Mode 1 | Mode2 | Mode3 | Mode4 |
| $V_{SS}1$ | 1 | 1 | Ground | | | |
| TEST | 2 | 2 | Test pin. Must be left open during normal operation. | | | |
| LN21 | 3 | 3 | Line 21H pulse output (even field) | | Line 21H pulse output (both fields) | Line 22H pulse output (both fields) |
| O/$\overline{E}$/CFOUT | 4 | 4 | Field discrimination pulse output | Ceramic oscillator output | Field discrimination pulse output | |
| $\overline{HS}$/CFIN | 5 | 5 | Sync separator $\overline{Hsync}$ pulse output | Ceramic oscillator input | $\overline{Hsync}$ pulse input | |
| CPDT | 6 | 6 | Caption data output (n-channel open-drain output) | | | |
| SCKIN | 7 | 7 | Caption data transfer clock input | | | |
| $\overline{CE}$ | 8 | 8 | Chip select input | | | |
| $V_{DD}1$ | 9 | 11 | Power supply | | | |
| MOD0 | 10 | 12 | Leave open | Short to the power supply | Leave open | Short to the power supply |
| CVIN | 11 | 13 | Composite video input | | | |
| VCOR | 12 | 14 | Connection for an external resistor to control the built-in VCO oscillator frequency | | | |
| MOD1 | 13 | 15 | Leave open | | Short to the power supply | |
| $V_{DD}2$ | 14 | 16 | Power supply | | | |
| $V_{SS}2$ | 15 | 17 | Ground | | | |
| CP | 16 | 18 | Connection for the filter used by the built-in PLL | | | |

Note: $V_{DD}1$ and $V_{SS}1$ are the power supply for the digital block, and $V_{DD}2$ and $V_{SS}2$ are the power supply for the analog block. Use a circuit similar to the one shown below to minimize mutual interference due to noise from these blocks.



## System Block Diagram




## Operation in the Different Modes

| Pin | | Mode | Application equipment | Operation |
|---|---|---|---|---|
| MOD1 | MOD0 | | | |
| Open | Open | Mode 1 | VCR | · Even field line 21 data extraction<br>The internal PLL is operated with the horizontal synchronizing signal separated from the composite video signal as the reference. |
| Open | $V_{DD}$ | Mode 2 | VCR | · Even field line 21 data extraction<br>An external 508 kHz ceramic oscillator is used, and the internal PLL is operated with that oscillator output divided by 32 as the reference. |
| $V_{DD}$ | Open | Mode 3 | NTSC-TV | · Odd and even field line 21 data extraction<br>The internal PLL is operated with the $\overline{\text{Hsync}}$ signal applied from fly back as the reference. |
| $V_{DD}$ | $V_{DD}$ | Mode 4 | PAL-TV | · Odd and even field line 22 data extraction<br>The internal PLL is operated with the $\overline{\text{Hsync}}$ signal applied from the fly back circuit as the reference. |

Note: The data extraction operations in modes 1 and 2 are identical. However, while mode 1 can operate without problem for normal "on air" signals, it may be difficult for the PLL to lock with signals such as scrambled CATV signals.

# Specifications

## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}1$, $V_{DD}2$: $V_{DD}1 = V_{DD}2$ | –0.3 to +7.0 | V |
| Input voltage | $V_I$ | $\overline{HS}$/CFIN, CVIN, SCKIN, $\overline{CE}$ | –0.3 to $V_{DD}$ +0.3 | V |
| Output voltage | $V_O$ | LN21, CPDT, O/$\overline{E}$/CFOUT, $\overline{HS}$/CFIN | –0.3 to $V_{DD}$ +0.3 | V |
| Allowable power dissipation | Pd max | LC7455A | 300 | mW |
| | | LC7455M | 150 | mW |
| Operating temperature | Topr | | –30 to +70 | °C |
| Storage temperature | Tstg | | –55 to +150 | °C |

Note: $V_{SS}1$ and $V_{SS}2$ must be at the same potential.
$V_{DD}1$ and $V_{DD}2$ must be at the same potential.

## Allowable Operating Ranges at Ta = –30 to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Operating supply voltage | $V_{DD}$ | $V_{DD}1$, $V_{DD}2$ : $V_{DD}1 = V_{DD}2$ | 4.5 | | 5.5 | V |
| Input high-level voltage | $V_{IH}$ | $\overline{HS}$/CFIN, SCKIN, $\overline{CE}$; $V_{DD}$ = 4.5 to 5.5 V | 0.75 $V_{DD}$ | | $V_{DD}$ | V |
| Input low-level voltage | $V_{IL}$ | $\overline{HS}$/CFIN, SCKIN, $\overline{CE}$; $V_{DD}$ = 4.5 to 5.5 V | $V_{SS}$ | | 0.25$V_{DD}$ | V |
| CVIN input amplitude | CVSYNC | CVIN : SYNC-WHITE = 1.0 V; $V_{DD}$ = 4.5 to 5.5 V | 1Vp-p – 3dB | 1Vp-p | 1Vp-p + 3dB | V |
| $\overline{HS}$ input frequency range | $f_H$ | $\overline{HS}$/CFIN : $V_{DD}$ = 4.5 V<br>For mode 3<br>For mode 4 | <br>15.23<br>15.13 | <br>15.73<br>15.63 | <br>16.23<br>16.13 | <br>kHz<br>kHz |
| Oscillator frequency range*1 | FmCF | $\overline{HS}$/CFIN, O/$\overline{E}$/CFOUT; For mode 2, see Figure 1. $V_{DD}$ = 4.5 to 5.5 V | 503 | 508 | 513 | kHz |
| Oscillator stabilization time*2 | tmsCF | $\overline{HS}$/CFIN, O/$\overline{E}$/CFOUT; For mode 2, see Figure 2. $V_{DD}$ = 4.5 to 5.5 V | | 0.5 | 5 | ms |

Note: 1. See Table 1 for more information on the oscillator frequency.
2. The oscillator stabilization time is the time required until the oscillator is stable after the power-supply voltage is applied. See figure 2.

## Electrical Characteristics at Ta = –30 to +70°C, $V_{SS}$ = 0 V.

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Input high-level current | $I_{IH}$ | $\overline{HS}$/CFIN, SCKIN, $\overline{CE}$ : $V_{IN} = V_{DD}$; $V_{DD}$ = 4.5 to 5.5 V | | | 1 | µA |
| Input low-level current | $I_{IL}$ | $\overline{HS}$/CFIN, SCKIN, $\overline{CE}$ : $V_{IN} = V_{SS}$; $V_{DD}$ = 4.5 to 5.5 V | –1 | | | µA |
| Output high-level voltage | $V_{OH}$ | LN21, O/$\overline{E}$/CFOUT, $\overline{HS}$/CFIN; $I_{OH}$ = –4 mA ; $V_{DD}$ = 4.5 to 5.5 V | $V_{DD}$ – 1.2 | | | V |
| Output low-level voltage | $V_{OL}$ | LN21, CPDT, O/$\overline{E}$/CFOUT, $\overline{HS}$/CFIN : $I_{OL}$ = 10 mA; $V_{DD}$ = 4.5 to 5.5 V | | | 1 | V |
| Input clamping voltage | $V_{CLMP}$ | CVIN ; $V_{DD}$ = 5.0 V | 2.3 | 2.5 | 2.7 | V |
| Input clamping current | $I_{IC}$ | CVIN : CVIN = 3 V ; $V_{DD}$ = 5.0 V | 5 | 10 | 18 | µA |
| Output clamping current | $I_{OC}$ | CVIN : CVIN = 2 V ; $V_{DD}$ = 5.0 V | –120 | –70 | –30 | µA |
| Current drain | $I_{DD}$ | $V_{DD}1$, $V_{DD}2$ ; $V_{DD}$ = 4.5 to 5.5 V | | 6 | 15 | mA |

## Serial Output Characteristics at Ta = –30 to +70°C, $V_{SS}$ = 0 V, $V_{DD}$ = 4.5 to 5.5 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| [Serial clock] | | | | | | |
| Input clock period | $t_{CKCY}$ | SCKIN : See Figure 3. | 1 | | | µs |
| Input clock low-level pulse width | $t_{CKL}$ | SCKIN : See Figure 3. | 0.5 | | | µs |
| Input clock high-level pulse width | $t_{CKH}$ | SCKIN : See Figure 3. | 0.5 | | | µs |
| Setup time | $t_{ICK}$ | SCKIN : Stipulated with respect to the falling edge of $\overline{CE}$. | 1 | | | µs |
| [Serial output] | | | | | | |
| Output delay time | $t_{CKO}$ | Stipulated with respect to the falling edge of SCKIN. A 1-kΩ external pull-up resistor is connected. See Figure 3. | | | 0.5 | µs |

## Table 1 Ceramic Oscillator Guaranteed Constants

| Oscillator type | Manufacturer | Oscillator element | C1 | C2 |
|---|---|---|---|---|
| 508-kHz ceramic oscillator | Murata Mfg. Co., Ltd. | CSB 508E | 150 pF | 150 pF |

Note: Capacitors with K tolerance (±10%) and SL characteristics must be used for C1 and C2.
- Since this circuit is influenced by the length of the circuit pattern, components related to oscillator functioning must be mounted as close together as possible so that pattern lines do not become longer than is absolutely necessary.
- The characteristics are not guaranteed if an oscillator element other than the one listed above is used.

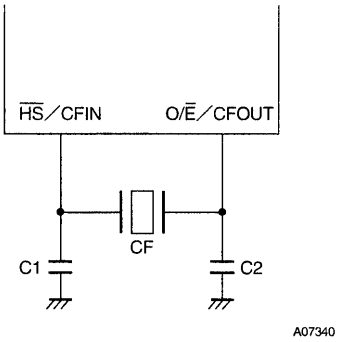



**Figure 1 Ceramic Oscillator**

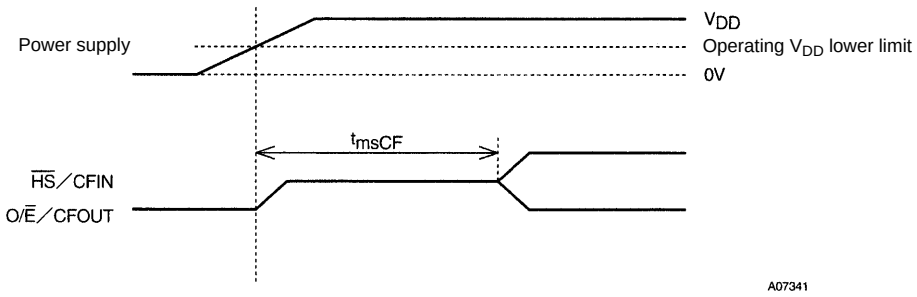
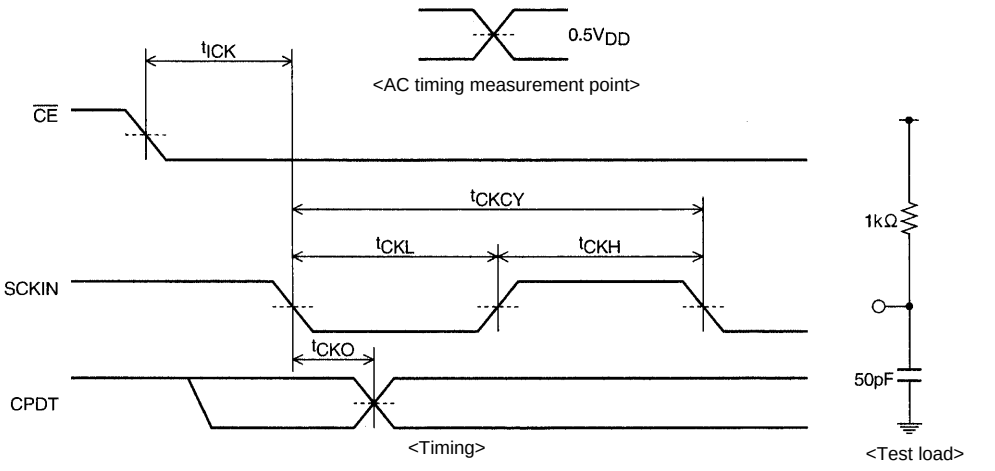


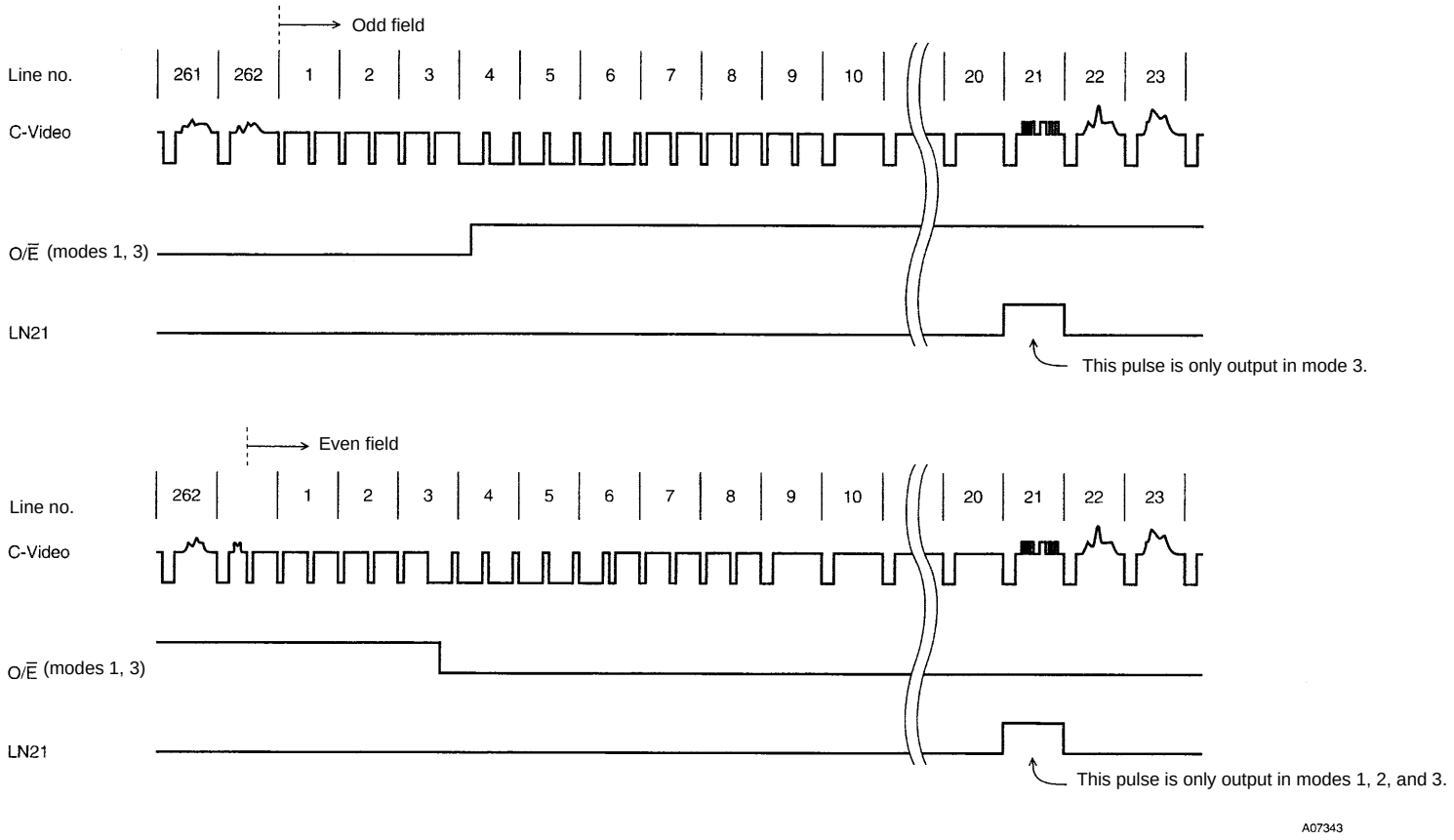

**Figure 2 Oscillator Stabilization Time**




Note: CPDT goes to the high-impedance state while $\overline{CE}$ is high.

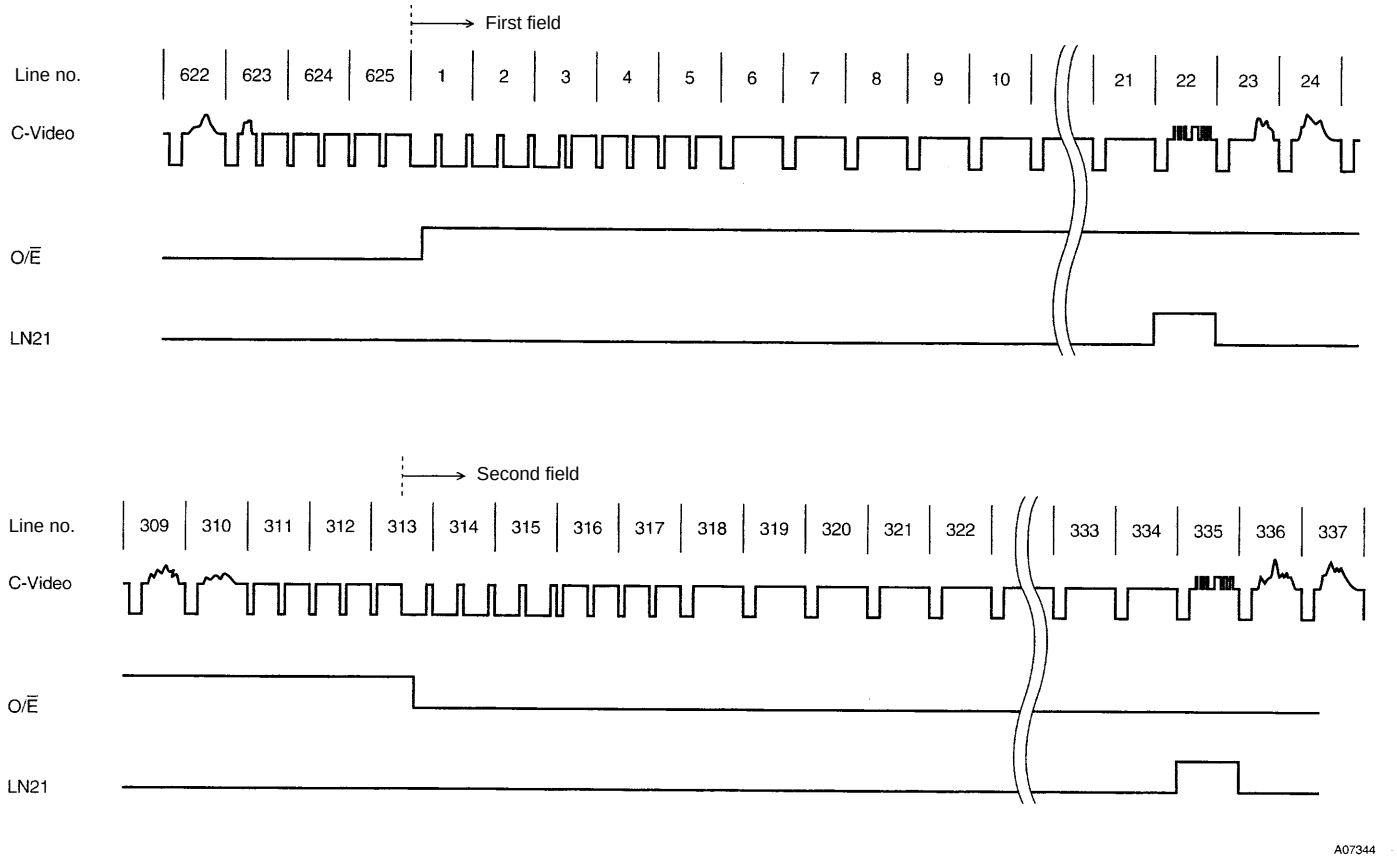
**Figure 3 Serial Output Test Conditions**

## O/$\overline{E}$ and LN21 Output Timing (Modes 1, 2, and 3)

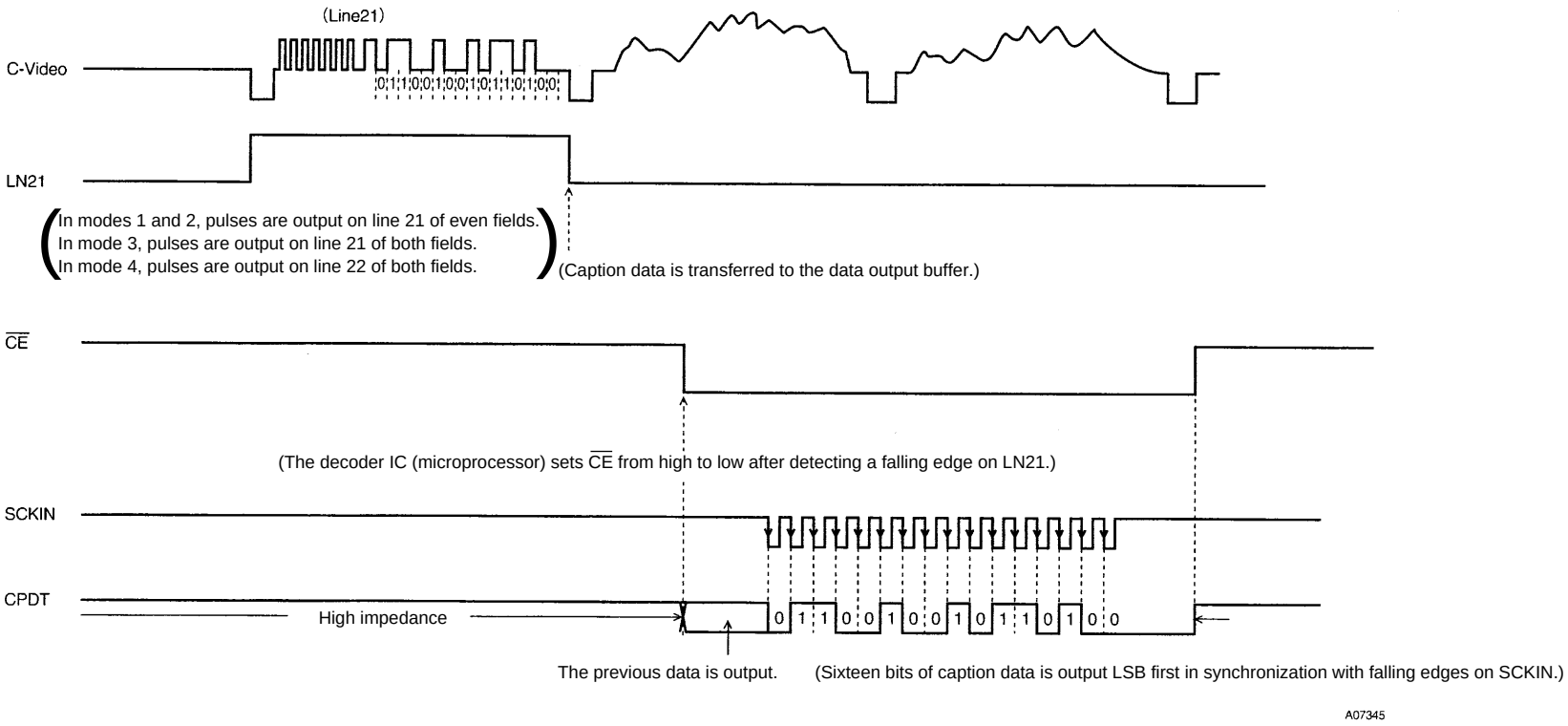



Notes: O/$\overline{E}$ is output in modes 1 and 3. In mode 2 it functions as the ceramic oscillator output pin.
LN21 is output for even fields in modes 1 and 2, and for both fields in mode 3.

## O/$\overline{E}$ and LN21 Output Timing (Mode 4)



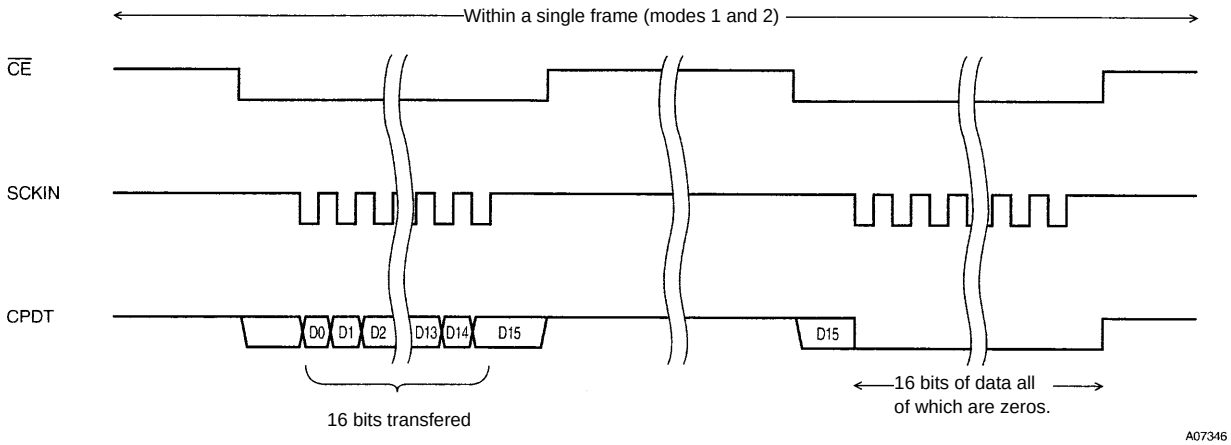
## Caption Data Transfer from the LC7455A/M to the Decoder IC (microcontroller): Method 1 (This is the basic technique.)




Notes: Applications that extract closed caption text data in mode 3 (NTSC TV) or mode 4 (PAL TV) must check the level of the O/$\overline{E}$/CFOUT pin when an LN21 falling edge is detected to determine whether odd field or even field data is being acquired.

## Caption Data Transfer from the LC7455A/M to the Decoder IC (microcontroller): Method 2

(For applications that cannot provide an input port on the decoder IC (microcontroller) to detect LN21 falling edges.)

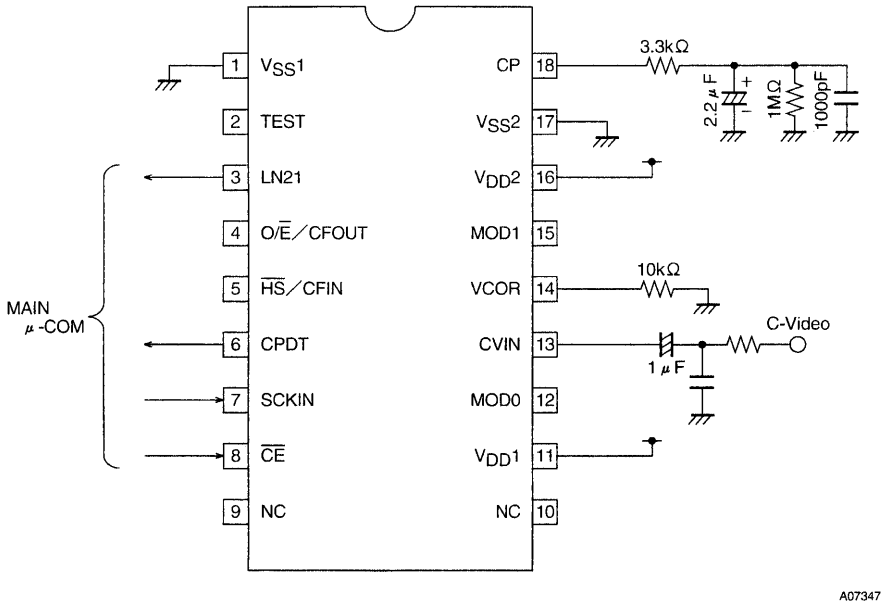



In modes 1 and 2, since data is output to the output buffer once every frame (in the even field), the decoder IC (microcontroller) must perform a transfer control operation at least twice every frame (about 32 ms).
When the second control operation is performed in a given frame, the CPDT output for that second operation will be 16 bits of zeros. This allows the microprocessor to recognize that the data for the next frame has not yet been transferred to the output buffer.

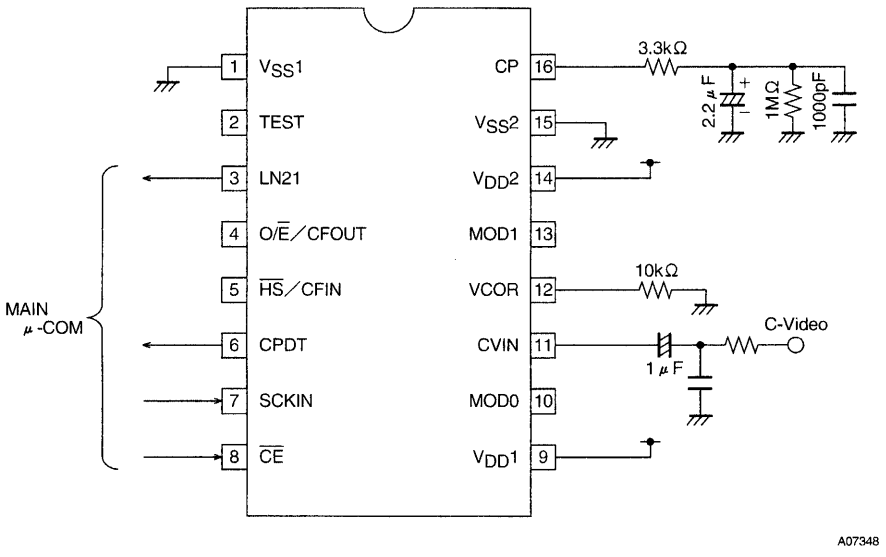
Notes: When $\overline{CE}$ remains low, the hardware will not transfer the data to the output buffer. Thus applications must restore $\overline{CE}$ from low to high after each data transfer to the decoder IC (microcontroller) operation has completed.
This transfer technique (method 2) cannot be used in modes 3 and 4.

## Sample Application Circuits (mode 1)

MFP18

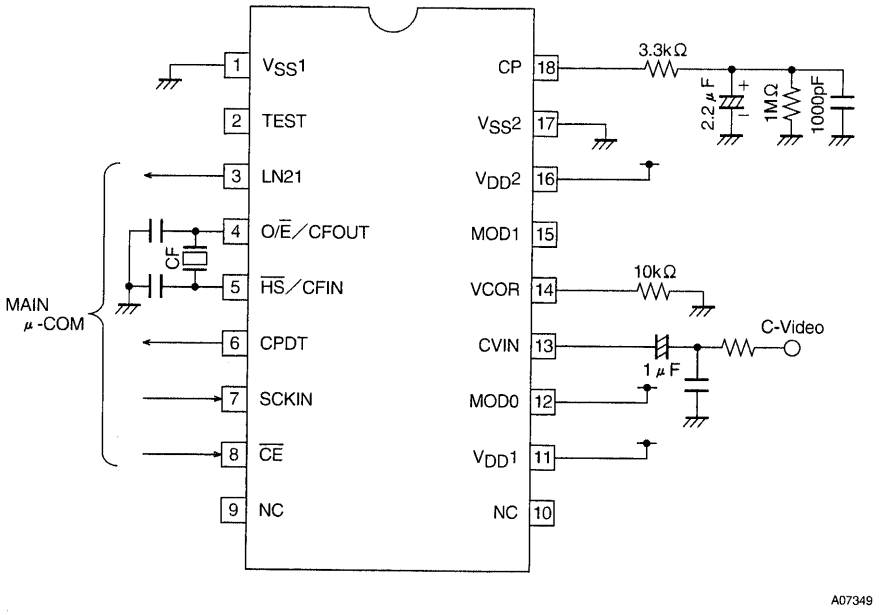



DIP16

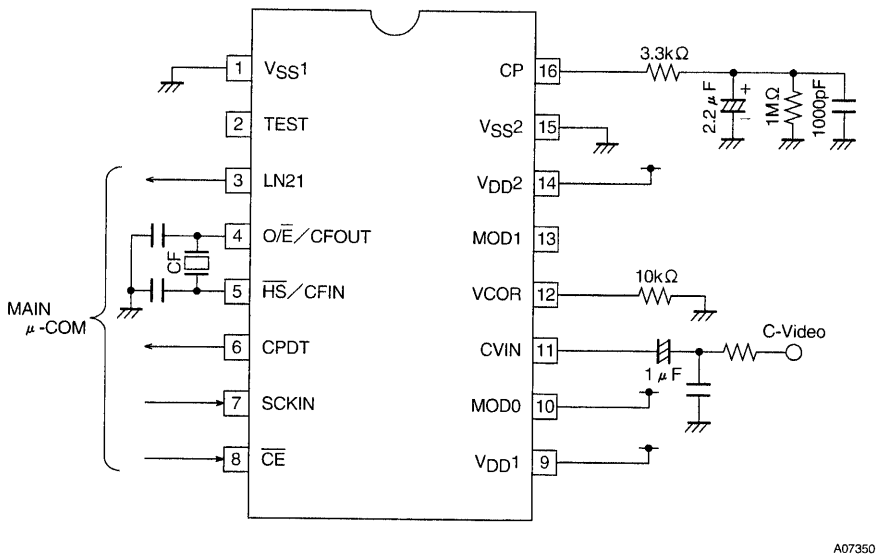


## Sample Application Circuits (mode 2)

MFP18

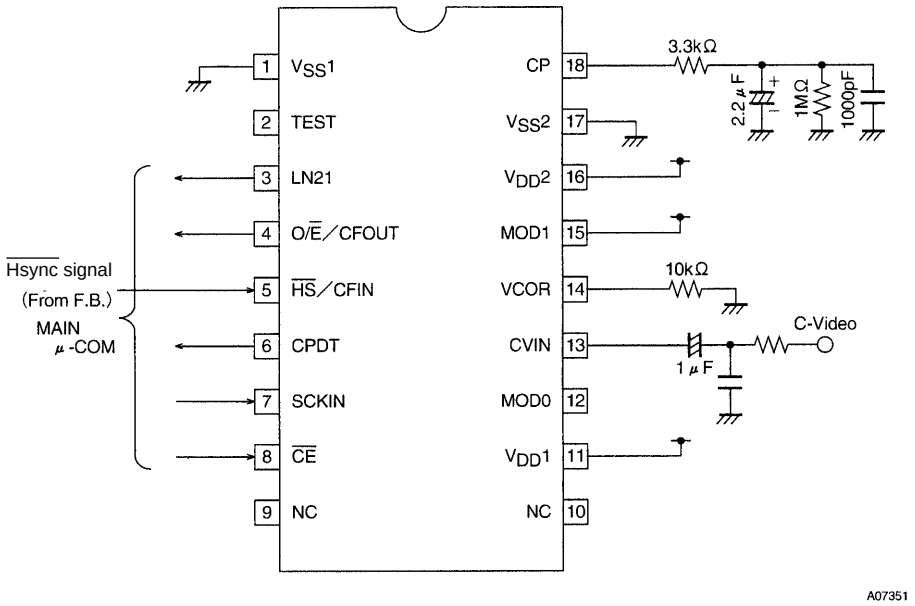



DIP16

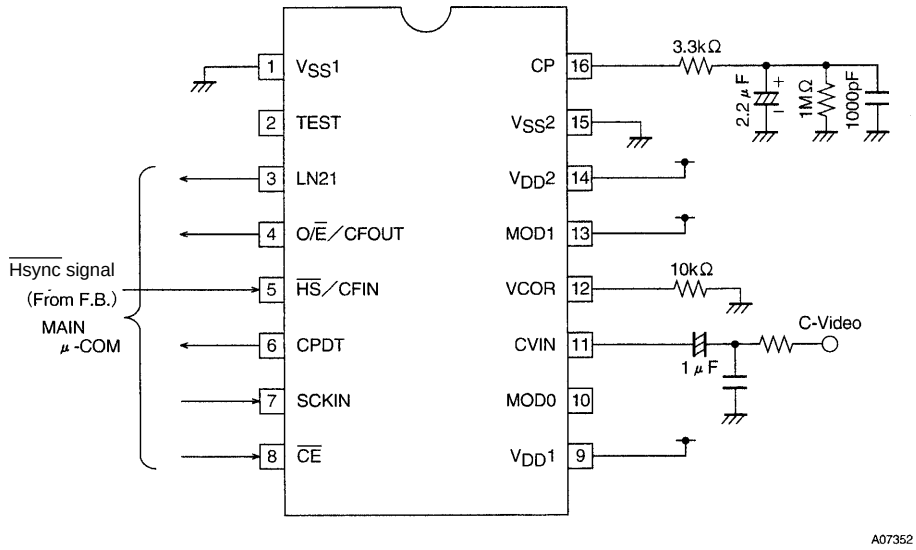


## Sample Application Circuits (mode 3)

MFP18

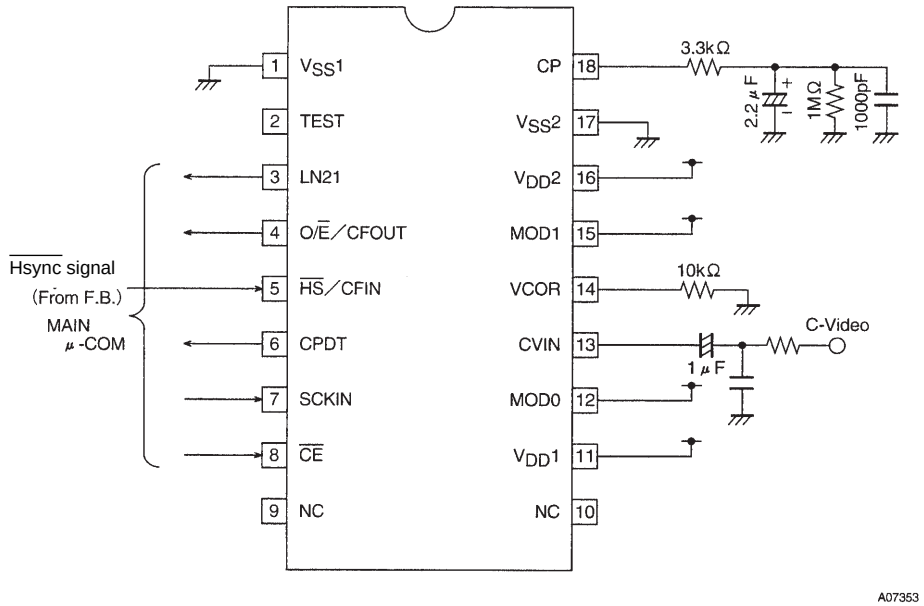



DIP16



## Sample Application Circuits (mode 4)

MFP18




DIP16