No.2522

LC7412,7413

CMOS LSI

VTR Servo Digital Controller

General Description

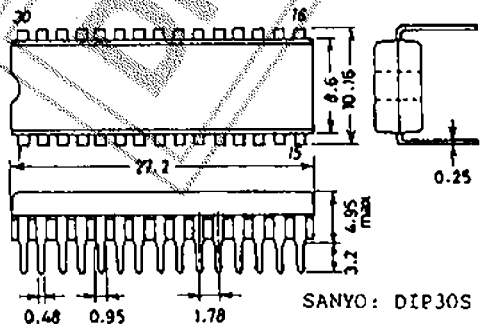
The LC7412,7413 are digital control CMOS LSIs for VTR servo circuit use. Since any servo characteristics can be achieved by coding the on-chip mask ROMs and externally addressing the ROMs, the LC7412,7413 can be applied to any multifunctional VTRs. The LC7412,7413, which contain the functions required for the servo circuit on single chips, can provide a servo system with a good cost performance.

Features

- Speed/phase control of drum unit (On-chip ROMs)
- Speed/phase control of capstan unit (On-chip ROMs)
- Generation of reference signal for phase control (On-chip ROM)
- Mode select by 4-bit parallel data
- Recording/playback control of control signal
- Automatic detection of tape speed during playback mode (SP/LP/EP)
- Division processing of control signal, capstan FG signal during special playback mode
- Processing of drum PG signal
- Pseudo V_D signal generating circuit
- Generation of switching signal for HiFi head
- Generation of 4-head control signal (LC7413)
- Fine/slow (Frame Advance) timing control (LC7413)
- Package DIP30S: LC7412
  DIP42S: LC7413

Case Outline 3047A-D30SIC
(unit:mm)

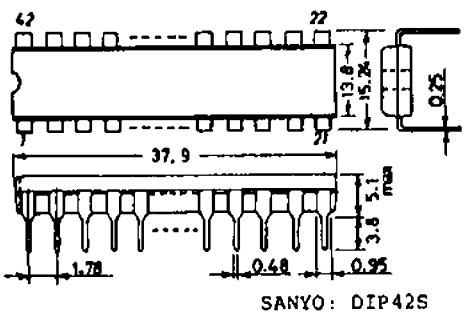
LC7412



SANYO: DIP30S

Case Outline 3025B-D42SIC
(unit:mm)

LC7413



SANYO: DIP42S

Specifications and information herein are subject to change without notice.

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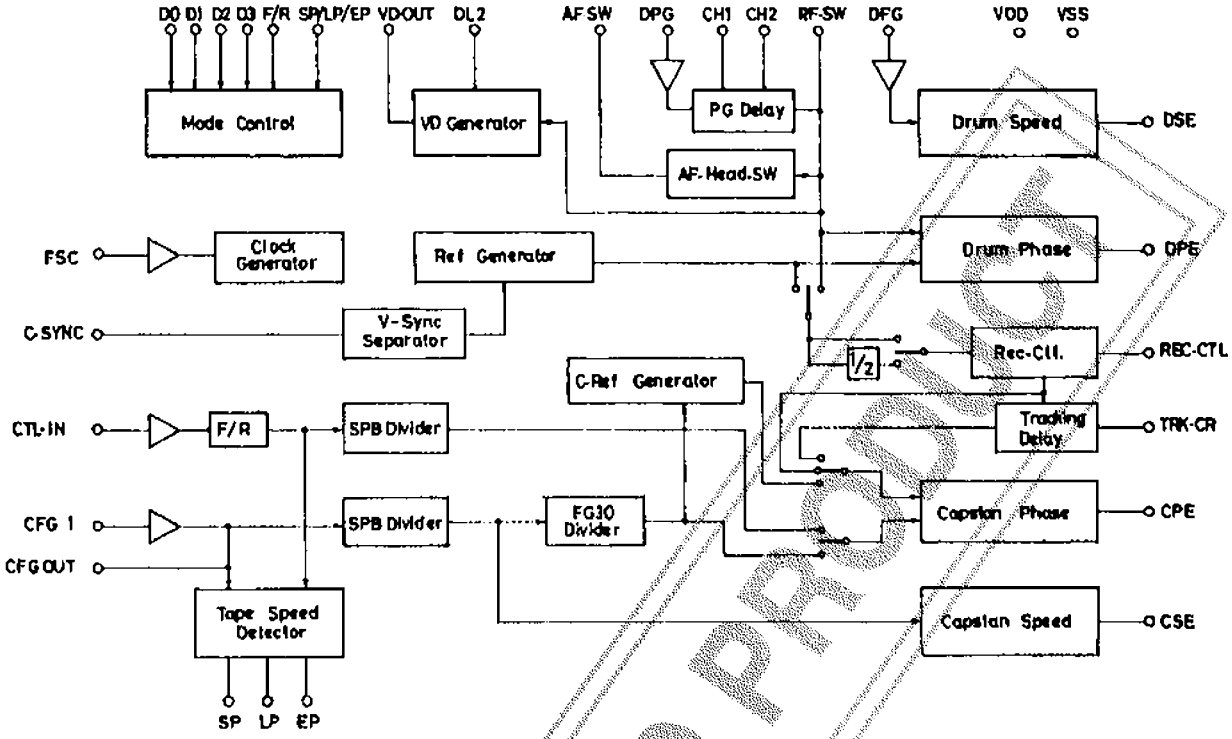
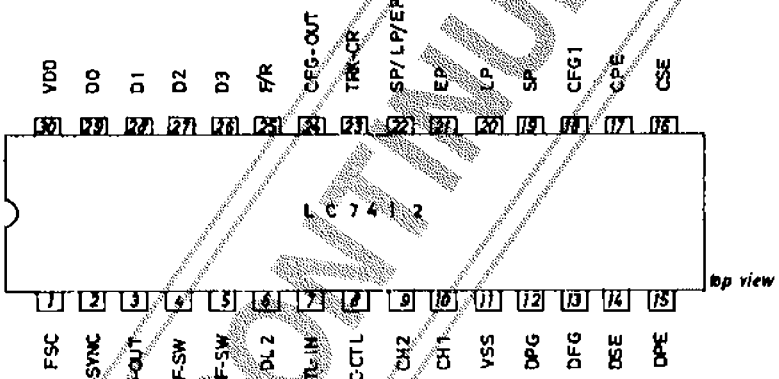
Equivalent Circuit Block Diagram LC7412

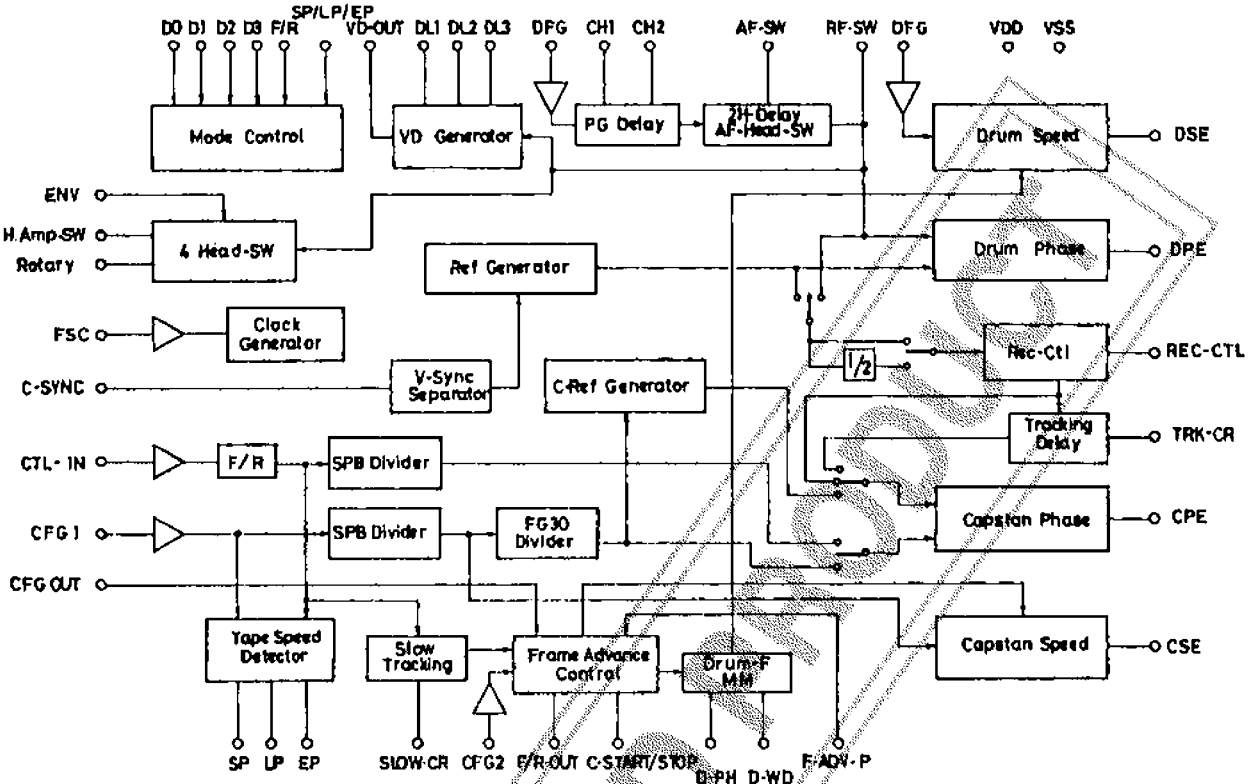


Pin Assignment LC7412



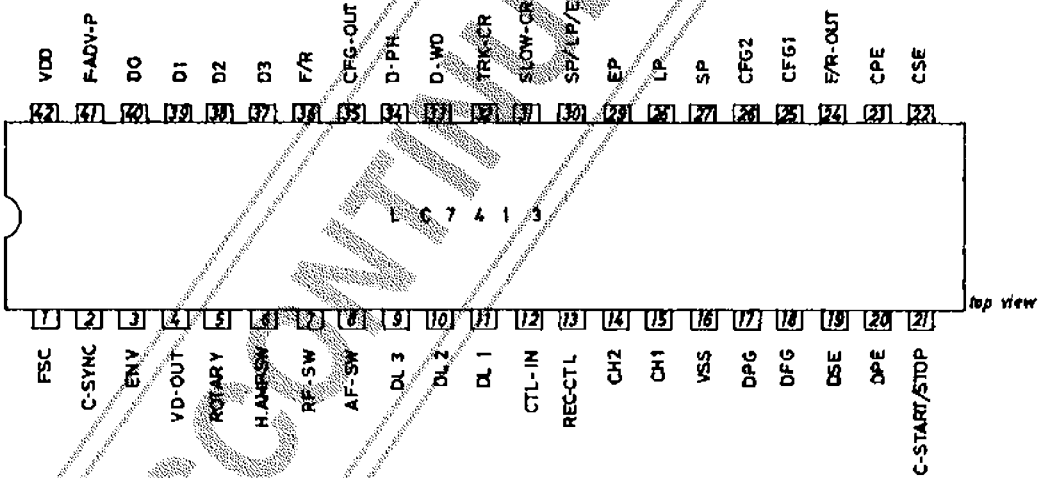
Equivalent Circuit Block Diagram

LC7413

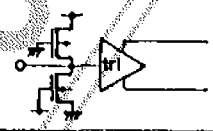
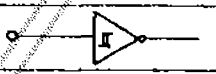
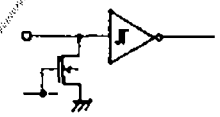
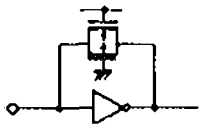
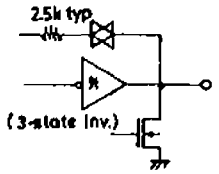
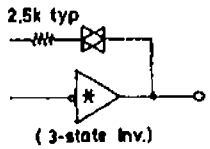


Pin Assignment

LC7413



Pin Description (*:LC7412)

Pin Name	Pin No.(*)	Functions	Input/Output Configuration
VDD VSS	42(30) 16(11)	LSI power supply VSS:0V VDD:4.5 to 5.5V	
D0,D1, D2,D3	40(29),39(28) 38(27),37(26)	Operation mode selection (16 modes) is made by 4-bit binary data. Latch function must be provided externally.	
F/R	36(25)	Forward/reverse selection. "H" level=Forward, "L" level=Reverse	
SP/LP/EP	30(22)	REC tape speed is specified. "H" level=SP, "M" level=LP, "L" level=EP	
C-SYNC	2(2)	Composite sync signal is input.	
F-ADV-P	41(-)	Frame advance pulse is input. Frame advance is made with every pulse.	
ENV	3(-)	Head select signal is input at 4-head special PB mode.	
Fsc	1(1)	Color subcarrier signal to be used for internal system clock of LSI is applied through capacitive coupling. Signal level of 0.3Vp-p or greater is required.	
CTL-IN	12(7)	Control signal is input through capacitive coupling.	
DPG	17(12)	Drum PG signal is input through capacitive coupling.	
DFG	18(13)	Drum FG signal is input through capacitive coupling.	
CFG1	25(18)	FG signal for capstan unit is input. Speed control, phase control, tape speed detection, and the like are performed.	
CFG2	26(-)	Second FG signal for capstan unit is input. Control is performed at frame advance slow mode.	
DSE	19(14)	Low-order 3 bits and high-order 5 to 8 bits of error output of drum unit speed control are output in the form of analog signal and PWM signal, respectively. This pin is brought to "L" level at drum stop mode.	
CSE	22(16)	Low-order 3 bits and high-order 5 to 8 bits of error output of capstan unit speed control are output in the form of analog signal and PWM signal, respectively. This pin is brought to "L" level at capstan stop mode.	
DPE	20(15)	Low-order 3 bits and high-order 5 to 8 bits of error output of drum unit phase control are output in the form of analog signal and PWM signal, respectively. Signal of duty 50% is output at the time of other than mode selection, stop mode, speed slope.	

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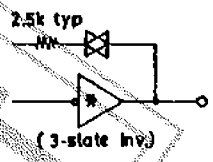
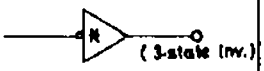
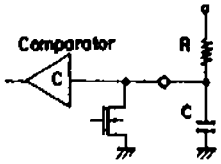
Pin Name	Pin No.(#)	Functions	Input/Output Configuration
CPE	23(17)	Low-order 3 bits and high-order 5 to 8 bits of error output of capstan unit phase control are output in the form of analog signal and PWM signal, respectively. Signal of duty 50% is output at the time of other than mode selection, stop mode, speed slope.	
RF-SW	7(4)	Drum head switching pulse output	
AF-SW	8(5)	Audio FM-use head switching pulse output.	
F/R-OUT	24(-)	Capstan motor forward/reverse control output. Signal is output according to motor start/stop at frame advance mode; and F/R pin input signal is output, as it is, at other than frame advance mode.	
SP	27(19)	REC time mode detect output. SP:"H"	
LP	28(20)	REC time mode detect output. LP:"H"	
EP	29(21)	REC time mode detect output. EP:"H"	
CFG-OUT	35(24)	CFG1 signal output pin. Division signal (1/1,1/2,1/4,1/8) of CFG1 signal is output.	
C-START /STOP	21(-)	Capstan motor start/stop signal is output at frame advance mode.	
ROTARY	5(6)	Head select signal is output at 4-head (3-head) mode.	
H AMP-S	6(-)		
VD-OUT	4(3)	Pseudo vertical sync signal is output at special REC mode. This pin is brought to "L" level at other than special REC mode.	
REC-CTL	13(8)	Control signal is output at REC mode. This pin is brought to high impedance state.	
DL1 DL2 DL3	9(-) 10(6) 11(-)	Pseudo V_D insert position adjust CR pin. DL1 --- Delay amount after RF-SW pulse fall DL2 --- Delay amount after RF-SW pulse rise DL3 --- Position correction at frame advance slow start mode	
CH1 CH2	15(10) 14(9)	DPG detector mounting position adjust CR pin	
TRK-CR	32(23)	Tracking CR pin	
SLOW-CR	31(-)	Slow tracking CR pin	
D-PH D-WD	34(-) 33(-)	CR pin for drum rotational speed fine timing adjust at frame advance mode	

Absolute Maximum Ratings at Ta=25°C

				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +7.0	V
Maximum Input Voltage	$V_I$max	Input pins	-0.3 to V_{DD}+0.3	V
Maximum Output Voltage	$V_O$max	Output pins	-0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax	Ta=-30 to +70°C	150	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

Allowable Operating Conditions at Ta=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Input "H"-Level Voltage	V_{IH1}	D0,D1,D2,D3	0.7V_{DD}		V_{DD}	V
	V_{IH2}	SP/LP/EP,F/R,C-SYNC, ENV,F-ADV-P	0.8V_{DD}		V_{DD}	V
Input "L"-Level Voltage	V_{IL1}	Pins for V_{IH1}	V_{SS}		0.3V_{DD}	V
	V_{IL2}	Pins for V_{IH2}	V_{SS}		0.2V_{DD}	V
Input "M"-Level Voltage	V_{IM}	SP/LP/EP	0.4V_{DD}		0.6V_{DD}	V
Input Amplitude	V_{IN1}	Sine wave capacitive coupling,FSC	0.3			Vp-p
	V_{IN2}	Capacitive coupling, DFG,CFG1,CFG2,DPG,CTL-IN	1.5			Vp-p
Input Pulse Width	t_{WI}	DPG,CTL-IN	50			us
Operating Frequency	f_{IN1}	Sine wave capacitive coupling,FSC	1.0		5.5	MHz
	f_{IN2}	DFG,CFG1,CFG2	0.1		30	kHz
	f_{IN3}	DPG,CTL-IN	10		1000	Hz
	f_{IN4}	$t_{WIH} \geq$ 1us,C-SYNC	5		50	kHz
Comparator Characteristics						
Comparison Level	V_{TH}	TRK-CR,DL1,DL2,DL3, CH1,CH2,D-PH,D-WD, SLOW-CR	-10% 0.6V_{DD}		+10%	V
	V_{TL}	TRK-CR,DL1,DL2,DL3, CH1,CH2,D-PH,D-WD, SLOW-CR	0.1V_{DD}			V
Delay Time	tdel	R=100kohms,C=0.01uF TRK-CR,DL1,DL2,DL3, CH1,CH2,D-PH,D-WD, SLOW-CR	0.78	0.92	1.08	ms

Electrical Characteristics at Ta=25°C, V_{DD}=5V±10%, V_{SS}=0V

				min	typ	max	unit
Input "H"-Level Current	I_{IH1}	V_{IN}=V_{DD}	D0,D1,D2,D3,F/R,C-SYNC			1.0	uA
	I_{IH2}	V_{IN}=V_{DD}	SP/LP/EP,F-ADV-P,ENV	5	10	20	uA
Input "L"-Level Current	I_{IL1}	V_{IN}=V_{SS}	D0,D1,D2,D3,F/R, C-SYNC,ENV,F-ADV-P	-1.0			uA
	I_{IL2}	V_{IN}=V_{SS}	SP/LP/EP	-20	-10	-5	uA
Input Floating Voltage	V_{IF1}	Input pins open,ENV,F-ADV-P		V_{SS}		V_{IL2} -0.5	V
	V_{IF2}	Input pins open,SP/LP/EP		0.45 xV_{DD}	0.5 xV_{DD}	0.55 xV_{DD}	V
Output "H"-Level Voltage	V_{OH1}	I_{OL}=0.3mA,SP,LP,EP,CFG-OUT, DSE,DPE,CSE,CPE,V_D-OUT, H AMP-SW,ROTARY,F/R-OUT,RF-SW, AF-SW,C-START/STOP		V_{DD} -0.3			V
	V_{OH2}	I_{OL}=5mA,REC-CTL		V_{DD}-1.0			V

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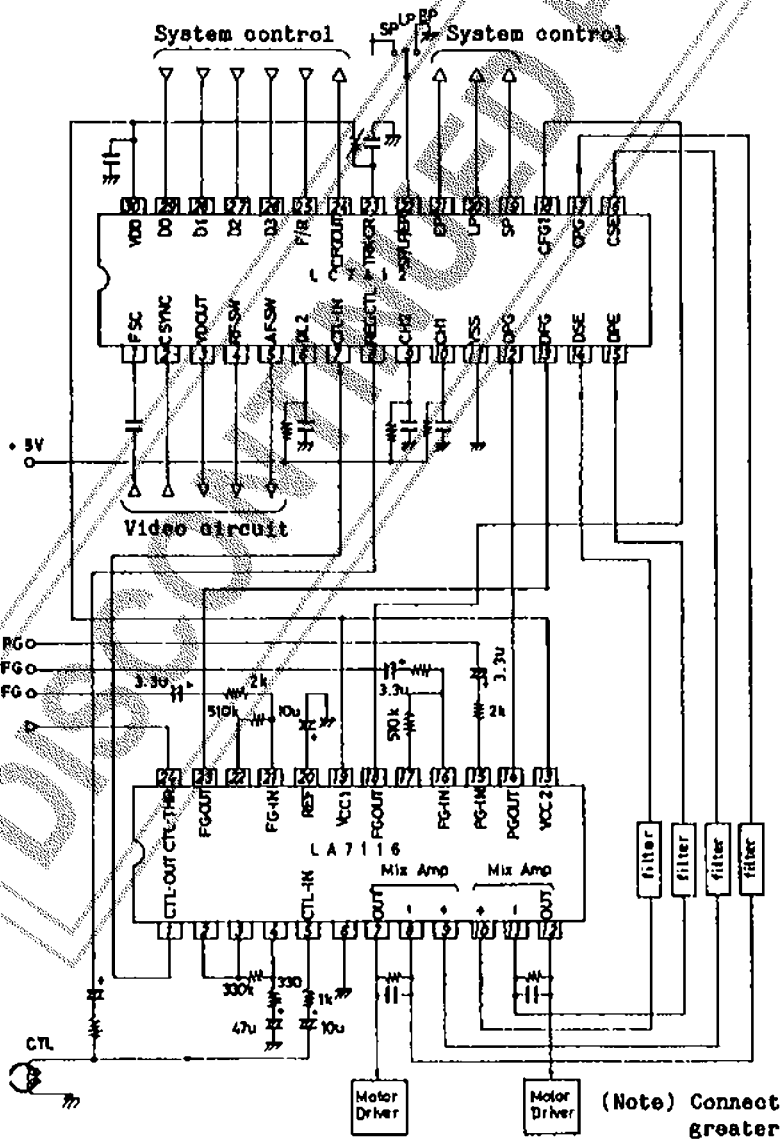
				min	typ	max	unit
Output "L"-Level Voltage	V_{OL1}	I_{OL}=0.3mA,pins for V_{OH1}, TRK-CR,DL1,DL2,DL3,CH1,CH2, D-PH,D-WD,SLOW-CR				0.3	V
	V_{OL2}	I_{OL}=5mA,REC-CTL				1.0	V
	V_{OL3}	I_{OL}=0.3mA,open drain tr. of DSE,CSE				0.6	V
DA Characteristics							
Bit Error	ΔV_{LSB}			-1/2LSB		+1/2LSB	V
Output Impedance	zo	R_L=100kohms		-30%	3.0	+30%	kohm
R-2R Ladder Composite Resistance	R_{OLDR}		DSE,DPE		2.5		kohm
			CSE,CPE				
DA Output Analog Switch ON-State Resistance	R_{onSW}	R_L=100kohms	(1LSB=1/8V_{DD})		0.5		kohm
Feedback Resistance	Rf	Fsc			0.7		Mohm
Output OFF-State Leakage Current	Ioff1	DSE,DPE,CSE,CPE		-2.0		2.0	uA
	Ioff2	REC-CTL		-1.0		1.0	uA
Input Sensitivity	V_{MIN}	Sine wave capacitive coupling,DFG,CFG1,CFG2,DPG,CTL-IN		0.5	1.0	1.5	Vp-p
Current Dissipation	I_{DD}	fsc=4.43MHz(0.3Vp-p) input				10.0	mA

Sample Application Circuit: LA7116 + LC7412



(Note) Connect a capacitor of 0.1uF or greater to the power line to prevent latch-up.