# LC05711ARA

# Battery Protection IC, Integrated Power MOSFET, 1-Cell Lithium-Ion Battery

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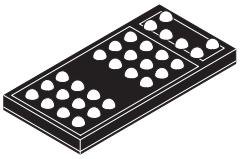


ECP30 (1.97×4.01, 0.4Pitch)

**GENERIC MARKING DIAGRAM**


A = Assembly Location
YY = Year
WW = Work Week

## Overview

The LC05711ARA is a protection IC for 1-cell lithium-ion secondary batteries with integrated power MOS FET. Also it integrates highly accurate detection circuits and detection delay circuits to prevent batteries from over-charging, over-discharging, over-current discharging and over-current charging.
A battery protection system can be made by only LC05711ARA and few external parts.

## Features

- Charge-and-discharge power MOSFET are integrated at Ta = 25°C, VCC = 4.0V
  ON resistance (total of charge and discharge ) 4.8mΩ (typ)
- Highly accurate detection voltage/current at Ta = 25°C, VCC = 3.7V
  Over-charge detection ±25mV
  Over-discharge detection ±50mV
  Charge over-current detection ±0.7A
  Discharge over-current detection ±0.7A
- Delay time for detection and release (fixed internally)
- Discharge/Charge over-current detection is compensated for temperature dependency of power FET
- 0V battery charging : “Permission”
- Auto wake-up function battery charging : “Permission”

## Typical Applications

- Smart phone
- Tablet
- Wearable device

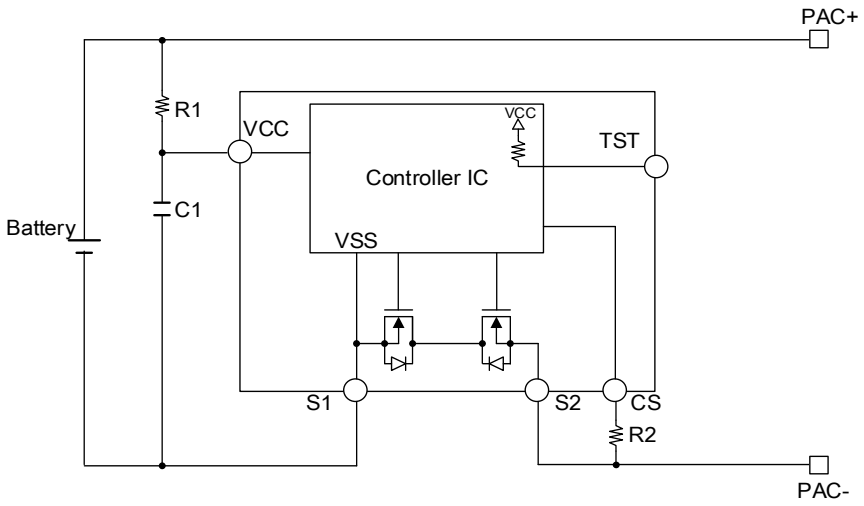
# Specifications

## Absolute Maximum Ratings at Ta = 25°C (Notes 1, 2, 3, 4, 6)

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | VCC | Between PAC+ and VCC : R1=680Ω | −0.3 to 12.0 | V |
| S1 - S2 voltage | VS1-S2 | | 20.0 | V |
| CS terminal Input voltage | CS | | VCC−20.0 to VCC+0.3 | V |
| TST terminal input voltage | TST | | −0.3 to 7 | V |
| Storage temperature | Tstg | | −55 to +125 | °C |
| Operating ambient temperature | Topr | | −40 to +100 | °C |
| Allowable power dissipation | Pd | (Note 5) | 800 | mW |
| Junction temperature | Tj | | 125 | °C |

1. Stresses exceeding those listed in the Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Absolute maximum ratings represent the values which cannot be exceeded at any given time
3. If you intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it is used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for confirmation
4. This device is made for power applications.
5. JESD 51−3 (1S)
6. Please execute appropriate test and take safety measures on your board.

## Example of Application Circuit




| Components | Recommended value | MAX | unit | Description |
|---|---|---|---|---|
| R1 | 680 | 1k | Ω | |
| R2 | 1k | 2k | Ω | |
| C1 | 1.0μ | − | F | |

* We don't guarantee the characteristics of the circuit shown above.

## Electrical Characteristics (Note 4, 6, 7, 8)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | | | | | | | |
| Over-charge detection voltage | Vov | R1=680Ω | Ta=25°C | Vov_set -25 | Vov_set | Vov_set +25 | mV |
| | | | Ta=−30 to 70°C | Vov_set -30 | Vov_set | Vov_set +30 | |
| Over-charge release voltage | Vovr | R1=680Ω | Ta=25°C | Vovr_set -40 | Vovr_set | Vovr_set +40 | mV |
| | | | Ta=−30 to 70°C | Vovr_set -70 | Vovr_set | Vovr_set +70 | |
| Over-discharge detection voltage | Vuv | R1=680Ω | Ta=25°C | Vuv_set -50 | Vuv_set | Vuv_set +50 | mV |
| | | | Ta=−30 to 70°C | Vuv_set -80 | Vuv_set | Vuv_set +80 | |
| Over-discharge release voltage | Vuvr | R1=680Ω CS=0V | Ta=25°C | Vuvr_set -100 | Vuvr_set | Vuvr_set +100 | mV |
| | | | Ta=−30 to 70°C | Vuvr_set -120 | Vuvr_set | Vuvr_set +120 | |
| Over-discharge release voltage2 | Vuvr2 | R1=680Ω CS=Open | Ta=25°C | Vuvr2_set -100 | Vuvr2_set | Vuvr2_set +100 | mV |
| | | | Ta=−30 to 70°C | Vuvr2_set -120 | Vuvr2_set | Vuvr2_set +120 | |
| Discharge over-current detection current | Ioc | R2=1kΩ | Ta=25°C VCC=3.7V | Ioc_set -0.7 | Ioc_set | Ioc_set +0.7 | A |
| | | | Ta=−30 to 70°C VCC=3.7V | Ioc_set -1.2 | Ioc_set | Ioc_set +1.2 | |
| Discharge over-current detection currnt2 (Short circuit) | Ioc2 | R2=1kΩ | Ta=25°C VCC=3.7V | Ioc2_set*0.8 | Ioc2_set | Ioc2_set*1.2 | A |
| | | | Ta=−30 to 70°C VCC=3.7V | Ioc2_set*0.6 | Ioc2_set | Ioc2_set*1.8 | |
| Charge over-current detection current | Ioch | R2=1kΩ | Ta=25°C VCC=3.7V | Ioch_set -0.7 | Ioch_set | Ioch_set +0.7 | A |
| | | | Ta=−30 to 70°C VCC=3.7V | Ioch_set -1.2 | Ioch_set | Ioch_set +1.2 | |
| Input voltage | | | | | | | |
| Operating Voltage for 0V charging | Vchg | VCC-CS VCC-S1=0V | Ta=25°C | | | 1.4 | V |
| Current consumption | | | | | | | |
| Operating current | Icc | At normal state | Ta=25°C VCC=3.7V | | 3 | 6 | μA |
| Standby current | Istb | At standby state | Ta=25°C VCC=2.0V | | | 0.95 | μA |
| Resistance | | | | | | | |
| ON resistance 1 of integrated power MOS FET | Ron1 | VCC=3.1V I=±2.0A | Ta=25°C | 4.4 | 5.4 | 6.9 | mΩ |
| ON resistance 2 of integrated power MOS FET | Ron2 | VCC=3.8V I=±2.0A | Ta=25°C | 4 | 4.9 | 5.8 | mΩ |
| ON resistance 3 of integrated power MOS FET | Ron3 | VCC=4.0V I=±2.0A | Ta=25°C | 3.9 | 4.8 | 5.7 | mΩ |
| ON resistance 4 of integrated power MOS FET | Ron4 | VCC=4.5V I=±2.0A | Ta=25°C | 3.8 | 4.7 | 5.6 | mΩ |
| Internal resistance (VCC-CS) | Rcsu | VCC=Vuv_set CS=0V | Ta=25°C | | 300 | | kΩ |
| Internal resistance (VSS-CS) | Rcsd | VCC=3.7V CS=0.1V | Ta=25°C | | 10 | | kΩ |
| Forward Source to Source Voltage | Vf(s-s) | VCC=2.0V Is=0.25A | Ta=25°C | | 0.67 | 1.06 | V |

Continued on next page.

Continued from preceding page.

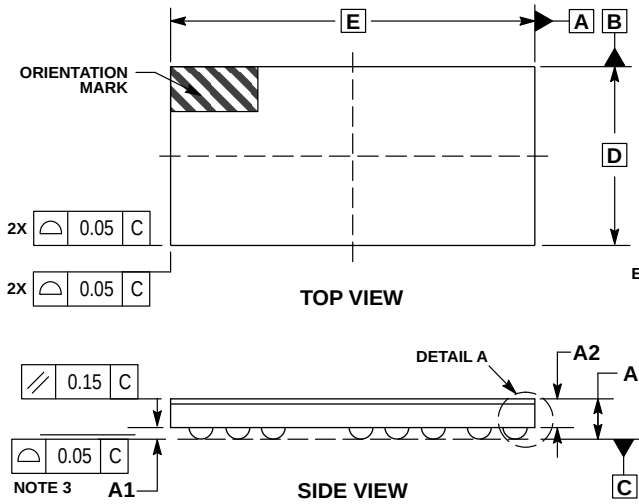
| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection and Release delay time | | | | | | | |
| Over-charge detection delay time | Tov | | Ta=25°C | 0.8 | 1 | 1.2 | s |
| | | | Ta=−30 to 70°C | 0.6 | 1 | 1.5 | |
| Over-charge release delay time | Tovr | | Ta=25°C | 12.8 | 16 | 19.2 | ms |
| | | | Ta=−30 to 70°C | 9.6 | 16 | 24 | |
| Over-discharge detection delay time | Tuv | | Ta=25°C | 14 | 20 | 26 | ms |
| | | | Ta=−30 to 70°C | 12 | 20 | 30 | |
| Over-discharge release delay time | Tuvr | | Ta=25°C | 0.9 | 1.1 | 1.3 | ms |
| | | | Ta=−30 to 70°C | 0.6 | 1.1 | 1.5 | |
| Discharge over-current detection delay time 1 | Toc1 | VCC=3.7V | Ta=25°C | 9.6 | 12 | 14.4 | ms |
| | | | Ta=−30 to 70°C | 7.2 | 12 | 18 | |
| Discharge over-current release delay time 1 | Tocr1 | VCC=3.7V | Ta=25°C | 3.2 | 4 | 4.8 | ms |
| | | | Ta=−30 to 70°C | 2.4 | 4 | 6 | |
| Discharge over-current detection delay time 2 (Short circuit) | Toc2 | VCC=3.7V | Ta=25°C | 230 | 300 | 420 | μs |
| | | | Ta=−30 to 70°C | 200 | 300 | 450 | |
| Charge Over-current detection delay time | Toch | VCC=3.7V | Ta=25°C | 12.8 | 16 | 19.2 | ms |
| | | | Ta=−30 to 90°C | 9.6 | 16 | 24 | |
| Charge Over-current release delay time | Tochr | VCC=3.7V | Ta=25°C | 3.2 | 4 | 4.8 | ms |
| | | | Ta=−30 to 90°C | 2.4 | 4 | 6 | |

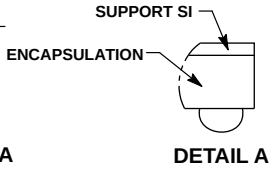
7. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
8. The specification in this parameter and all specification at high and low temperature are guaranteed by design.

## Package Dimensions

unit : mm

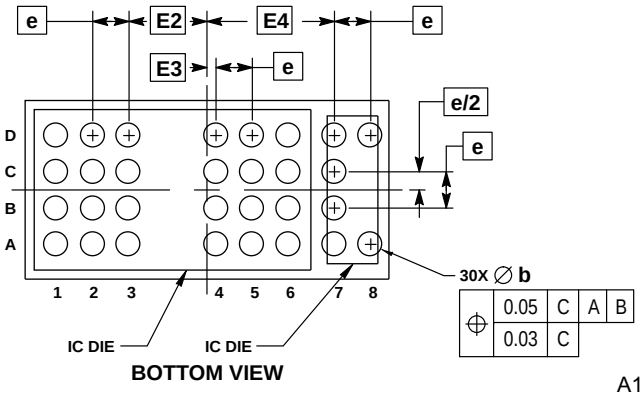
**ECP30, 1.97x4.01**
CASE 971BC
ISSUE A



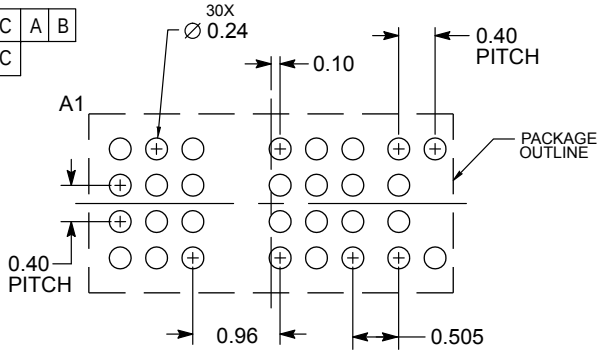




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER PARALLEL TO DATUM C.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.545 | 0.625 |
| A1 | 0.165 | 0.205 |
| A2 | 0.380 | 0.420 |
| b | 0.245 | 0.285 |
| D | 1.970 BSC | |
| E | 4.010 BSC | |
| E2 | 0.860 BSC | |
| E3 | 0.100 BSC | |
| E4 | 1.405 BSC | |
| e | 0.400 BSC | |



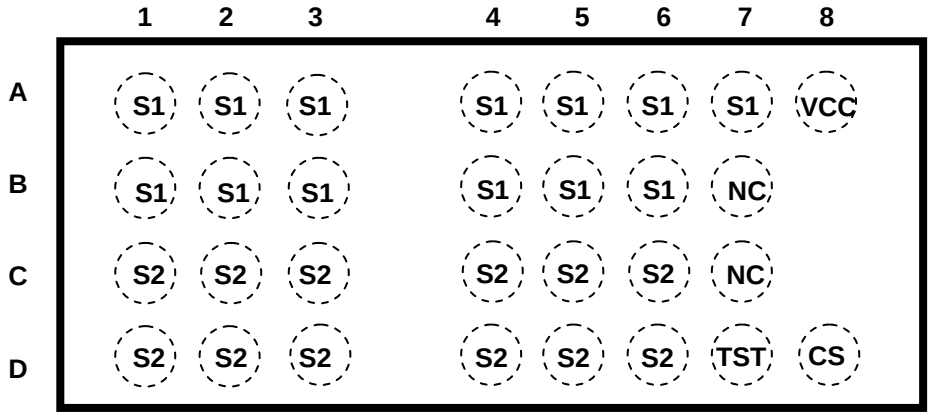

**RECOMMENDED SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

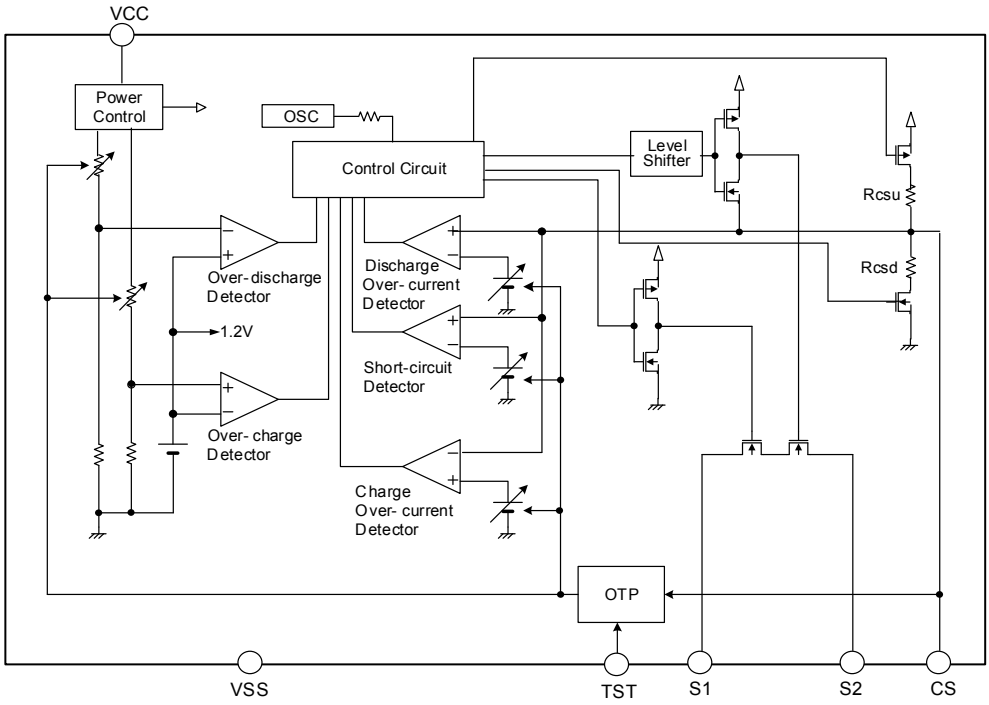
## Pin Functions



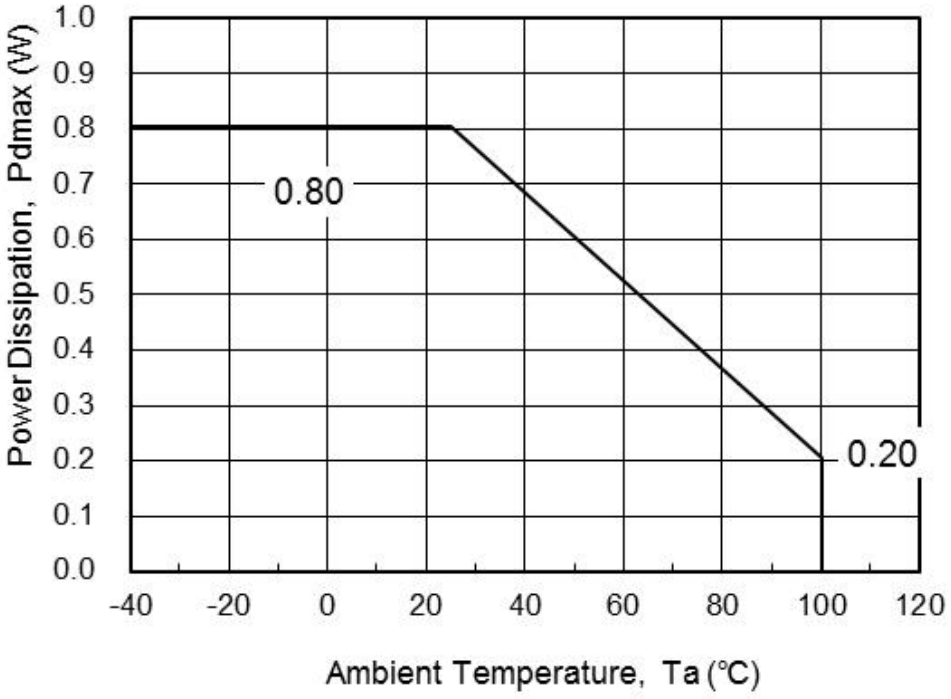

TOP VIEW

| Pin No. | Symbol | Pin Function | Description |
|---|---|---|---|
| A1-7<br>B1-6 | S1 | Source 1 | Negative power input |
| A8 | VCC | VCC terminal | |
| C1-6<br>D1-6 | S2 | Source 2 | |
| D7 | TST | Test terminal | Connected to VCC with 100kΩ |
| D8 | CS | Charger minus voltage input terminal | |
| B7,C7 | NC | Non connection | |

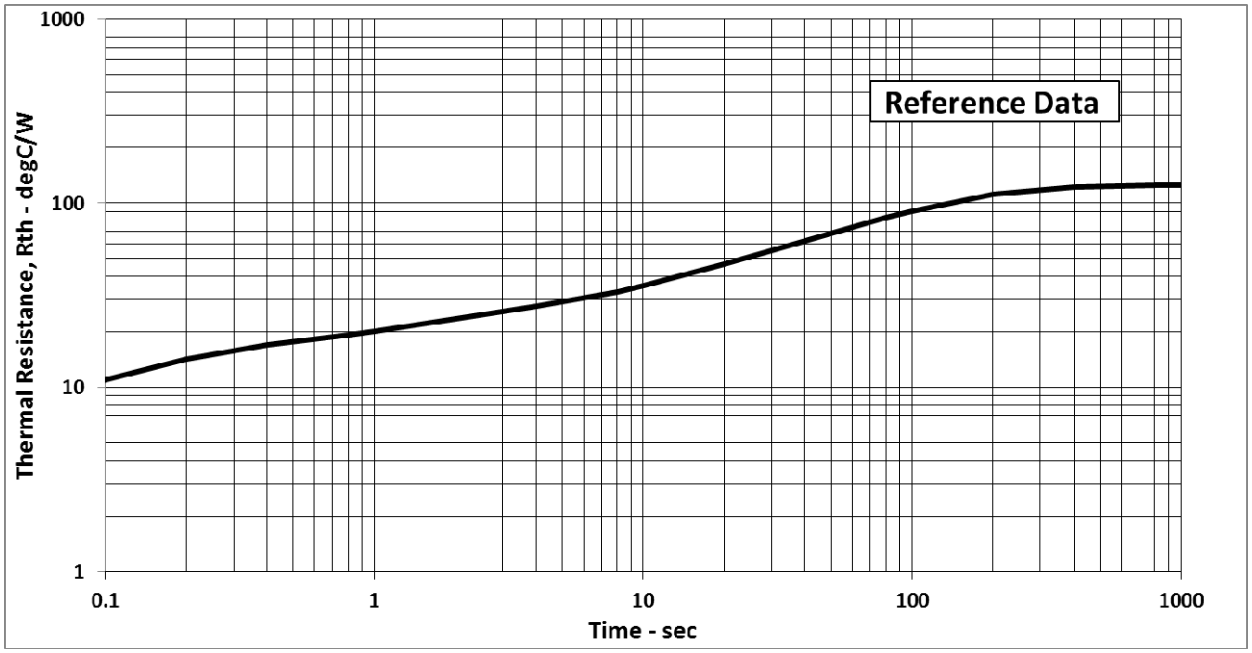
## Block Diagram



## Pdmax vs Ta




## Thermal Resistance vs Time



## Description of operation

(1)Normal mode

•LC05711ARA controls charging and discharging by detecting cell voltage (VCC) and controls S2-S1 current. In case that cell voltage is between over-discharge detection voltage (Vuv) and over-charge detection voltage (Vov), and S2-S1 current is between charge over-current detection current (Ioch) and discharge over-current detection current (Ioc), internal power MOS FETs as CHG_SW, DCHG_SW are both turned ON.
This is the normal mode, and it is possible to be charged and discharged.

(2)Over-charging mode

•Internal poer MOS FETCHG_SW turns off if cell voltage becomes greater than or equal to over-charge detection voltage (Vov) over the delay time of over-charging (Tov).
This is the over-charging detection mode.

•The recovery from over-charging will be made after the following two conditions are satisfied.

1. Charger is removed from IC.
2. Cell voltage decreases under over-charge release voltage (Vovr) over the delay time of over-charging releasing (Tovr) due to discharging through a load.

Consequently, internal power MOS FET as CHG_SW will be turned on and normal mode will be resumed.

•In over-charging mode, discharging over-current detection is made only when CS pin increases more than discharging over-current detection current 2(Ioc2), because discharge current flows through parasitic diode of CHG_SW FET.
If CS pin voltage increases more than discharging over-current detection current 2 (Ioc2) over the delay time of discharging over-current 2 (Toc2), discharging will be shut off, because internal power FETs as DCHG_SW is turned off. (short-circuit detection mode)
After detecting short-circuit, CS pin will be pulled down to Vss by internal resistor Rcsd.

The recovery from short circuit detection in over-charging mode will be made after the following two conditions are satisfied.

1. Load is removed from IC.
2. CS pin voltage becomes less than or equal to discharging over-current detection current 2 (Ioc2) due to CS pin pulled down through Rcsd.

Consequently, internal power MOS FET as DCHG_SW will be turned on, and over-charging detection mode will be resumed.

(3)Over-discharging mode with Auto Wake Up function

•If cell voltage drops lower than over-discharge detection voltage (Vuv) over the delay time of over-discharging (Tuv), discharging will be shut off, internal power FETs as DCHG_SW is turned off.
This is the over-discharging mode.
After detecting over-discharging, CS pin will be pulled up to Vcc by an internal resistor Rcsu and the bias of internal circuits will be shut off. (Shut-down mode)
In shut-down mode, operating current is suppressed under 0.1uA (max).

•The recovery from stand-by mode will be made by internal circuits biased after the following two conditions are satisfied.

1. Charger is connected.
2. VCC level rise more than Over-discharge release voltage2 (Vuvr2) without charger.(Auto wake-up function)

•By continuing to be charged, if cell voltage increases more than over-discharge detection voltage (Vuvr) over the delay time of over-discharging (Tuvr), internal power MOS FETs as DCHG_SW is turned on and normal mode will be resumed.

•In over-discharge detection mode, charging over-current detection does not operate.
By continuing to be charged, charging over-current detection starts to operate after cell voltage goes up more than over-discharge release voltage (Vuvr).

(4)Discharging over-current detection mode 1

•Internal power MOS FET as DCHG_SW will be turned off and discharging current will be shut off if CS pin voltage becomes greater than or equal to discharging over-current detection current (Ioc) over the delay time of discharging over-current (Toc1).
This is the discharging over-current detection mode 1.
In discharging over-current detection mode 1, CS pin will be pulled down to Vss with internal resistor Rcsd.

•The recovery from discharging over-current detection mode will be made after the following two conditions are satisfied.

1. Load is removed from IC.
2. CS pin voltage becomes less than or equal to discharging over-current release current (Iocr) over the delay time of discharging over-current release (Tocr1) due to CS pin pulled down

through Rcsd.

Consequently, internal power MOS FET as DCHG_SW will be turned on, and normal mode will be resumed.

(5)Discharging over-current detection mode 2 (short circuit detection)

- Internal power MOS FET as DCHG_SW will be turned off and discharging current will be shut off if CS pin voltage becomes greater than or equal to discharging over-current detection current2 (Ioc2) over the delay time of discharging over-current 2 (Toc2).
  This is the short circuit detection mode.

- In short circuit detection mode, CS pin will be pulled down to Vss by internal resistor Rcsd.
  The recovery from short circuit detection mode will be made after the following two conditions are satisfied.
  a. Load is removed from IC.
  b. CS pin voltage becomes less than or equal to discharging over-current release current (Iocr) over the delay time of discharging over-current release (Tocr1) due to CS pin pulled down through Rcsd.

Consequently, internal power MOS FET as DCHG_SW will be turned on, and normal mode will be resumed.

(6)Charging over-current detection mode

- Internal power MOS FET as CHG_SW will be turned off and charging current will be shut off if CS pin voltage becomes less than or equal to charging over-current detection current (Ioch) over the delay time of charging over-current (Toch).
  This is the charging over-current detection mode.

- The recoveries from charging over-current detection mode will be made after the following two conditions are satisfied.
  1. Charger is removed from IC and CS pin will increase by load connection.
  2. CS pin voltage becomes greater than or equal to charging over-current release current (Iochr) over the delay time of charging over-current release (Tocrh).

Consequently, internal power MOS FET as CHG_SW will be turned on, and normal mode will be resumed.

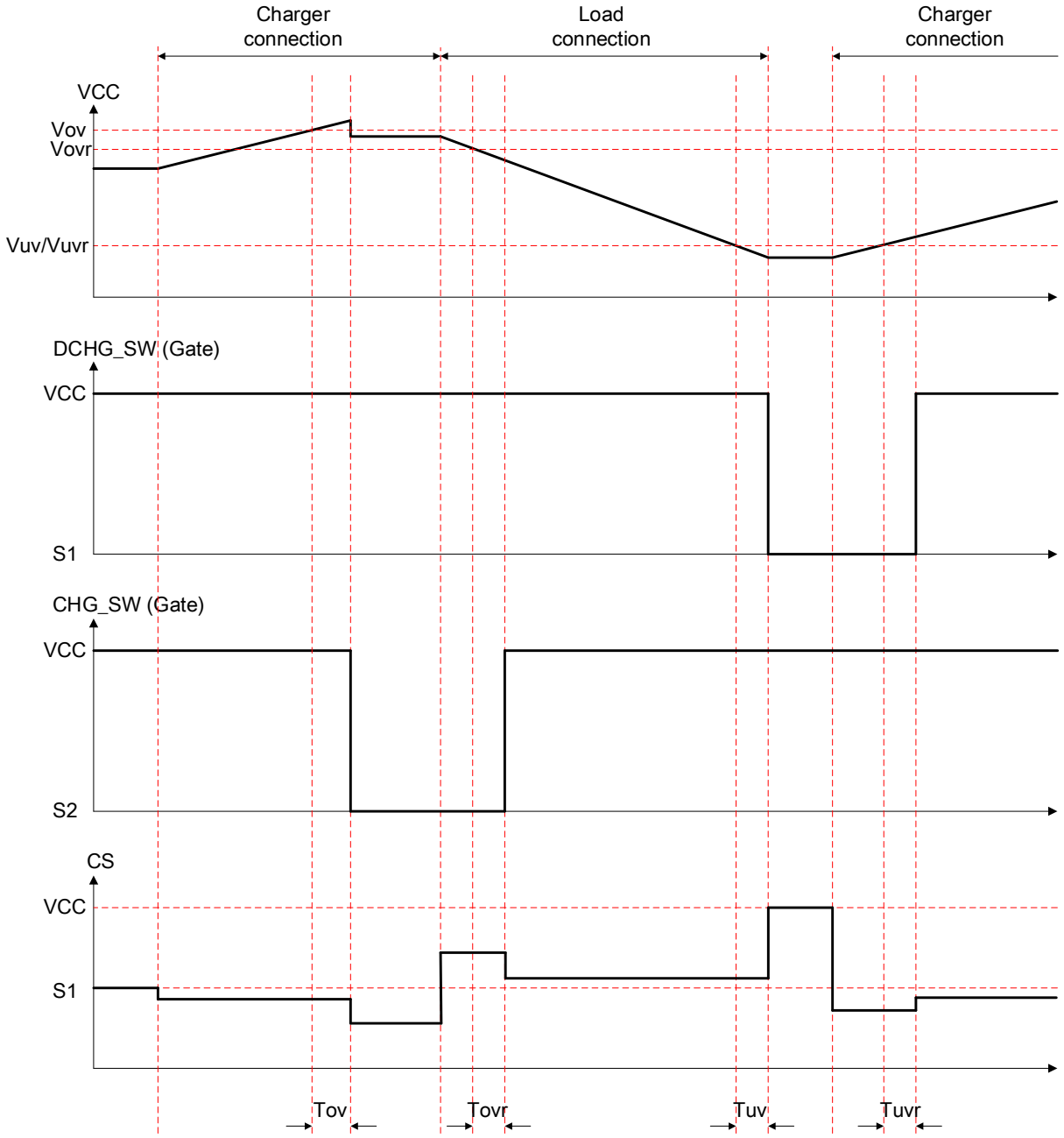
*Internal current flows out through CS and S2 terminals.
After charger is removed, it flows through parasitic diode of CHG_SW FET.
Therefore, CS pin voltage will go up more than charging over-current release current (Iochr).
So CS pin voltage is not an indispensable condition for recovery from charging over-current detection.

(7) Available Voltage for 0V charging

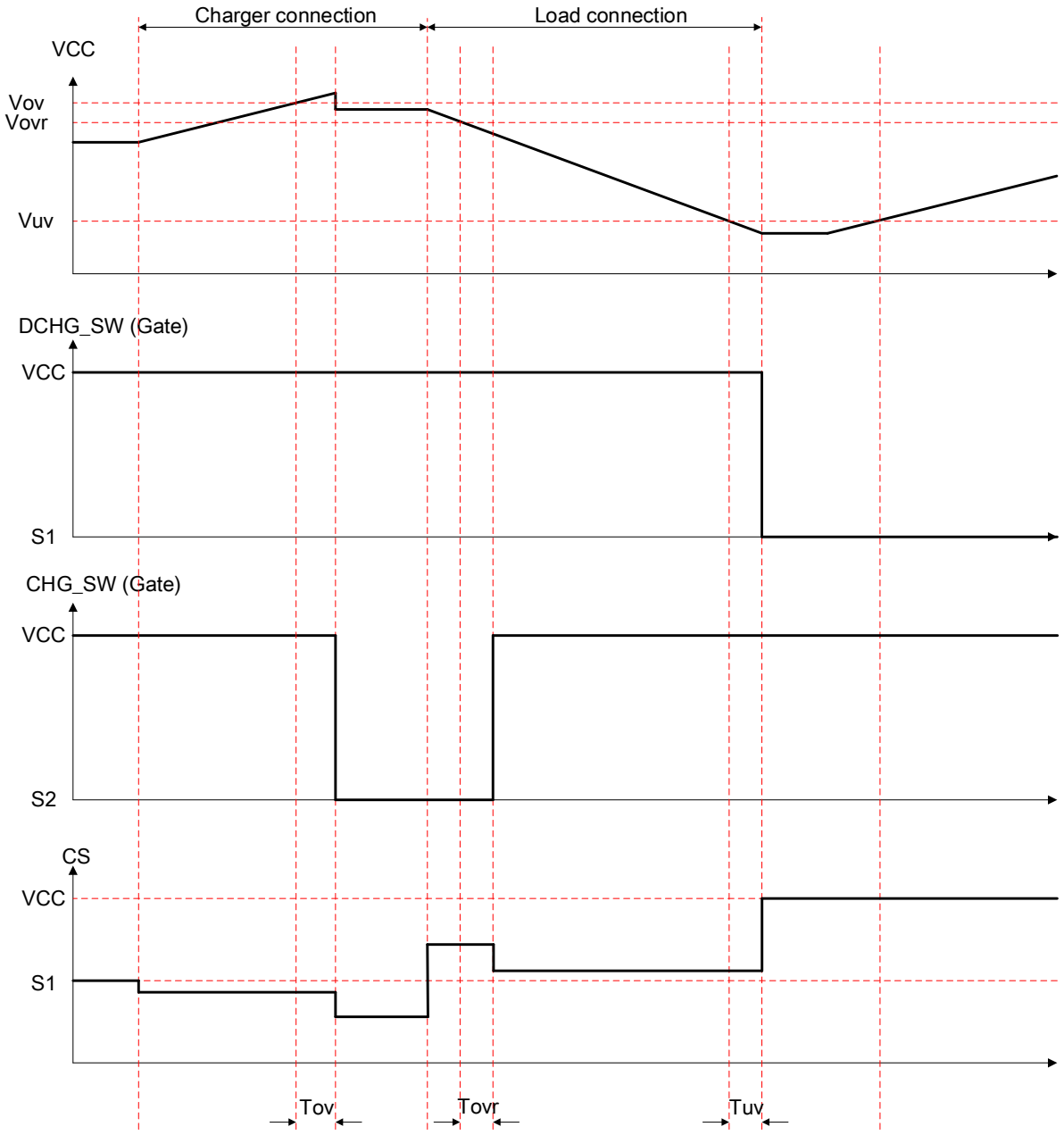
It is the function that the voltage of a connected battery can charge from the state that became 0V by self-discharge. The 0V battery charge start battery charger voltage (Vchg), it fix a gate of the charge system order FET to the VDD terminal voltage when it connect a battery charger of the above-mentioned voltage to PAC+ terminal between PAC- terminals.
Gate-source voltage of the charge control FET becomes equal to the turn-on voltage or more due to the charger voltage, the charging control FET To start charging row is turned on.
Discharge control FET is off at this time, the charge current flows through the internal parasitic diode in the discharging control FET. It is the normal state battery voltage becomes the overdischarge release voltage (Vuvr) or more.

## Timing Chart

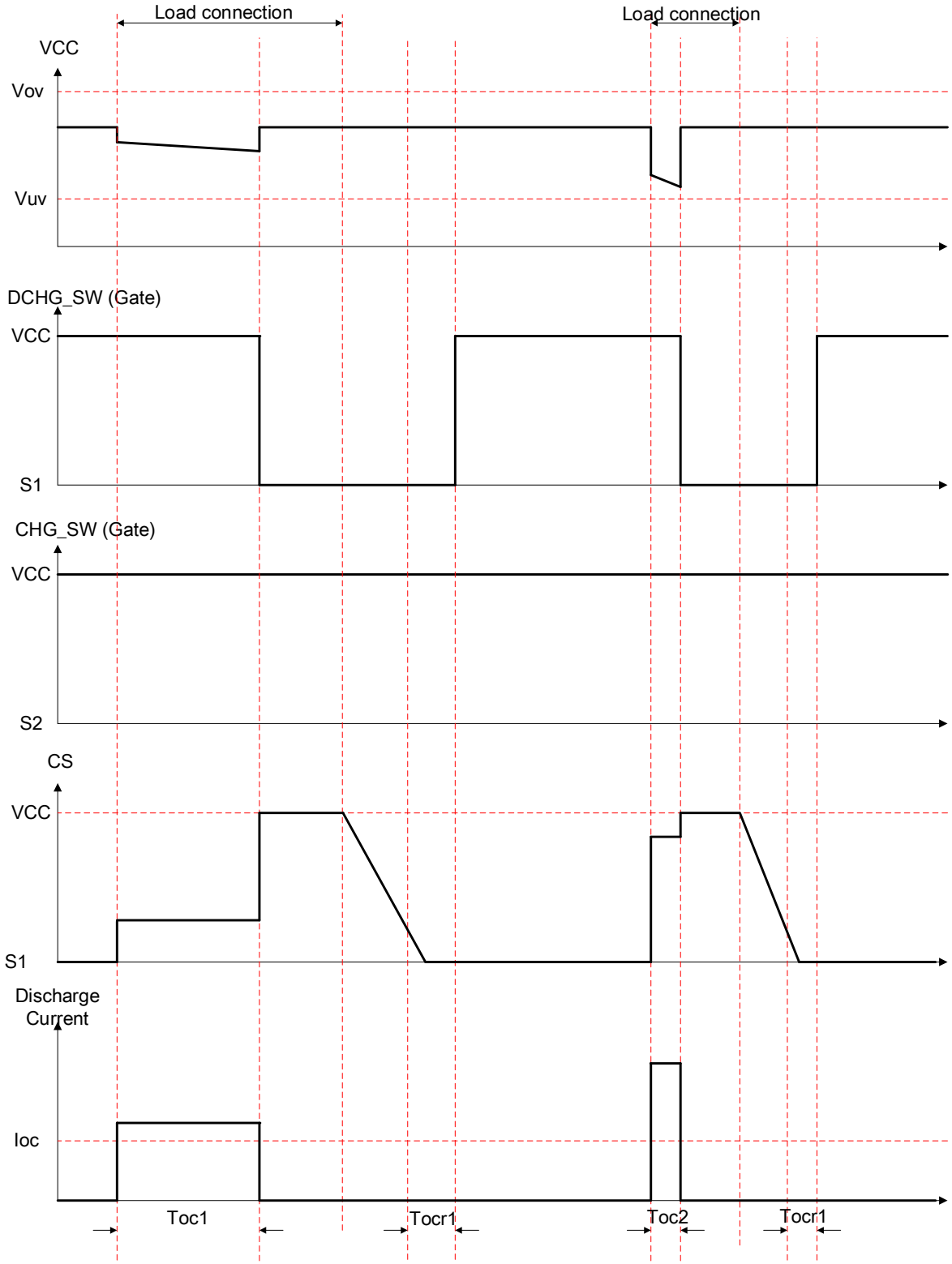
Over-charge detection/release, Over-discharge detection/release (Connect charger)



Over-charge detection/release, Over-discharge detection/release (Non-connect charger)



Discharge over-current detection1, Discharge over-current detection2
(Short circuit)



Charge over-current detection