



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LB1980H — Monolithic Digital IC For VCR Capstan Motors 3-Phase Brushless Motor Driver

Overview

The LB1980JH is a 3-phase brushless motor driver that is particularly appropriate for VCR capstan motor drivers.

Functions

- 3-phase full-wave drive
- Built-in torque ripple correction circuit (variable correction ratio)
- Current limiter circuit
- Upper and lower side output stage over-saturation prevention circuit that does not require external capacitors.
- FG amplifier
- Thermal shutdown circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|----------------------|-------------|------|
| Maximum supply voltage | V _{CC} max | | 7 | V |
| | V _S max | | 24 | V |
| Maximum output current | I _O max | | 1.3 | A |
| Allowable power dissipation | Pd max | Mounted on a board * | 1.81 | W |
| | | Independent IC | 0.77 | W |
| Operating temperature | T _{opr} | | -20 to 75 | °C |
| Storage temperature | T _{stg} | | -55 to +150 | °C |

* Mounted on a 76.1mm×114.3mm×1.6mm, glass epoxy printed circuit board.

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Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------|--------------|---|----------------------|-------|
| Supply voltage | V_S | | 5 to 22 | V |
| | V_{CC} | | 4.5 to 5.5 | V |
| Hall input amplitude | V_{HALL} | Between the hall inputs | ± 30 to ± 80 | mVo-p |
| GSENSE pin input range | V_{GSENSE} | With respect to the control system ground | -0.20 to +0.20 | V |

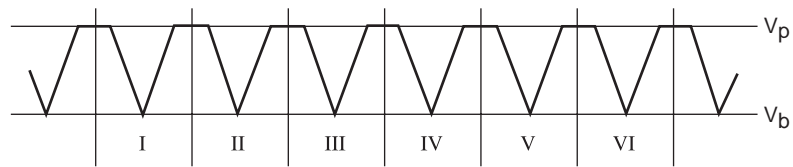
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_S = 15\text{V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|------------------------|---|---------|------|-------|------------------|
| | | | min | typ | max | |
| V_{CC} supply current | I_{CC} | $R_L = \infty$, $V_{CTL} = 0\text{V}$, $V_{LIM} = 0\text{V}$ (Quiescent) | | 12 | 18 | mA |
| Outputs | | | | | | |
| Output saturation voltage | VO sat1 | $I_O = 500\text{mA}$, $R_f = 0.5\Omega$, Sink+Source $V_{CTL} = V_{LIM} = 5\text{V}$ (With saturation prevention) | | 2.1 | 2.6 | V |
| | VO sat2 | $I_O = 1.0\text{mA}$, $R_f = 0.5\Omega$, Sink+Source $V_{CTL} = V_{LIM} = 5\text{V}$ (With saturation prevention) | | 2.6 | 3.5 | V |
| Output leakage current | I_O leak | | | | 1.0 | mA |
| FR | | | | | | |
| FR pin input threshold voltage | V_{FSR} | | 2.25 | 2.50 | 2.75 | V |
| FR pin input bias current | $I_B(\text{FSR})$ | | -5.0 | | | mA |
| Control | | | | | | |
| CTLREF pin voltage | V_{CREF} | | 2.05 | 2.15 | 2.25 | V |
| CTLREF pin input range | V_{CREFIN} | | 1.50 | | 3.50 | V |
| CTL pin input bias current | $I_B(\text{CTL})$ | With $V_{CTL} = 5\text{V}$ and the CTLREF pin open | | | 4.0 | μA |
| CTL pin control start voltage | $V_{CTL}(\text{ST})$ | With $R_f = 0.5\Omega$, $V_{LIM} = 5\text{V}$, $I_O \geq 10\text{mA}$, Hall input logic fixed (U, V, W=H, H, L) | 2.00 | 2.15 | 2.30 | V |
| CTL pin control Gm | $G_m(\text{CTL})$ | With $R_f = 0.5\Omega$, $\Delta I_O = 200\text{mA}$, Hall input logic fixed (U, V, W=H, H, L) | 0.46 | 0.58 | 0.70 | A / V |
| Current Limiter | | | | | | |
| LIM current limit offset voltage | $V_{off}(\text{LIM})$ | With $R_f = 0.5\Omega$, $V_{CTL} = 5\text{V}$, $I_O \geq 10\text{mA}$, Hall input logic fixed (U, V, W=H, H, L) | 140 | 200 | 260 | mV |
| LIM pin input bias current | $I_B(\text{LIM})$ | With $V_{CTL} = 5\text{V}$ and the V_{CREF} pin open | -2.5 | | | μA |
| LIM pin current control level | I_{LIM} | With $R_f = 0.5\Omega$, $V_{CTL} = 5\text{V}$, $V_{LIM} = 2.06\text{V}$ Hall input logic fixed (U, V, W=H, H, L) | 830 | 900 | 970 | mA |
| Hall Amplifier | | | | | | |
| Hall amplifier input offset voltage | $V_{off}(\text{HALL})$ | | -6 | | +6 | mA |
| Hall amplifier input bias current | $I_B(\text{HALL})$ | | | 1.0 | 3.0 | μA |
| Hall amplifier common-mode input voltage range | $V_{CM}(\text{HALL})$ | | | 1.3 | 3.3 | V |
| TRC | | | | | | |
| Torque ripple correction ratio | TRC | For the high and low peaks in the R_f waveform when $I_O = 200\text{mA}$. ($R_f = 0.5\Omega$, with the ADJ pin open) *1 | | 9 | | % |
| ADJ pin voltage | V_{ADJ} | | 2.37 | 2.50 | 2.63 | V |
| FG Amplifier | | | | | | |
| FG amplifier input offset voltage | $V_{off}(\text{FG})$ | | -8 | | +8 | mV |
| FG amplifier input bias current | $I_B(\text{FG})$ | | -100 | | | nA |
| FG amplifier output saturation voltage | V_O sat (FG) | Sink side, for the load provided by the internal pull-up resistor | | | 0.5 | V |
| FG amplifier voltage gain | $V_G(\text{FG})$ | For the open loop state with $f = 10\text{kHz}$ | 41.5 | 44.5 | 47.5 | dB |
| FG amplifier common-mode input voltage | $V_{GM}(\text{FG})$ | | 0.5 | | 4.0 | V |
| Saturation | | | | | | |
| Saturation prevention circuit lower side voltage setting | VO sat(DET) | The voltages between each OUT and R_f pair when $I_O = 10\text{mA}$, $R_f = 0.5\Omega$, and $V_{CTL} = V_{LIM} = 5\text{V}$ | 0.175 | 0.25 | 0.325 | V |
| TSD | | | | | | |
| TSD operating temperature | TSD | Design target value *2 | | 180 | | $^\circ\text{C}$ |
| Hysteresis width | ΔTSD | Design target value *2 | | 20 | | $^\circ\text{C}$ |

Notes : *1. The torque ripple correction ratio is determined as follows from the R_f voltage waveform.

*2. Parameters that are indicated as design target values in the conditions column are not tested.

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For each Hall logic setting

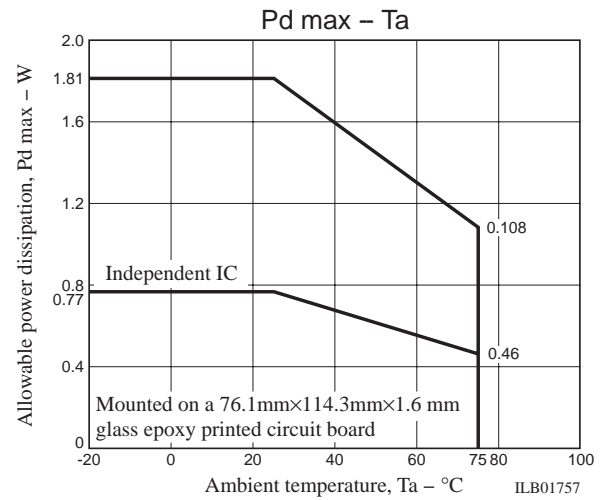
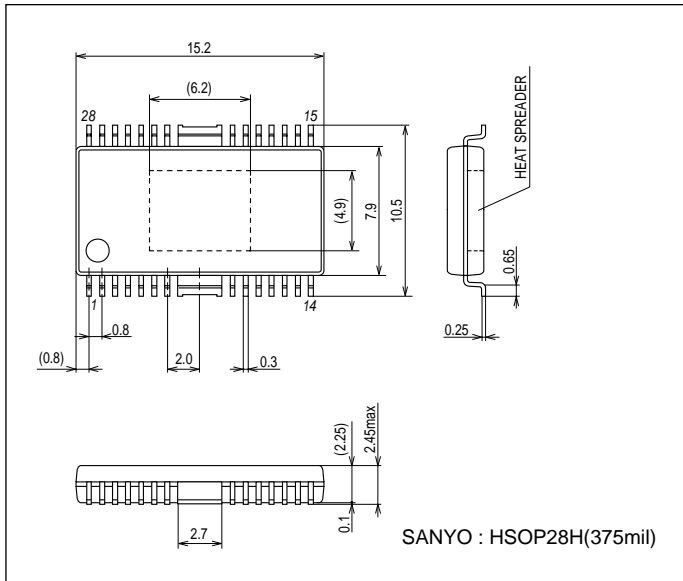
Ground level

$$\text{Correction ratio} = \frac{25(V_p - V_b)}{V_p - V_b} \cdot 1005(\%)$$

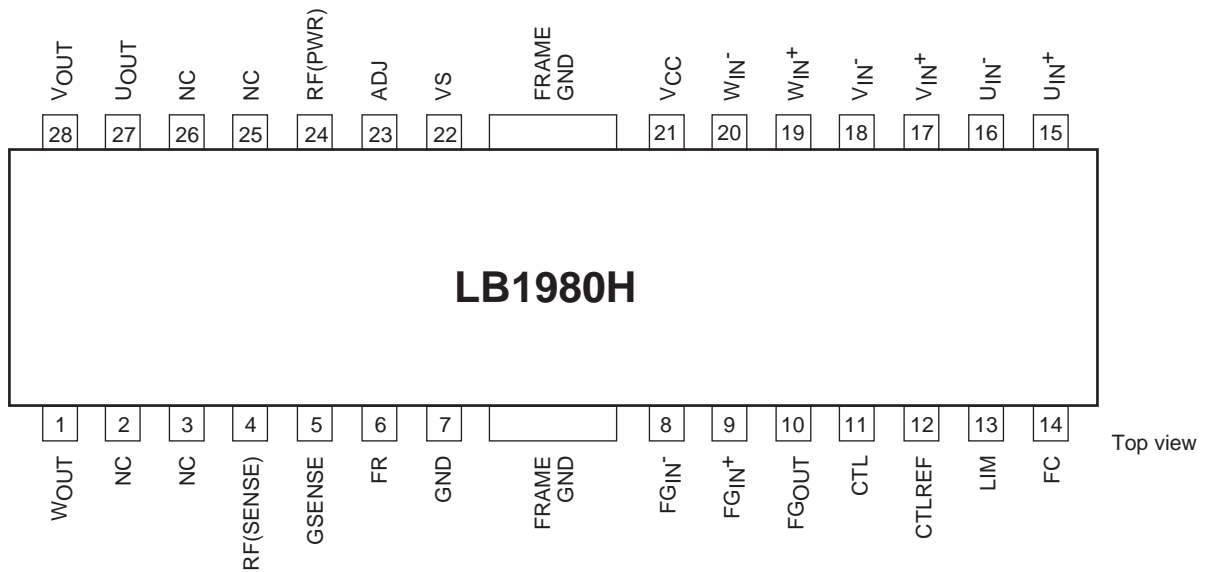
Package Dimensions

unit : mm (typ)

3233B

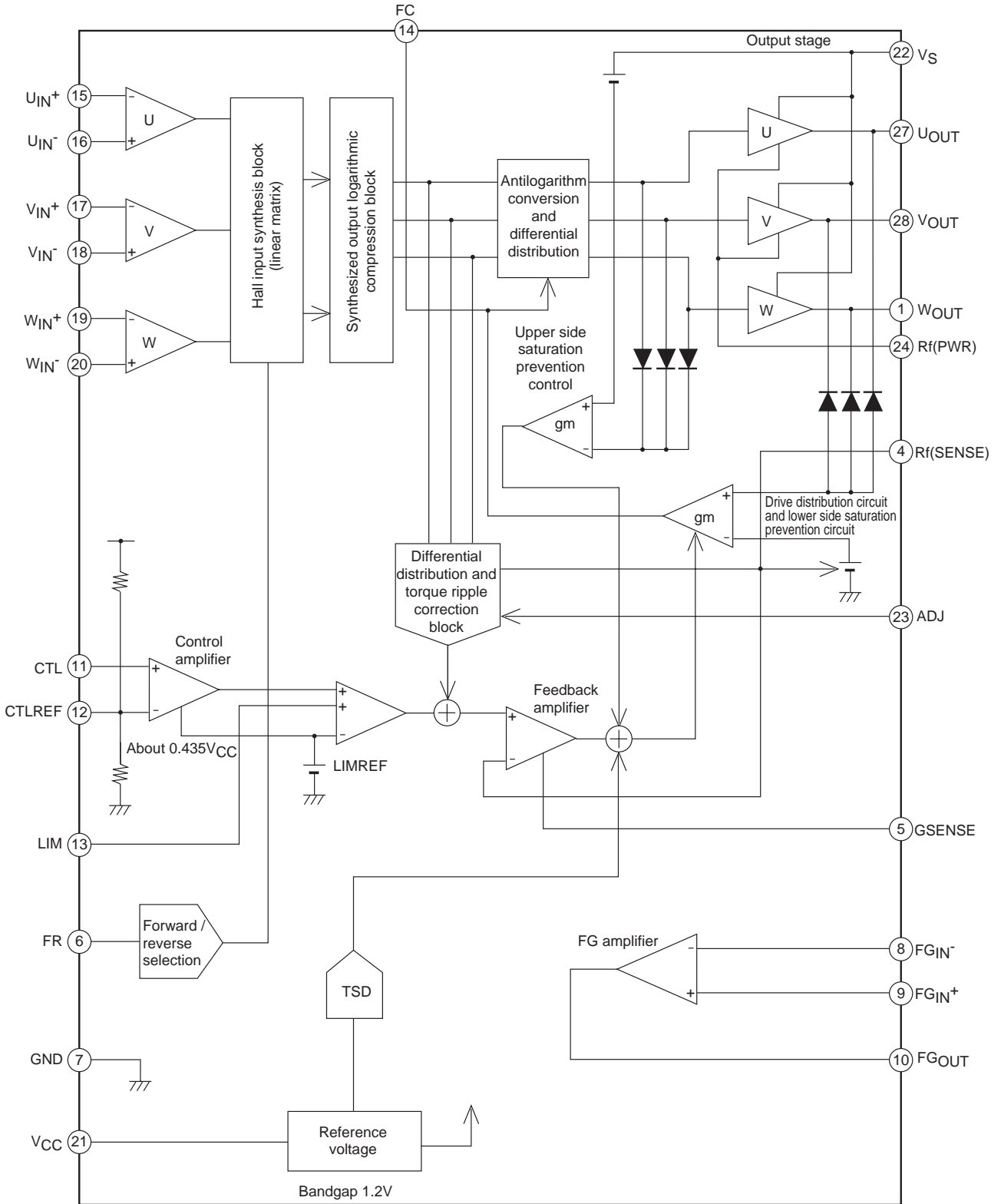


Pin Assignment

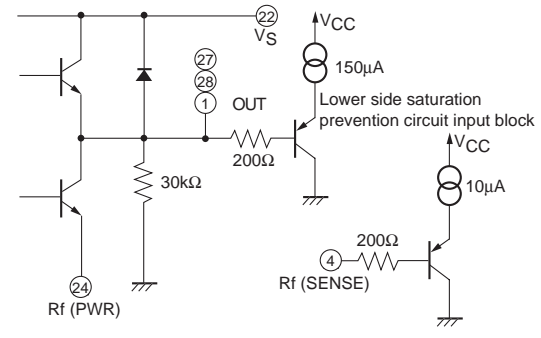
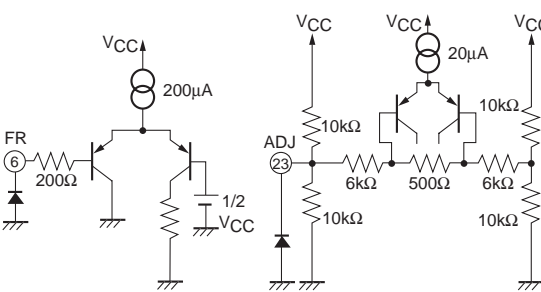
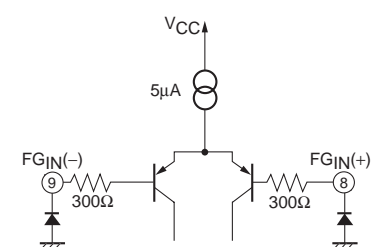
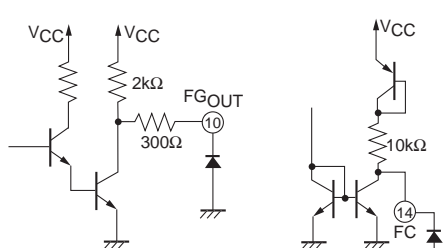


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Block Diagram



Pin Function

| Pin No. | Pin Name | Function | Equivalent circuit |
|---------------|-------------------------------------|--|--|
| 27 28 1 | U_{OUT} V_{OUT} W_{OUT} | U phase output, Spark killer diodes are built-in. V phase output, Spark killer diodes are built-in. W phase output, Spark killer diodes are built-in. |  |
| 4 5 | R_f (SENSE) R_f (PWR) | Output current detection. The control block current limiter operates using the resistor R_f connected between these pins and ground. Also, the lower side saturation prevention circuit and the torque ripple correction circuit operate based on the voltages across this resistor. It is especially important to note that, since the saturation prevention level is set using this voltage, the lower side saturation prevention circuit will become less effective in the high current region if the value of R_f is lowered excessively. Also, the PWR and SENSE pins must be connected together. | |
| 22 | V_S | Output block power supply | |
| 5 | GSENSE | Ground sensing. The influence of the common ground impedance on R_f can be excluded by connecting this pin to nearest ground for the R_f resistor side of the motor ground wiring that includes R_f . (This pin must not be left open.) | |
| 6 | FR | Forward / reverse selection. The voltage applied to this pin selects the motor direction (forward or reverse). ($V_{th}=2.5V$ at $V_{CC}=5V$ (typical)) |  |
| 23 | ADJ | Used for external adjustment of the torque ripple correction ratio. Apply a voltage externally with a low-impedance circuit to the ADJ pin to adjust the correction ratio. The correction ratio falls as the applied voltage is increased, and increases as the applied voltage decreases. The torque ripple correction ratio can be modified by factors in the range 0 to 2 times the ratio that applies when this pin is left open. (The pin voltage is set to about $V_{CC} / 2$ internally, and the input impedance is about $5k\Omega$.) | |
| 7 | GND | Ground for all circuits other than the output transistors. The lowest potential of the output transistors is that of the R_f pin. | |
| 8 | FG_{IN}^- | Input used when the FG amplifier is used as an inverting input. A feedback resistor must be connected between FG_{OUT} and this pin. |  |
| 9 | FG_{IN}^+ | Non-inverting input used when the FG amplifier is used as a differential input amplifier. No bias is applied internally. | |
| 10 | FG_{OUT} | FG amplifier output. There is an internal resistive load. |  |
| 14 | FC | Speed control loop frequency characteristics correction. | |

Continued on next page.

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Continued from preceding page.

| Pin No. | Pin Name | Function | Equivalent circuit |
|---------|------------|---|--------------------|
| 11 | CTL | Speed control input. The control implemented is fixed current drive controlled by current feedback from Rf. $G_m=0.58 / V$ (typical) when $R_f=0.5\Omega$ | |
| 12 | CTLREF | Control reference voltage. While this pin is set to about $0.43 \times V_{CC}$ internally, this voltage can be modified by applying a voltage from a low-impedance circuit. (The input impedance is about $4.3k\Omega$). | |
| 13 | LIM | Current limiter function control. The output current can be varied linearly by applying a voltage to this pin. The slope is $0.5A / V$ (typical) when $R_f=0.5\Omega$. | |
| 15 | U_{IN}^+ | U phase Hall element inputs. | |
| 16 | U_{IN}^- | Logic high is defined as states where $IN^+ > IN^-$. | |
| 17 | V_{IN}^+ | V phase Hall element inputs. | |
| 18 | V_{IN}^- | Logic high is defined as states where $IN^+ > IN^-$. | |
| 19 | W_{IN}^+ | W phase Hall element inputs. | |
| 20 | W_{IN}^- | Logic high is defined as states where $IN^+ > IN^-$. | |
| 21 | V_{CC} | Power supply for all internal blocks other than the output block. This voltage must be stabilized so that noise and ripple do not enter the IC. | |

Truth Table and Control Functions

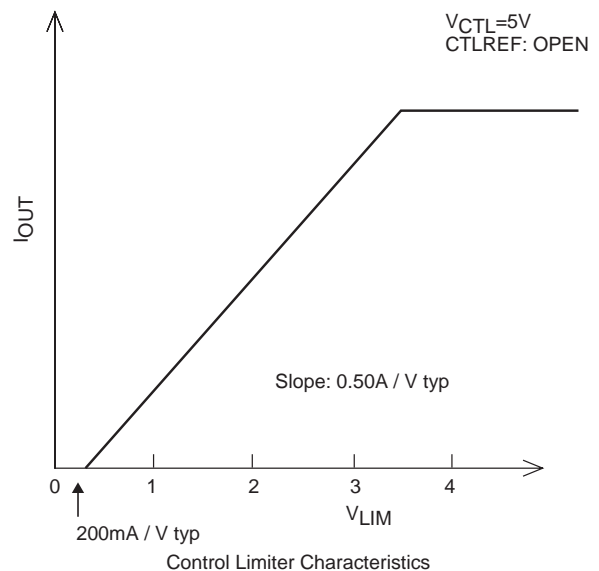
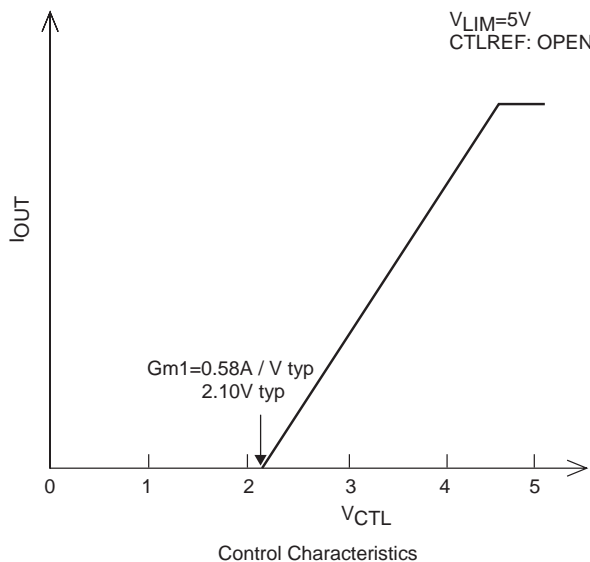
| | Source → Sink | Hall input | | | FR |
|---|-------------------|------------|---|---|----|
| | | U | V | W | |
| 1 | Phase V → Phase W | H | H | L | H |
| | Phase W → Phase V | H | H | L | L |
| 2 | Phase U → Phase W | H | L | L | H |
| | Phase W → Phase U | H | L | L | L |
| 3 | Phase U → Phase V | H | L | H | H |
| | Phase V → Phase U | H | L | H | L |
| 4 | Phase W → Phase V | L | L | H | H |
| | Phase V → Phase W | L | L | H | L |
| 5 | Phase W → Phase U | L | H | H | H |
| | Phase U → Phase W | L | H | H | L |
| 6 | Phase V → Phase U | L | H | L | H |
| | Phase U → Phase V | L | H | L | L |

Note: In the FR column, “H” refers to a voltage of 2.75V or higher, and “L” refers to 2.25V or lower (when $V_{CC}=5V$).

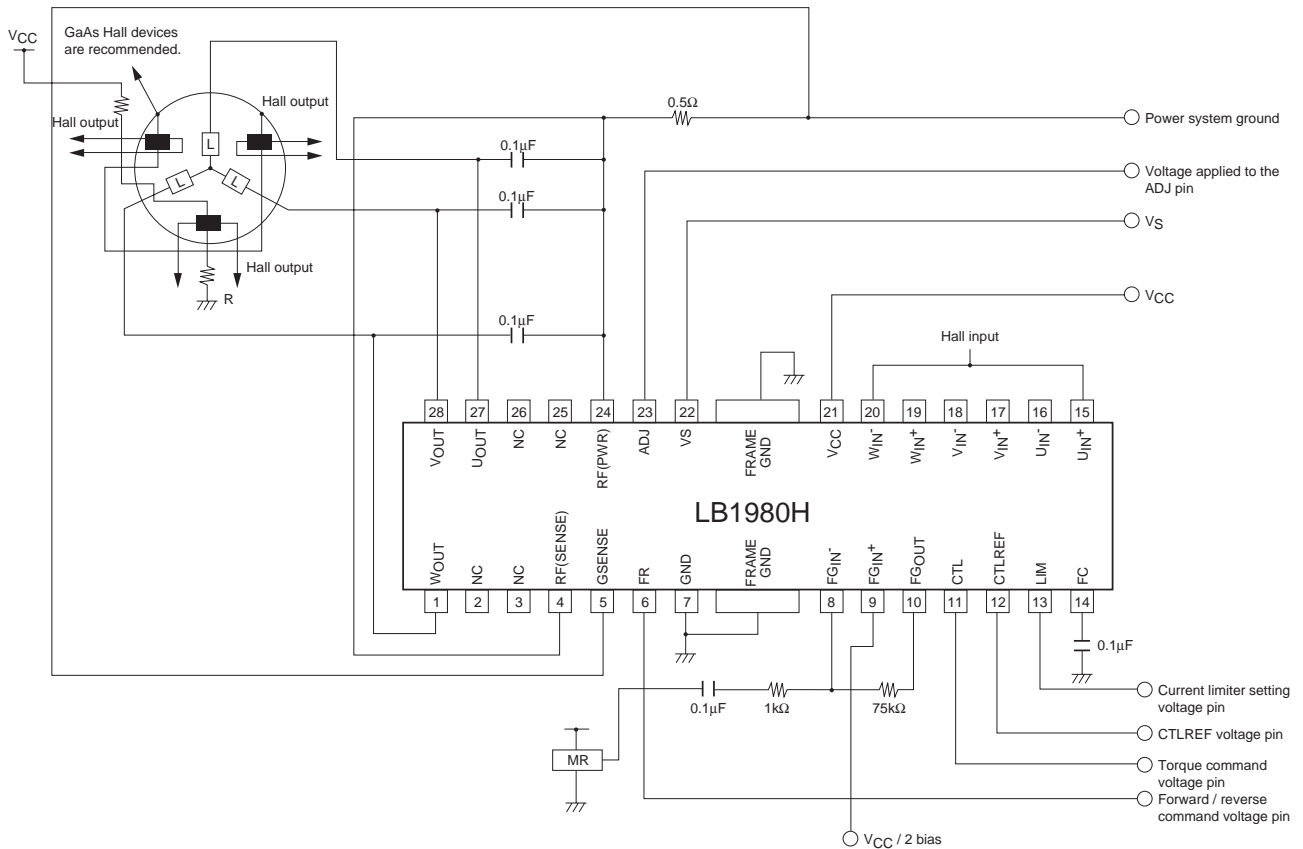
Note: In the Hall input column, “H” refers to the state in the corresponding phase where the +input is at a potential at least 0.01V higher than the -input, and “L” refers to the state where the -input is at a potential at least 0.01V higher than the +input.

Note: Since the drive technique adopted is a 180° technique, phases other than the sink and source phase do not turn off.

Control Function and Current Limiter Function



Application Circuit Example



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