



# LB1952, 1952M

## 3-phase Brushless Motor Driver for VCR Capstans

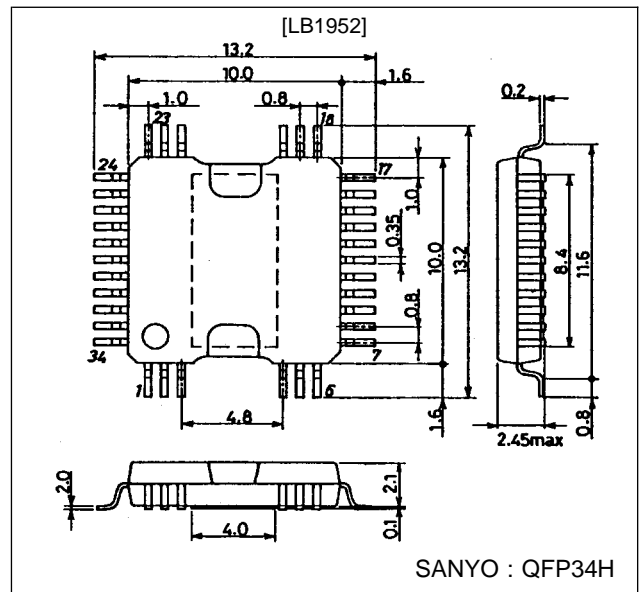
### Functions

- 3-phase full-wave current linear drive system
- Torque ripple correction circuit built in (variable correction factor)
- Current limiting circuit built in
- Output stage upper/lower oversaturation prevention circuit built in (no external capacitor required)
- FG amplifier built in
- Thermal shutdown circuit built in

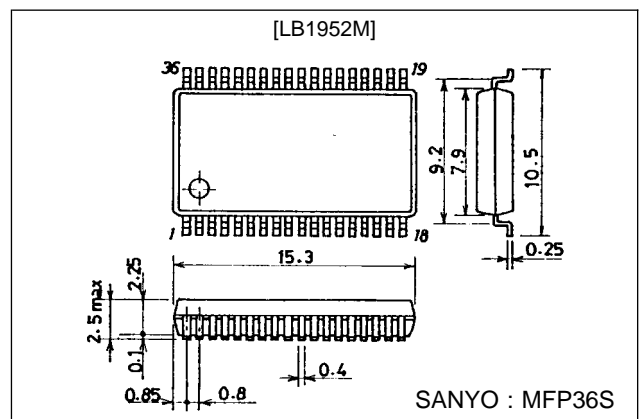
### Package Dimensions

unit : mm

#### 3206-QFP34H



#### 3129-MFP36S



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## Specifications

### Absolute Maximum Ratings at $T_a = 25\text{ }^\circ\text{C}$

| Parameter                   | Symbol       | Conditions                         | Ratings     | Unit             |
|-----------------------------|--------------|------------------------------------|-------------|------------------|
| Maximum supply voltage      | $V_{CC}$ max |                                    | 7           | V                |
|                             | $V_S$ max    |                                    | 24          | V                |
| Maximum output current      | $I_O$ max    |                                    | 1.3         | A                |
| Allowable power dissipation | Pd max       | Arbitrarily large heat sink LB1952 | 12.5        | W                |
|                             |              | Independent IC LB1952              | 0.77        | W                |
|                             |              | Independent IC LB1952M             | 0.95        | W                |
| Operating temperature       | $T_{opr}$    |                                    | -20 to +75  | $^\circ\text{C}$ |
| Storage temperature         | $T_{stg}$    |                                    | -55 to +150 | $^\circ\text{C}$ |

### Allowable Operating Ranges at $T_a = 25\text{ }^\circ\text{C}$

| Parameter            | Symbol       | Conditions                     | Ratings              | Unit              |
|----------------------|--------------|--------------------------------|----------------------|-------------------|
| Supply voltage       | $V_S$        |                                | 5 to 22              | V                 |
|                      | $V_{CC}$     |                                | 4.5 to 5.5           | V                 |
| Hall input amplitude | $V_{HALL}$   | Between Hall inputs            | $\pm 30$ to $\pm 80$ | mV <sub>0-P</sub> |
| GSENSE input range   | $V_{GSENSE}$ | Relative to control system GND | -0.20 to +0.20       | V                 |

### Electrical Characteristics at $T_a = 25\text{ }^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ , $V_S = 15\text{ V}$

| Parameter                                | Symbol           | Conditions   | min  | typ  | max  | Unit          |
|--|------------------|--|------|------|------|---------------|
| $V_{CC}$ supply current                  | $I_{CC}$         | $R_L = \infty$ (when stopped), $V_{CTL} = 0\text{ V}$ , $V_{LIM} = 0\text{ V}$   |      | 12   | 18   | mA            |
| [Output]                                 |                  |  |      |      |      |               |
| Output saturation voltage                | $V_{Osat1}$      | $I_O = 500\text{ mA}$ , $R_f = 0.5\ \Omega$ , Sink + Source<br>$V_{CTL} = V_{LIM} = 5\text{ V}$ (with saturation prevention)   |      | 2.1  | 2.6  | V             |
|  | $V_{Osat2}$      | $I_O = 1.0\text{ A}$ , $R_f = 0.5\ \Omega$ , Sink + Source<br>$V_{CTL} = V_{LIM} = 5\text{ V}$ (with saturation prevention)    |      | 2.6  | 3.5  | V             |
| Output leakage current                   | $I_{oleak}$      |  |      |      | 1.0  | mA            |
| [FR]                                     |                  |  |      |      |      |               |
| FR pin input threshold voltage           | $V_{FSR}$        |  | 2.25 | 2.50 | 2.75 | V             |
| FR pin input bias current                | $I_b$ (FSR)      |  | -5.0 |      |      | $\mu\text{A}$ |
| [Control]                                |                  |  |      |      |      |               |
| CTLREF pin voltage                       | $V_{CREF}$       |  | 2.05 | 2.15 | 2.25 | V             |
| CTLREF pin input range                   | $V_{CREFIN}$     |  | 1.50 |      | 3.50 | V             |
| CTL pin input bias current               | $I_b$ (CTL)      | With $V_{CTL} = 5\text{ V}$ , CTLREF : Open  |      |      | 4.0  | $\mu\text{A}$ |
| CTL pin control start voltage            | $V_{CTL}$ (ST)   | With $R_f = 0.5\ \Omega$ , $V_{LIM} = 5\text{ V}$ , $I_O \geq 10\text{ mA}$ ,<br>Hall input logic fixed, (u, v, w = H, H, L)   | 2.00 | 2.15 | 2.30 | V             |
| CTL pin control Gm                       | Gm (CTL)         | With $R_f = 0.5\ \Omega$ , $\Delta I_O = 200\text{ mA}$ ,<br>Hall input logic fixed, (u, v, w = H, H, L)                       | 0.46 | 0.58 | 0.70 | A/V           |
| [Current Limit]                          |                  |  |      |      |      |               |
| LIM current limit offset voltage         | $V_{off}$ (LIM)  | With $R_f = 0.5\ \Omega$ , $V_{CTL} = 5\text{ V}$ , $I_O \geq 10\text{ mA}$ ,<br>Hall input logic fixed, (u, v, w = H, H, L)   | 140  | 200  | 260  | mV            |
| LIM pin input bias current               | $I_b$ (LIM)      | With $V_{CTL} = 5\text{ V}$ , CTLREF : Open,<br>$V_{LIM} = 0\text{ V}$   | -2.5 |      |      | $\mu\text{A}$ |
| LIM pin current limit level              | $I_{lim}$        | With $R_f = 0.5\ \Omega$ , $V_{CTL} = 5\text{ V}$ , $V_{LIM} = 2.06\text{ V}$ ,<br>Hall input logic fixed, (u, v, w = H, H, L) | 830  | 900  | 970  | mA            |
| [Hall Amplifier]                         |                  |  |      |      |      |               |
| Hall amplifier input offset voltage      | $V_{off}$ (HALL) |  | -6   |      | +6   | mV            |
| Hall amplifier input bias current        | $I_b$ (HALL)     |  |      | 1.0  | 3.0  | $\mu\text{A}$ |
| Hall amplifier common-mode input voltage | $V_{cm}$ (HALL)  |  | 1.3  |      | 3.3  | V             |
| [TRC]                                    |                  |  |      |      |      |               |
| Torque ripple correction factor          | $T_{RC}$         | At bottom and peak in $R_f$ waveform at $I_O = 200\text{ mA}$<br>( $R_f = 0.5\ \Omega$ , ADJ-OPEN) Note 2                      |      | 9    |      | %             |
| ADJ pin voltage                          | $V_{adj}$        |  | 2.37 | 2.50 | 2.63 | V             |

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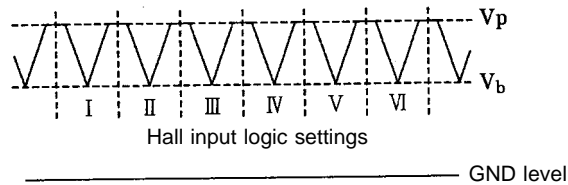
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| Parameter                                       | Symbol                  | Conditions   | min   | typ  | max   | Unit |
|---|-------------------------|--|-------|------|-------|------|
| <b>[FG Amplifier]</b>                           |                         |  |       |      |       |      |
| FG amplifier input offset voltage               | V <sub>off</sub> (FG)   |  | -8    |      | +8    | mV   |
| FG amplifier input bias current                 | I <sub>b</sub> (FG)     |  | -100  |      |       | nA   |
| FG amplifier output saturation voltage          | V <sub>Osat</sub> (FG)  | At internal pull-up resistor load on sink side   |       |      | 0.5   | V    |
| FG amplifier common-mode input voltage          | V <sub>CM</sub> (FG)    |  | 0.5   |      | 4.0   | V    |
| <b>[Saturation]</b>                             |                         |  |       |      |       |      |
| Saturation prevention circuit lower set voltage | V <sub>Osat</sub> (DET) | Voltage between each Out and R <sub>f</sub> at I <sub>O</sub> = 10 mA, R <sub>f</sub> = 0.5 Ω, V <sub>CTL</sub> = V <sub>LIM</sub> = 5 V | 0.175 | 0.25 | 0.325 | V    |
| <b>[TSD]</b>                                    |                         |  |       |      |       |      |
| TSD operation temperature                       | T-TSD                   | (Design target) Note 1   |       | 180  |       | °C   |
| TSD temperature hysteresis width                | ΔTSD                    | (Design target) Note 1   |       | 20   |       | °C   |

Note 1: No measurements are performed for any values listed in the condition column as design targets.

Note 2: The torque ripple correction factor is calculated using the R<sub>f</sub> voltage waveform as follows.



$$\text{Correction factor} = \frac{2 \times (V_p - V_b)}{V_p + V_b} \times 100 (\%)$$

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### Truth Table & Control Function

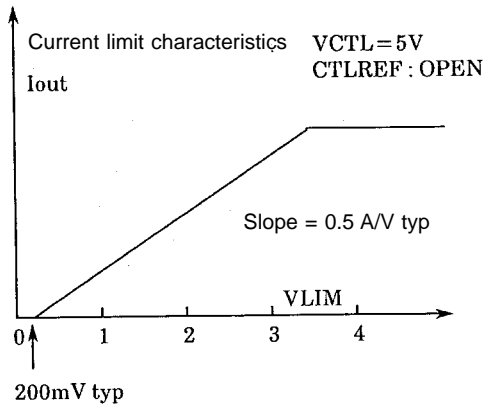
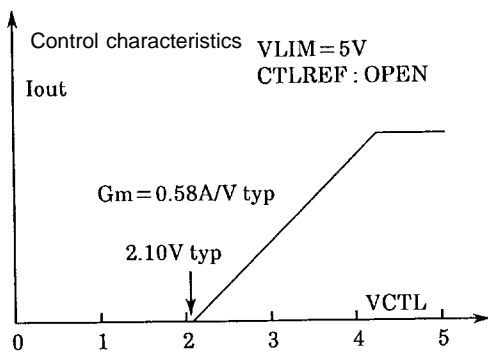
|   | Source → Sink | Hall input |   |   | FR |
|---|---------------|------------|---|---|----|
|   |               | U          | V | W |    |
| 1 | V → W         | H          | H | L | H  |
|   | W → V         | H          | H | L | L  |
| 2 | U → W         | H          | L | L | H  |
|   | W → U         | H          | L | L | L  |
| 3 | U → V         | H          | L | H | H  |
|   | V → U         | H          | L | H | L  |
| 4 | W → V         | L          | L | H | H  |
|   | V → W         | L          | L | H | L  |
| 5 | W → U         | L          | H | H | H  |
|   | U → W         | L          | H | H | L  |
| 6 | V → U         | L          | H | L | H  |
|   | U → V         | L          | H | L | L  |

Note: “H” in the FR column represents a voltage of 2.75V or more; “L” represents a voltage of 2.25V or less.  
(At V<sub>CC</sub> = 5 V)

Note: “H” in the hall input columns represents a state in which “+” has a potential which is higher by 0.01 V or more than that of the “-” phase inputs.  
Conversely, “L” represents a state in which “+” has a potential which is lower by 0.01V or more than that of the “-” phase input.

Note: Since 180° conduction is used as the drive system, other phases than the sink and source phases are turned off.

**Control Function & Current Limit Function**



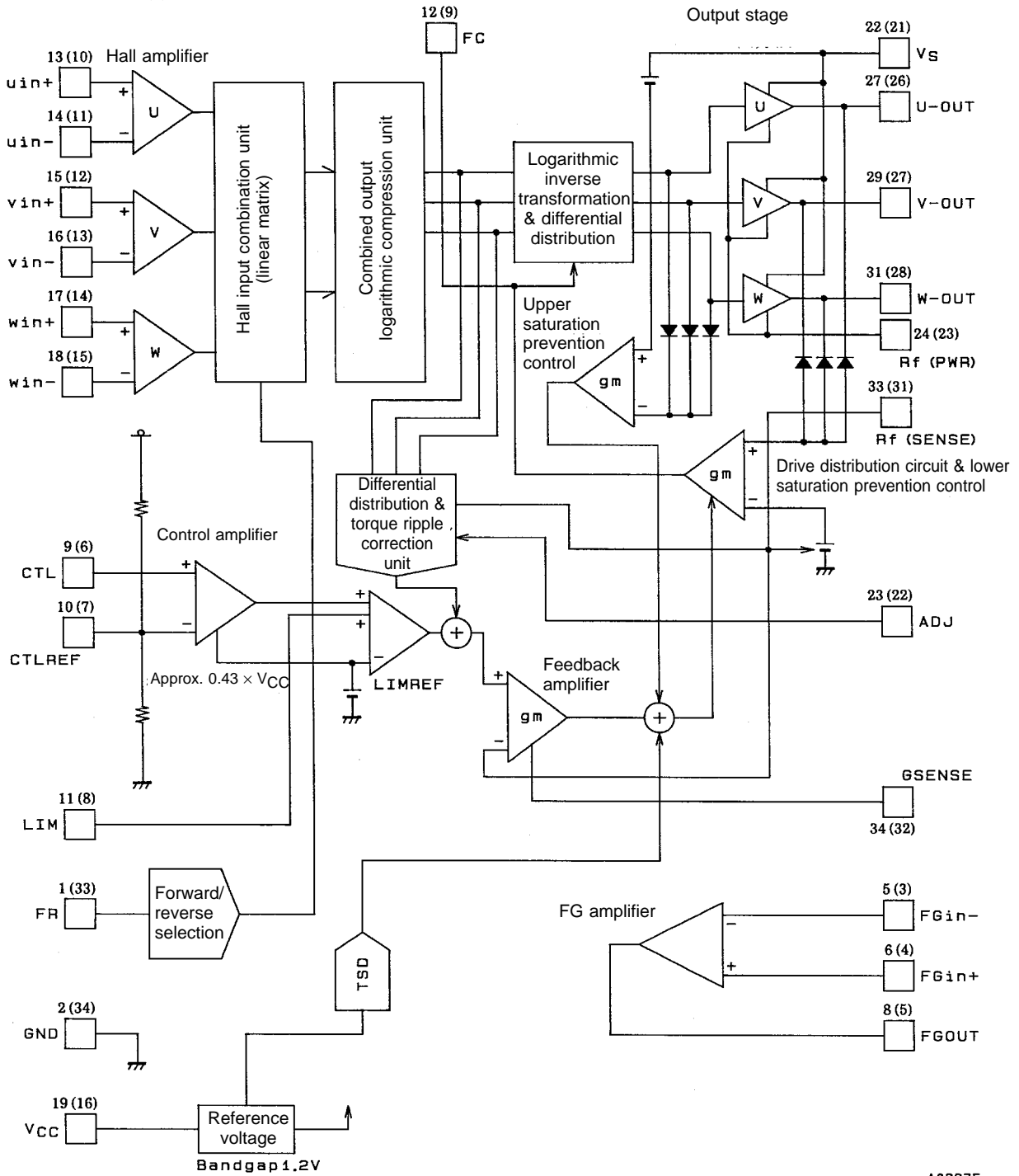
**Pin Functions**

The pin numbers in ( ) are for MFP.

| Pin name  | Pin No.   | Function  |
|---|---|---|
| FR  | 1 (33)  | Forward/reverse select pin. The pin voltage selects forward/reverse. ( $V_{th} = 2.5 V$ typ at $V_{CC} = 5 V$ )   |
| GND   | 2 (34)  | GND for other than output transistor. Minimum potential of output transistor is at Rf pin.  |
| FGin (-)  | 5 (3)   | Input pin when FG amplifier is used with inverted input. Feedback resistor is connected between this pin and FG-OUT.  |
| FGin (+)  | 6 (4)   | Noninverting input pin when FG amplifier is used with differential input. Internal bias is not applied.   |
| FG-OUT  | 8 (5)   | FG amplifier output pin. Resistive load provided internally.  |
| CTL   | 9 (6)   | Speed control pin. Control is exercised by constant-current drive with current feedback applied from Rf. $G_m = 0.58 A/V$ typ at $R_f = 0.5 \Omega$   |
| CTLREF  | 10 (7)  | Control reference voltage pin. The voltage is set internally to approx. $0.43 \times V_{CC}$ but this can be varied by applying voltage through a low impedance (input impedance = approx. $4.3 k\Omega$ ).   |
| LIM   | 11 (8)  | Current limiting function control pin. The output current is varied linearly by this pin voltage; slope = $0.5 A/V$ typ at $R_f = 0.5 \Omega$ .   |
| FC  | 12 (9)  | Speed control loop frequency characteristic correction pin  |
| Uin <sup>+</sup> , Uin <sup>-</sup><br>Vin <sup>+</sup> , Vin <sup>-</sup><br>Win <sup>+</sup> , Win <sup>-</sup> | 13, 14 (10, 11)<br>15, 16 (12, 13)<br>17, 18 (14, 15) | U-phase Hall device input pin; logic "H" represent $IN+ > IN-$ .<br>V-phase Hall device input pin; logic "H" represent $IN+ > IN-$ .<br>W-phase Hall device input pin; logic "H" represent $IN+ > IN-$ .  |
| $V_{CC}$  | 19 (16)   | Power supply pin for supplying power to all circuits except output section in IC; this voltage must be stabilized so as to eliminate ripple and noise.  |
| $V_S$   | 22 (21)   | Output section power supply pin   |
| ADJ   | 23 (22)   | Pin for external adjustment of torque ripple correction factor. When this factor is to be adjusted, a voltage is externally applied to the ADJ pin through a low impedance. If the voltage applied is increased, the factor drops; conversely, if it is reduced, the factor rises. The factor varies between 0 and 2 times that of the open state. (The voltage is set to approx. $V_{CC}/2$ internally, and the input impedance is approx. $5 k\Omega$ .)  |
| Rf (PWR)<br>Rf (SNS)  | 24 (23)<br>33 (31)                                    | Output current detection pin. Current feedback is applied to the control section by connecting Rf between this pin and GND. The lower oversaturation prevention circuit and torque ripple correction circuit are activated in accordance with this pin voltage. Since the oversaturation prevention level is set with this voltage, the lower oversaturation prevention effect may deteriorate in the high current range if the Rf value is reduced to an extremely low level. The PWR and SENSE pins must always be connected. |
| Uout<br>Vout<br>Wout  | 27 (26)<br>29 (27)<br>31 (28)                         | U-phase output pin<br>V-phase output pin<br>W-phase output pin<br>(Built-in spark killer diode)   |
| GSENSE  | 34 (32)   | GND sensing pin. By connecting this pin to the neighboring GND on the Rf resistor side of the motor GND wire which contains Rf, the effect that GND common impedance exerts on Rf can be eliminated. (This pin must not be left open.)  |

# Block Diagram

Pin number inside ( ): for MFP

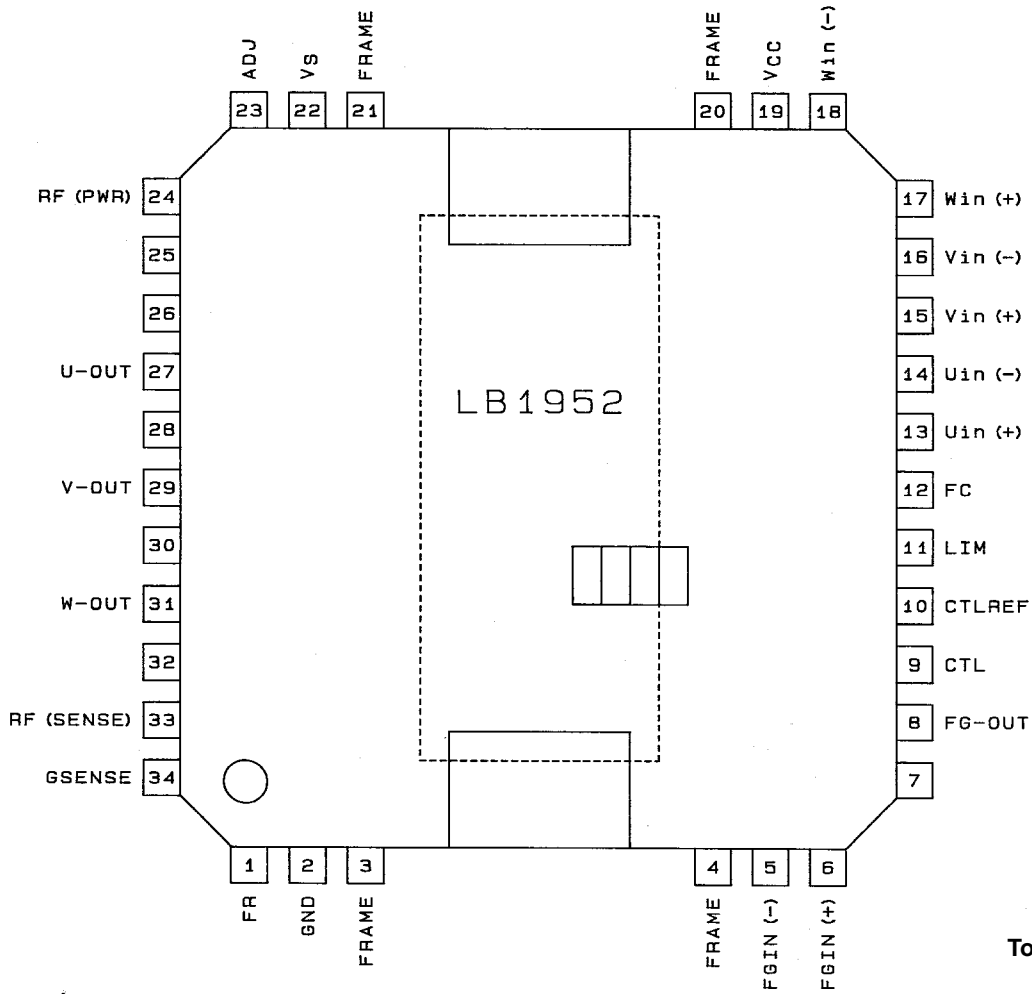


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## Pin Assignment [LB1952]

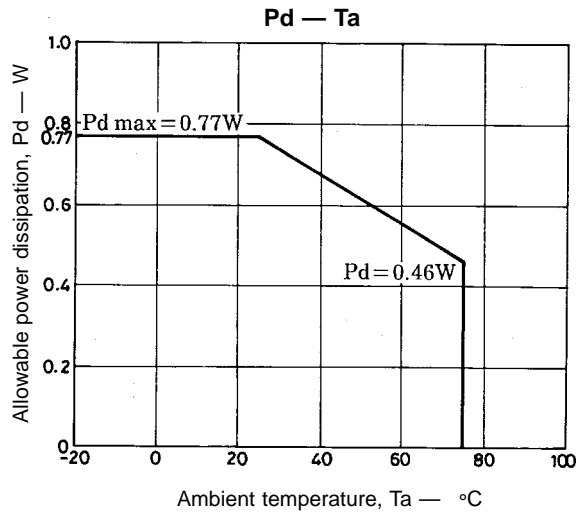
(PACKAGE: QFP-34H-A)



Top view

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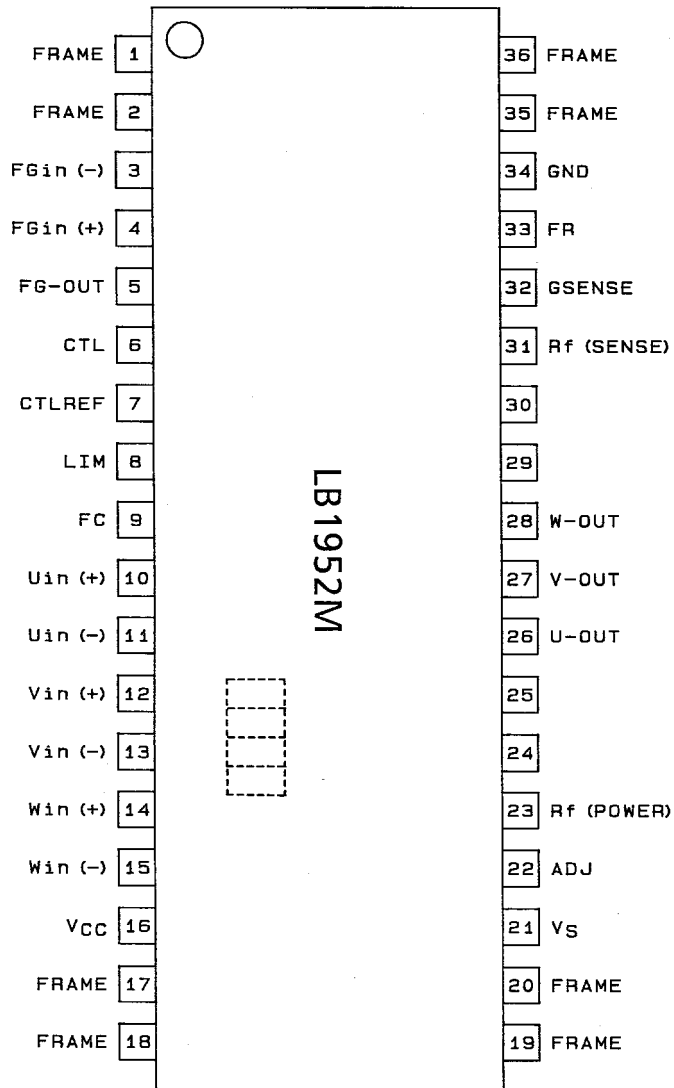
Note: FRAME must be connected to GND for GND potential stabilization.



# LB1952, 1952M

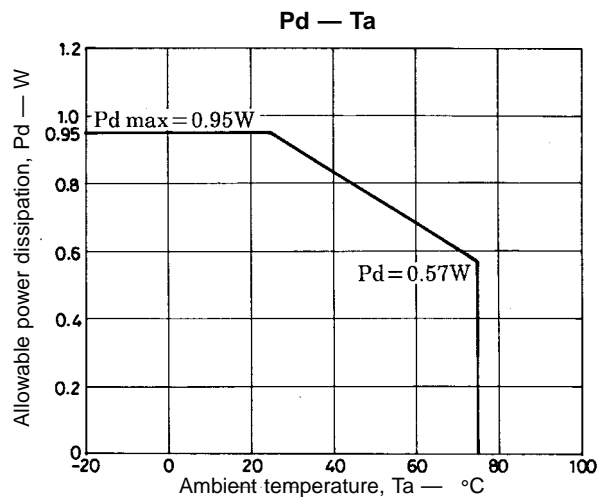
## Pin Assignment [LB1952M]

(PACKAGE: MFP-36S-LF)

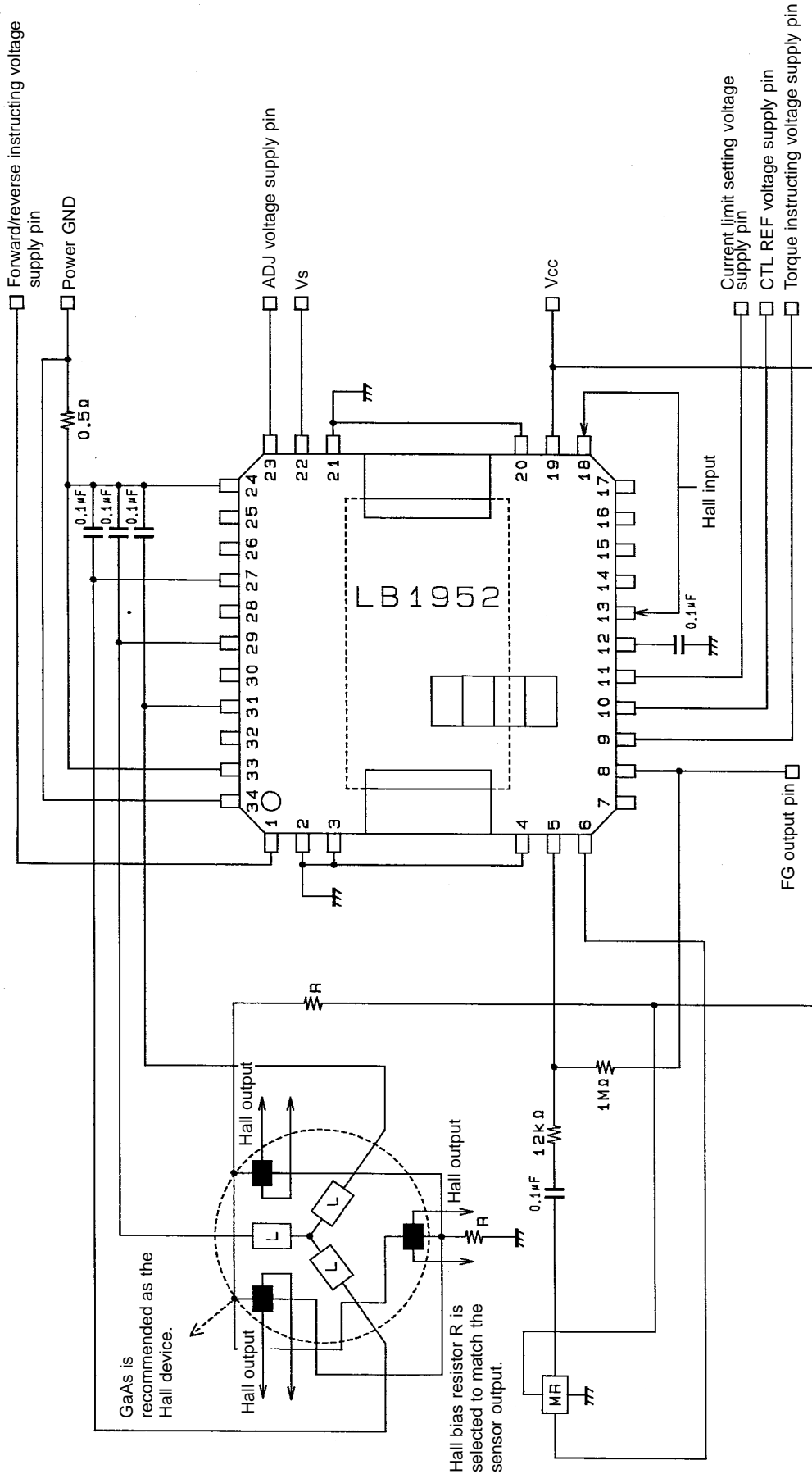


A03977 Top view

Note: Although there is no internal connections between the FRAME pin and GND, FRAME must be connected to GND externally for GND potential stabilization.



Sample Application Circuit [LB1952]

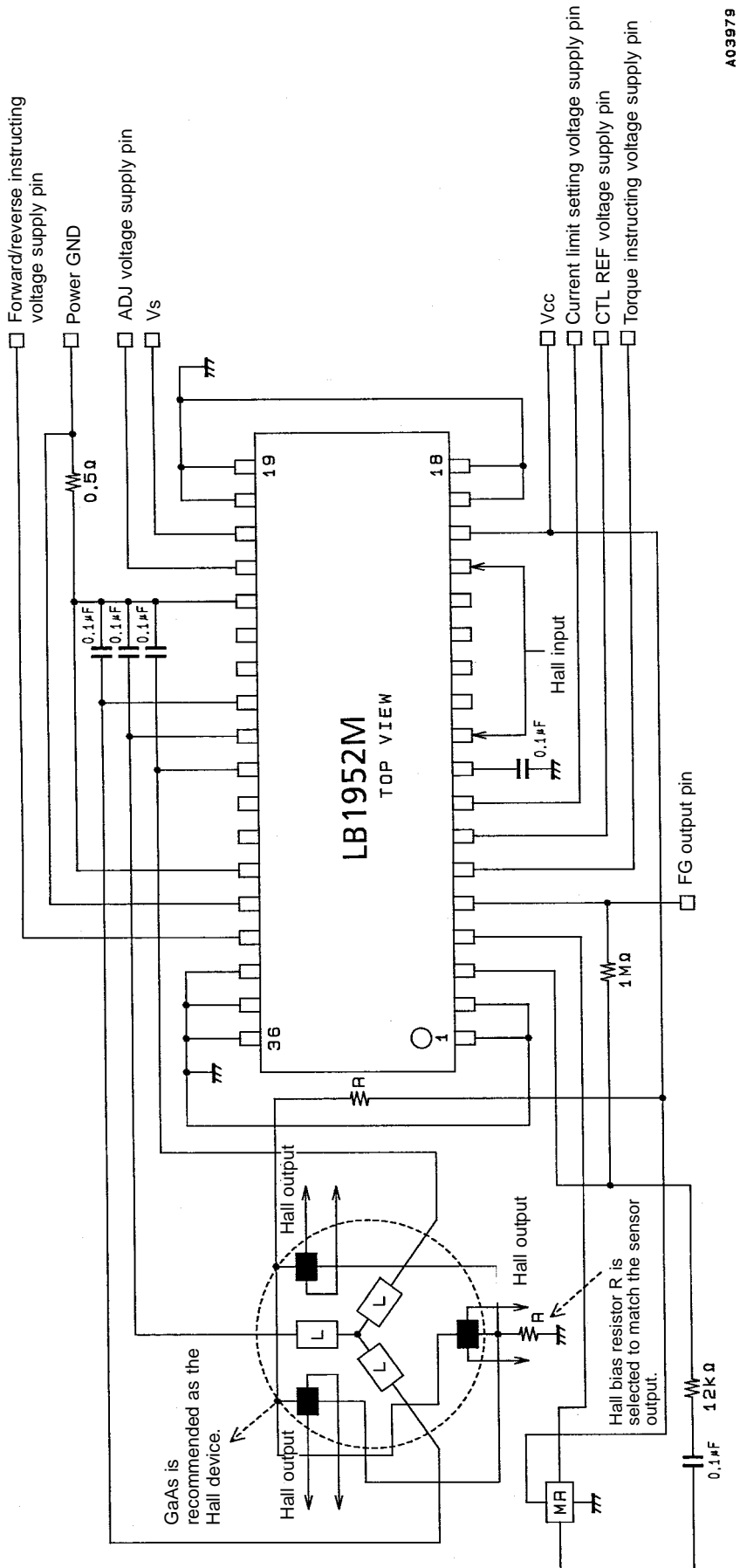


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# LB1952, 1952M

## Sample Application Circuit [LB1952M]



Note: The constants provided in this sample application circuit are provided by way of example and are not intended to guarantee the characteristics.

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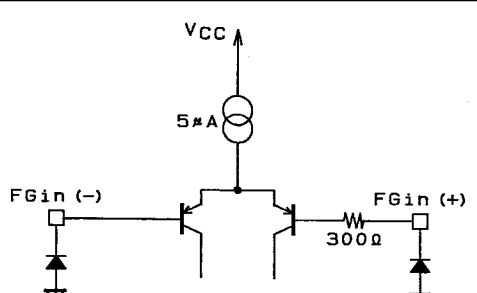
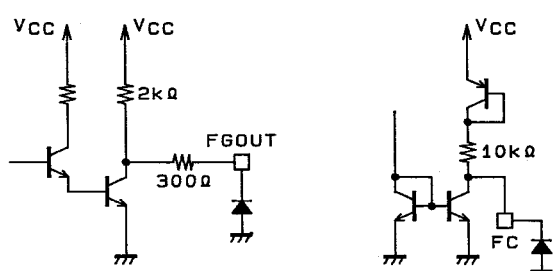
## Pin Input/Output Equivalent Circuit

| Pin name   | Input/Output Equivalent Circuit  |
|--|--|
| Uin (+)<br>Uin (-)<br>Vin (+)<br>Vin (-)<br>Win (+)<br>Win (-) | <p style="text-align: center;">Each (+) input                      Each (-) input</p> <p style="text-align: right;">A03980</p> |
| U-OUT<br>V-OUT<br>W-OUT<br>Vs<br>Rf (POWER)<br>Rf (SENSE)      | <p style="text-align: center;">Each output</p> <p style="text-align: right;">A03981</p>  |
| CTL<br>LIM<br>CTLREF   | <p style="text-align: right;">A03982</p>   |
| FR<br>ADJ  | <p style="text-align: right;">A03983</p>   |

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| Pin name             | Input/Output Equivalent Circuit   |
|----------------------|---|
| FGin (-)<br>FGin (+) |  <p style="text-align: right; margin-right: 50px;">A03984</p> |
| FGOUT<br>FC          |  <p style="text-align: right; margin-right: 50px;">A03985</p> |

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