



# LB1881V

## Three-Phase Brushless Motor Driver IC

### Overview

The LB1881V is a three-phase brushless motor driver IC designed for use as a camcorder capstan or drum motor driver, or as a digital audio tape player/recorder motor driver.

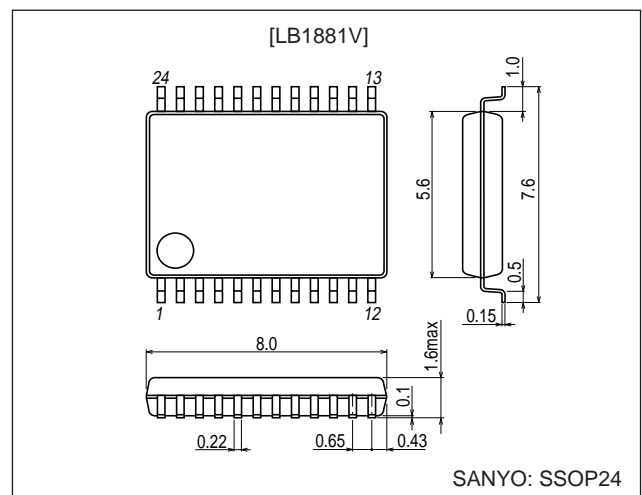
### Features

- 120° voltage linear system
- Appropriate for portable applications, since the LB1881V reduces system power requirements by using motor voltage control for speed control.
- Built-in torque ripple compensation circuit
- Small external capacitances due to the adoption of a soft switching technique (chip capacitor).
- Built-in thermal shutdown circuit
- Built-in FG amplifier

### Package Dimensions

unit: mm

#### 3175A-SSOP24



### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter                   | Symbol                | Conditions     | Ratings     | Unit             |
|-----------------------------|-----------------------|----------------|-------------|------------------|
| Supply voltage              | $V_{CC1 \text{ max}}$ |                | 7           | V                |
|                             | $V_{CC2 \text{ max}}$ |                | 12          | V                |
|                             | $V_S \text{ max}$     |                | $V_{CC2}$   | V                |
| Output applied voltage      | $V_O \text{ max}$     |                | $V_S + 2$   | V                |
| Input applied voltage       | $V_I \text{ max}$     | All input pins | $V_{CC1}$   | V                |
| Output current              | $I_O \text{ max}$     |                | 1.0         | A                |
| Allowable power dissipation | $P_d \text{ max}$     |                | 0.5         | W                |
| Operating temperature       | $T_{opr}$             |                | -20 to +75  | $^\circ\text{C}$ |
| Storage temperature         | $T_{stg}$             |                | -55 to +150 | $^\circ\text{C}$ |

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## LB1881V

### Allowable Operating Ranges at Ta = 25°C

| Parameter      | Symbol           | Conditions                          | Ratings                | Unit |
|----------------|------------------|-------------------------------------|------------------------|------|
| Supply voltage | V <sub>CC1</sub> | V <sub>CC1</sub> ≤ V <sub>CC2</sub> | 4.0 to 6.0             | V    |
|                | V <sub>CC2</sub> |                                     | 4 to 10                | V    |
|                | V <sub>S</sub>   |                                     | Up to V <sub>CC2</sub> | V    |

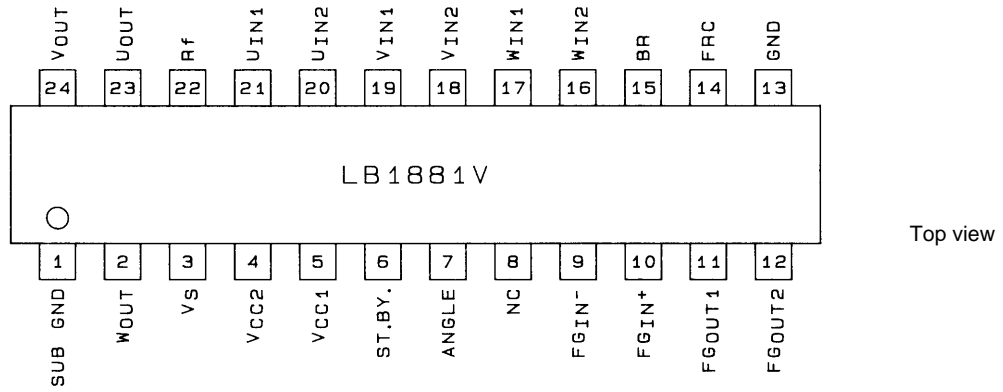
### Electrical Characteristics at Ta = 25°C, V<sub>CC1</sub> = 5 V, V<sub>CC2</sub> = 7 V, V<sub>S</sub> = 3 V

| Parameter  | Symbol                 | Conditions   | Ratings |      |       | Unit |
|--|------------------------|--|---------|------|-------|------|
|  |                        |  | min     | typ  | max   |      |
| Supply current                                   | I <sub>CC1</sub>       | V <sub>BR</sub> = 5 V  |         | 3.0  | 5.0   | mA   |
|  | I <sub>CC2</sub>       | V <sub>BR</sub> = 5 V  |         | 6.5  | 10.0  | mA   |
|  | I <sub>S</sub>         | V <sub>BR</sub> = 5 V, R <sub>L</sub> = ∞  |         |      | 5.0   | mA   |
| Output quiescent current                         | I <sub>CCOQ</sub>      | V <sub>STBY</sub> = 0 V  |         |      | 100   | μA   |
|  | I <sub>SOQ</sub>       | V <sub>STBY</sub> = 0 V, R <sub>L</sub> = ∞  |         |      | 150   | μA   |
| Output saturation voltage                        | V <sub>O(sat)</sub>    | I <sub>OUT</sub> = 0.6 A, sink + source  |         |      | 1.7   | V    |
| Output TRS withstand voltage                     | V <sub>O(sus)</sub>    | I <sub>OUT</sub> = 20 mA*1   | 12      |      |       | V    |
| Output quiescent voltage                         | V <sub>OQ</sub>        | V <sub>BR</sub> = 5 V  | 1.45    | 1.55 | 1.65  | V    |
| Hall amplifier input offset voltage              | V <sub>HOFFSET</sub>   | *1   | -5      |      | +5    | mV   |
| Hall amplifier common mode input voltage range   | V <sub>HCOM</sub>      |  | 1.4     |      | 2.8   | V    |
| Hall I/O voltage gain                            | GV <sub>HO</sub>       | Rangle = 8.2 kΩ  | 34.0    | 37.0 | 40.0  | dB   |
| Brake pin high level voltage                     | V <sub>BRH</sub>       |  | 2.0     |      |       | V    |
| Brake pin low level voltage                      | V <sub>BRL</sub>       |  |         |      | 0.8   | V    |
| Brake pin input current                          | I <sub>BRIN</sub>      |  |         |      | 120   | μA   |
| Brake pin leakage current                        | I <sub>BRLEAK</sub>    |  |         |      | -30   | μA   |
| FRC pin high level voltage                       | V <sub>FRCH</sub>      |  | 2.8     |      |       | V    |
| FRC pin low level voltage                        | V <sub>FRCL</sub>      |  |         |      | 1.2   | V    |
| FRC pin input current                            | I <sub>FRGIN</sub>     |  |         |      | 100   | μA   |
| FRC pin leakage current                          | I <sub>FRCLEAK</sub>   |  |         |      | -30   | μA   |
| Upper side residual voltage                      | V <sub>XH</sub>        | I <sub>OUT</sub> = 100 mA, V <sub>CC2</sub> = 6 V, V <sub>S</sub> = 2 V                    | 0.285   |      | 0.455 | V    |
| Lower side residual voltage                      | V <sub>XL</sub>        | I <sub>OUT</sub> = 100 mA, V <sub>CC2</sub> = 6 V, V <sub>S</sub> = 2 V                    | 0.350   |      | 0.440 | V    |
| Residual voltage inflection point                | V <sub>SΔVX</sub>      | I <sub>OUT</sub> = 100 mA, V <sub>CC2</sub> = 6 V*1  |         | 0.9  |       | V    |
| Overlap level                                    | OL                     | V <sub>CC2</sub> = 6 V, V <sub>S</sub> = 3 V, R <sub>L</sub> = 100 Ω (Y)                   | 60      | 70   | 80    | %    |
| Overlap vertical difference                      | ΔOL                    | V <sub>CC2</sub> = 6 V, V <sub>S</sub> = 3 V, R <sub>L</sub> = 100 Ω (Y)                   | -10     | 0    | +10   | %    |
| Standby on voltage                               | V <sub>STBYL</sub>     | *2   | -0.2    |      | +0.8  | V    |
| Standby off voltage                              | V <sub>STBYH</sub>     |  | 2       |      | 5     | V    |
| Standby pin bias current                         | I <sub>STBYIN</sub>    |  |         |      | 100   | μA   |
| Thermal protection circuit operating temperature | T <sub>TSD</sub>       | *1   | 150     | 180  | 210   | °C   |
| Thermal protection circuit hysteresis            | ΔT <sub>TSD</sub>      | *1   |         | 15   |       | °C   |
| FG amplifier input offset voltage                | V <sub>FG OFFSET</sub> |  | -8      |      | +8    | mV   |
| Open loop voltage gain                           | GV <sub>FG</sub>       | f = 10 kHz   |         | 43   |       | dB   |
| Source output saturation voltage                 | V <sub>FG OU</sub>     | I <sub>O</sub> = -2 mA   | 3.7     |      |       | V    |
| Sink output saturation voltage                   | V <sub>FG OD</sub>     | I <sub>O</sub> = 2 mA  |         |      | 1.3   | V    |
| Common mode signal exclusion ratio               | G <sub>HR</sub>        | *1   |         | 80   |       | dB   |
| FG amplifier common mode input voltage range     | V <sub>FG CH</sub>     |  | 0       |      | 3.5   | V    |
| Phase margin                                     | φ <sub>M</sub>         | *1   |         | 20   |       | deg  |
| Schmitt amplifier threshold voltage              | V <sub>FGS SH</sub>    | V <sub>FGIN</sub> <sup>+</sup> = 2.5 V,<br>when V <sub>FGOUT</sub> 2 goes from high to low | 2.45    | 2.50 | 2.55  | V    |
| Schmitt amplifier hysteresis width               | V <sub>FGS HIS</sub>   | V <sub>FGIN</sub> <sup>+</sup> = 2.5 V   | 20      | 40   | 60    | mV   |

Note: 1. These are target settings, and are not measured. The overlap ratings are taken as test ratings without change.  
2. When the standby pin is open the IC will be in the standby state.

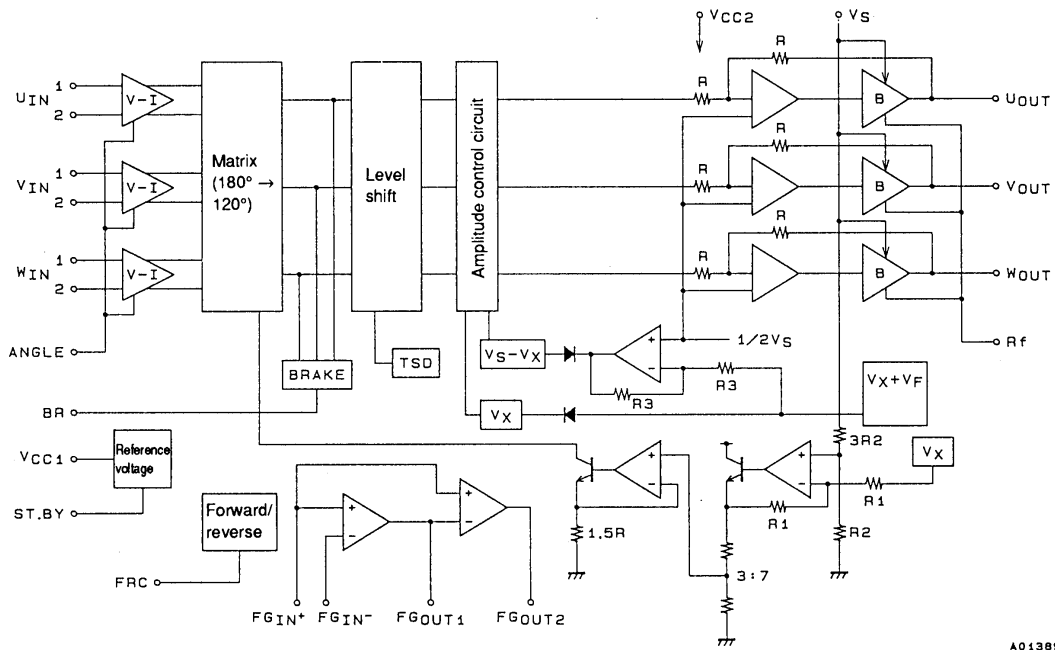
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## Pin Assignment

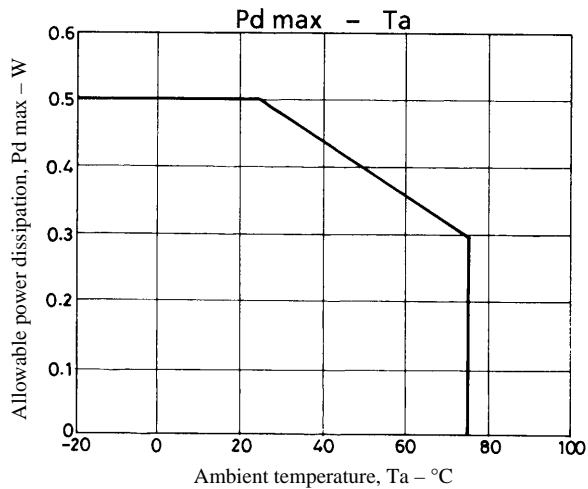


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## Block Diagram



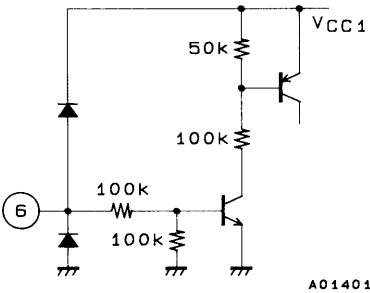
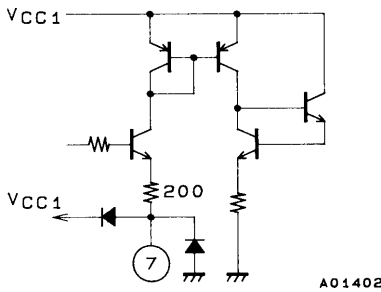
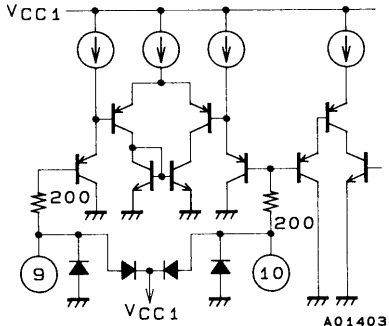
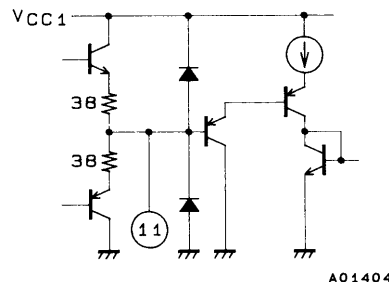
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# LB1881V

## Pin Functions

Unit (resistance:  $\Omega$ )

| Pin No. | Symbol                     | Pin voltage   | Equivalent circuit   | Pin function   |
|---------|----------------------------|---|--|--|
| 3       | $V_S$                      | $\leq V_{CC2}$  |  | Power supply input that determines the output amplitude. It must be set to a voltage equal or lower than $V_{CC2}$ .   |
| 4       | $V_{CC2}$                  | 4 to 10 V   |  | Power supply for power amplifier systems other than motor drive transistors. Power supply pin that provides voltage for blocks other than control blocks supplied by $V_{CC1}$ .                                   |
| 5       | $V_{CC1}$                  | 4 to 6 V  |  | Power supply that provides voltage for the Hall amplifier, the forward/reverse circuit, the FG amplifier, and the thermal shutdown circuit.  |
| 6       | ST. BY                     | (H): 2.0 V max<br>(L): 0.8 V min<br>(When $V_{CC1}$ is 5 V) |  <p style="text-align: right;">A01401</p>   | All circuits can be made inoperative either by connecting this pin to GND, or by leaving it open. In that state the supply current will be approximately 0 $\mu$ A. Hold at 2 V or higher during normal operation. |
| 7       | ANGLE                      |   |  <p style="text-align: right;">A01402</p>  | Connect a resistor between this pin and GND. Changing the value of this resistor will change the Hall input-output gain (motor waveform slope).  |
| 9<br>10 | $FG_{IN}^-$<br>$FG_{IN}^+$ | 0 V min<br>3.5 V max<br>(When $V_{CC1}$ is 5 V)             |  <p style="text-align: right;">A01403</p> | FG signal input pin  |
| 11      | $FG_{OUT1}$                |   |  <p style="text-align: right;">A01404</p> | FG amplifier output pin  |

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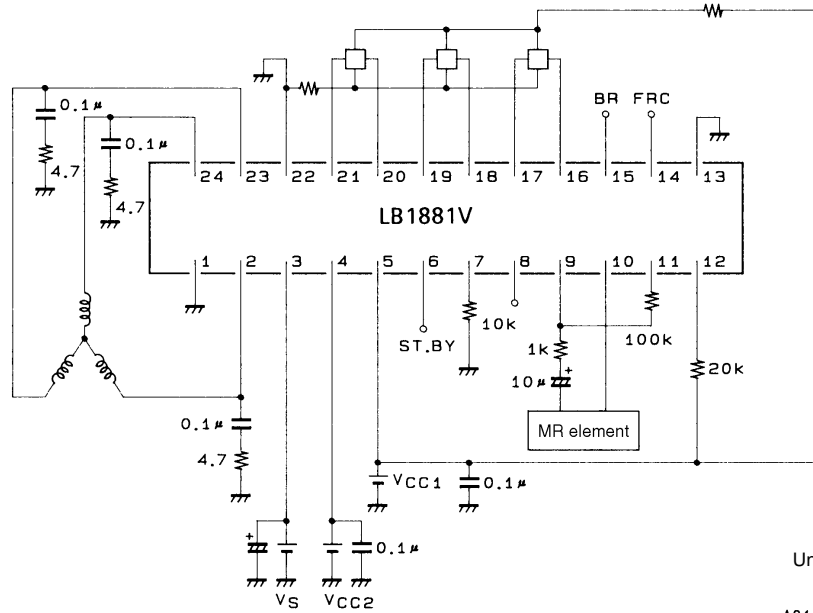
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Unit (resistance:  $\Omega$ )

| Pin No.                          | Symbol   | Pin voltage  | Equivalent circuit | Pin function   |
|----------------------------------|--|--|--------------------|--|
| 12                               | FG <sub>OUT2</sub>   |  |                    | FG Schmitt amplifier output pin  |
| 14                               | FRC  | (H): 2.8 V min<br>(L): 1.2 V max<br>(When V <sub>CC1</sub> is 5 V) |                    | Pin for setting the motor to forward or reverse rotation<br>Low level: Forward rotation (under 1.2 V: when V <sub>CC1</sub> is 5 V)<br>High level: Reverse rotation (over 2.8 V: when V <sub>CC1</sub> is 5 V)   |
| 15                               | BR   | (H): 2.0 V min<br>(L): 0.8 V max                                   |                    | Motor brake pin<br>Low level: Motor drive (under 0.8 V)<br>High level: Motor brake (over 2.0 V)  |
| 16<br>17<br>18<br>19<br>20<br>21 | W <sub>IN2</sub><br>W <sub>IN1</sub><br>V <sub>IN2</sub><br>V <sub>IN1</sub><br>U <sub>IN2</sub><br>U <sub>IN1</sub> | 1.4 V min<br>2.8 V max<br>(When V <sub>CC1</sub> is 5 V)           |                    | W phase Hall element input pins.<br>Logic high is defined to be states where W <sub>IN1</sub> > W <sub>IN2</sub> .<br>V phase Hall element input pins.<br>Logic high is defined to be states where V <sub>IN1</sub> > V <sub>IN2</sub> .<br>U phase Hall element input pins.<br>Logic high is defined to be states where U <sub>IN1</sub> > U <sub>IN2</sub> . |
| 22                               | R <sub>f</sub>   |  |                    | Output transistor GND  |
| 23<br>24<br>2                    | U <sub>OUT</sub><br>V <sub>OUT</sub><br>W <sub>OUT</sub>   |  |                    | Output pin   |
| 1<br>13                          | SUBGND<br>GND  |  |                    | GND for all circuits other than output transistors.  |

# LB1881V

## Sample Application Circuit



Units (resistance: Ω, capacitance: F)

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## Logic Value Table

|   | Source            | Sink | Input |   |   | Forward and reverse control<br>F/RC |
|---|-------------------|------|-------|---|---|-------------------------------------|
|   |                   |      | U     | V | W |                                     |
| 1 | W phase → V phase |      | H     | H | L | L                                   |
|   | V phase → W phase |      | H     | H | L | H                                   |
| 2 | W phase → U phase |      | H     | L | L | L                                   |
|   | U phase → W phase |      | H     | L | L | H                                   |
| 3 | V phase → W phase |      | L     | L | H | L                                   |
|   | W phase → V phase |      | L     | L | H | H                                   |
| 4 | U phase → V phase |      | L     | H | L | L                                   |
|   | V phase → U phase |      | L     | H | L | H                                   |
| 5 | V phase → U phase |      | H     | L | H | L                                   |
|   | U phase → V phase |      | H     | L | H | H                                   |
| 6 | U phase → W phase |      | L     | H | H | L                                   |
|   | W phase → U phase |      | L     | H | H | H                                   |

Inputs:

High: For each phase, the input 1 potential is at least 0.2 V higher than the input 2 potential.

Low: For each phase, the input 1 potential is at least 0.2 V lower than the input 2 potential.

Forward/reverse control:

High: 2.8 V to V<sub>CC1</sub>

Low: 0 to 1.2 V

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