Ordering number : ENA0609A

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

Monolithic Digital IC

LB11850VA — For Fan Motor Single-Phase Full-Wave Pre-Driver with Speed Control Function

Overview

The LB11850VA is a single-phase bipolar fan motor driver with speed control function that works with a speed feedback signal. A highly efficient, quiet and low power consumption motor driver circuit, with a high speed accuracy and large variable speed can be implemented by adding a small number of external components.
This pre-driver is optimal for driving large scale fan motors (with large air volume and large current) such as those used in servers and consumer products.

Functions and features

- Pre-driver for single-phase full-wave drive
  →PMOS-NMOS is used as an external power TR, enabling high-efficiency and low-power-consumption drive by means of the low-saturation output and single-phase full-wave drive.
- On-chip speed control circuit
  →The speed control (closed loop control) using a speed feedback signal makes it possible to achieve higher speed accuracy and lower speed fluctuations when supply voltage fluctuates or load fluctuates, compared with an open-loop control system. Separately excited upper direct PWM control method is used as the variable-speed control system.
- External PWM input or analog voltage input enabling variable speed control
  →The speed control input signal is compatible with PWM duty ratio or analog voltages.
- On-chip soft start circuit
- Lowest speed setting pin
  →The lowest speed can be set with the external resistor.
- Current limiter circuit incorporated
  →Chopper type current limit at start or lock.
- Reactive current cut circuit incorporated
  →Reactive current before phase change is cut to enable silent and low-consumption drive.
- Constraint protection and automatic reset functions incorporated
- FG (speed detection), RD (lock detection) output
- Constant-voltage output pin for hall bias

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} maximum supply voltage	V_{CC} max		18	V
OUTN pin maximum output current	I_{OUT}N max		20	mA
OUTP pin maximum sink current	I_{OUT}P max		20	mA
OUT pin output withstand voltage	V_{OUT} max		18	V
HB maximum output current	HB		10	mA
CTL, C pin withstand voltage	CTL, C max		7	V
CVI, LIM pin withstand voltage	CVI, LIM max		7	V
RD/FD output pin output withstand voltage	FG max		19	V
RD/FG output current	FG max		10	mA
5VREG pin maximum output current	I5VREG max		10	mA
Allowable power dissipation	Pd max	Mounted on a specified board *	0.9	W
Operating temperature range	Topr		-30 to +95	°C
Storage temperature range	Tstg		-55 to +150	°C

Note *1: Mounted on a specified board: 114.3mm×76.1mm×1.6mm, glass epoxy.

Note *2: Tj max = 150°C. Use the device in a condition that the chip temperature does not exceed Tj = 150°C during operation.

Recommended Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} supply voltage 1	V_{CC}1	V_{CC} pin	5.5 to 16	V
V_{CC} supply voltage 2	V_{CC}2	When V_{CC}-5VREG shorted	4.5 to 5.5	V
CTL input voltage range	VCTL		0 to 5VREG	V
LIM input voltage range	VLIM		0 to 5VREG	V
VCI input voltage range	VCVI		0 to 5VREG	V
Hall input common phase input voltage range	VICM		0.2 to 3	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V, unless otherwise specified

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Circuit current	I_{CC}1	During drive		12	15	mA
	I_{CC}2	During lock protection		12	15	mA
5VREG voltage	5VREG	I5VREG = 5mA	4.8	5.0	5.2	V
HB voltage	VHB	IHB = 5mA	1.05	1.20	1.35	V
Current limiter voltage	VLIM		190	210	230	mV
CPWM pin H level voltage	VCRH		2.8	3.0	3.2	V
CPWM pin L level voltage	VCRL		0.9	1.1	1.3	V
CPWM pin charge current	ICPWM1	VCPWM = 0.5V	24	30	36	μA
CPWM pin discharge current	ICPWM2	VCPWM = 3.5V	21	27	33	μA
CPWM oscillation frequency	FPWM	C = 220pF		30		kHz
CT pin H level voltage	VCTH		2.8	3.0	3.2	V
CT pin L level voltage	VCTL		0.9	1.1	1.3	V
CT pin charge current	ICT1	VCT = 2V	1.6	2.0	2.5	μA
CT pin discharge current	ICT2	VCT = 2V	0.16	0.20	0.25	μA
CT pin charge/discharge current ratio	RCT	ICT1/ICT2	8	10	12	times
OUTN pin output H voltage	VONH	I_O = 10mA		V_{CC}-0.85	V_{CC}-1.0	V
OUTN pin output L voltage	VONL	I_O = 10mA		0.9	1.0	V
OUTP pin output L voltage	VOPL	I_O = 10mA		0.5	0.65	V

Continued on next page.

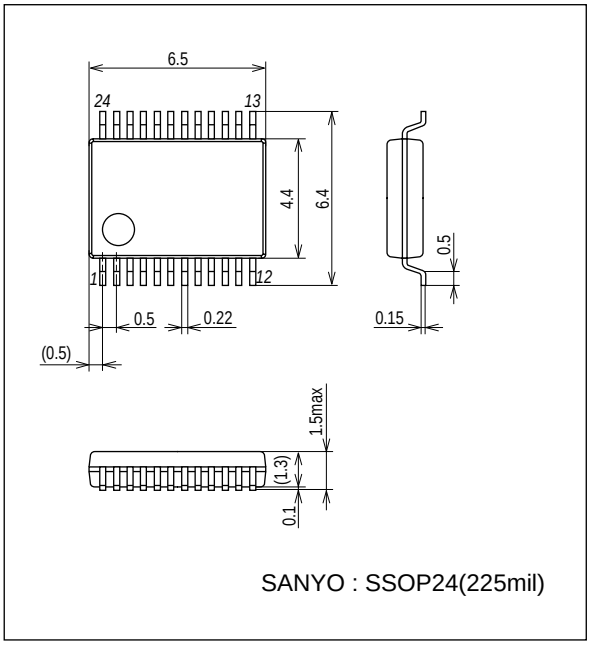
Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Hall input sensitivity	VHN	IN^+, IN^- difference voltage (including offset and hysteresis)		±15	±25	mV
FG output L voltage	VFGL	IFG = 5mA		0.15	030	μA
FG pin leak current	IFGL	VFG = 19V			30	μA
RD output L voltage	VRDL	IRD = 5mA		0.15	0.30	V
RD pin leak current	IRDL	VRD = 19V			30	μA
EO pin output H voltage	VEOH	IEO1 = -0.2mA	VREG-1.2	VREG-0.8		V
EO pin output L voltage	VEOL	IEO1 = 0.2mA		0.8	1.1	V
RC pin output H voltage	VRCH		3.2	3.45	3.7	V
RC pin output L voltage	VRCL		0.7	0.8	1.05	V
RC pin clamp voltage	VRCCLP		1.3	1.5	1.7	V
CTL pin input H voltage	VCTLH		2.0		VREG	V
CTL pin input L voltage	VCTLL		0		1.0	V
CTL pin input open voltage	VCTLO		VREG-0.5		VREG	V
CTL pin H input H current	ICTLH	VFGIN = 5VREG	-10	0	10	μA
CTL pin L input L current	ICTLL	VFGIN = 0V	-120	-90		μA
C pin output H voltage	VCH		VREG-0.3	VREG-0.1		V
C pin output L voltage	VCL		1.8	2.0	2.2	V
LIM pin input bias current	IBLIM		-1		1	μA
LIM pin common phase input voltage range	VILIM		2.0		VREG	V
SOFT pin charge current	ICSOFT		1.0	1.3	1.6	μA
SOFT pin operating voltage range	VISOFT		2.0		VREG	V
CVI pin input bias current	IB(VCI)		-1		2	μA
CVI pin common phase input voltage range	VIVCI		2.0		VREG	V
CVO pin output H level voltage	V_{OH}(VCO)		VREG-0.35	VREG-0.2		V
Output L level voltage	V_{OL}(VCO)		1.8	2.0	2.2	V

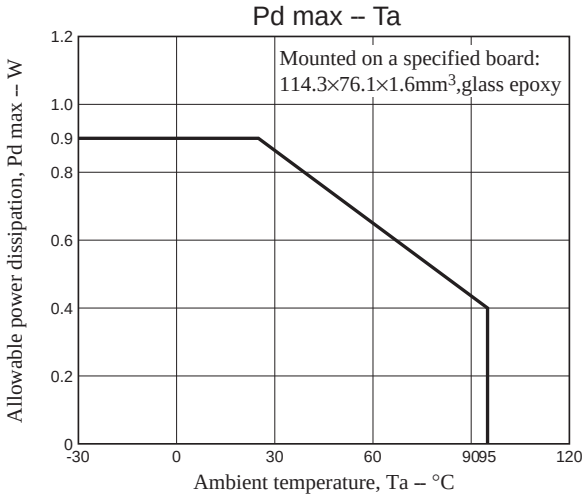
Package Dimensions

unit : mm (typ)

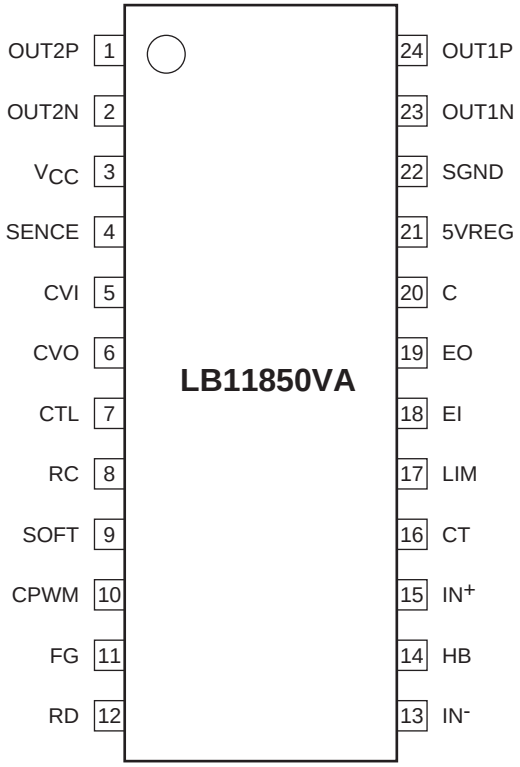
3287



SANYO : SSOP24(225mil)



Pin Assignment



Top view

Truth Table

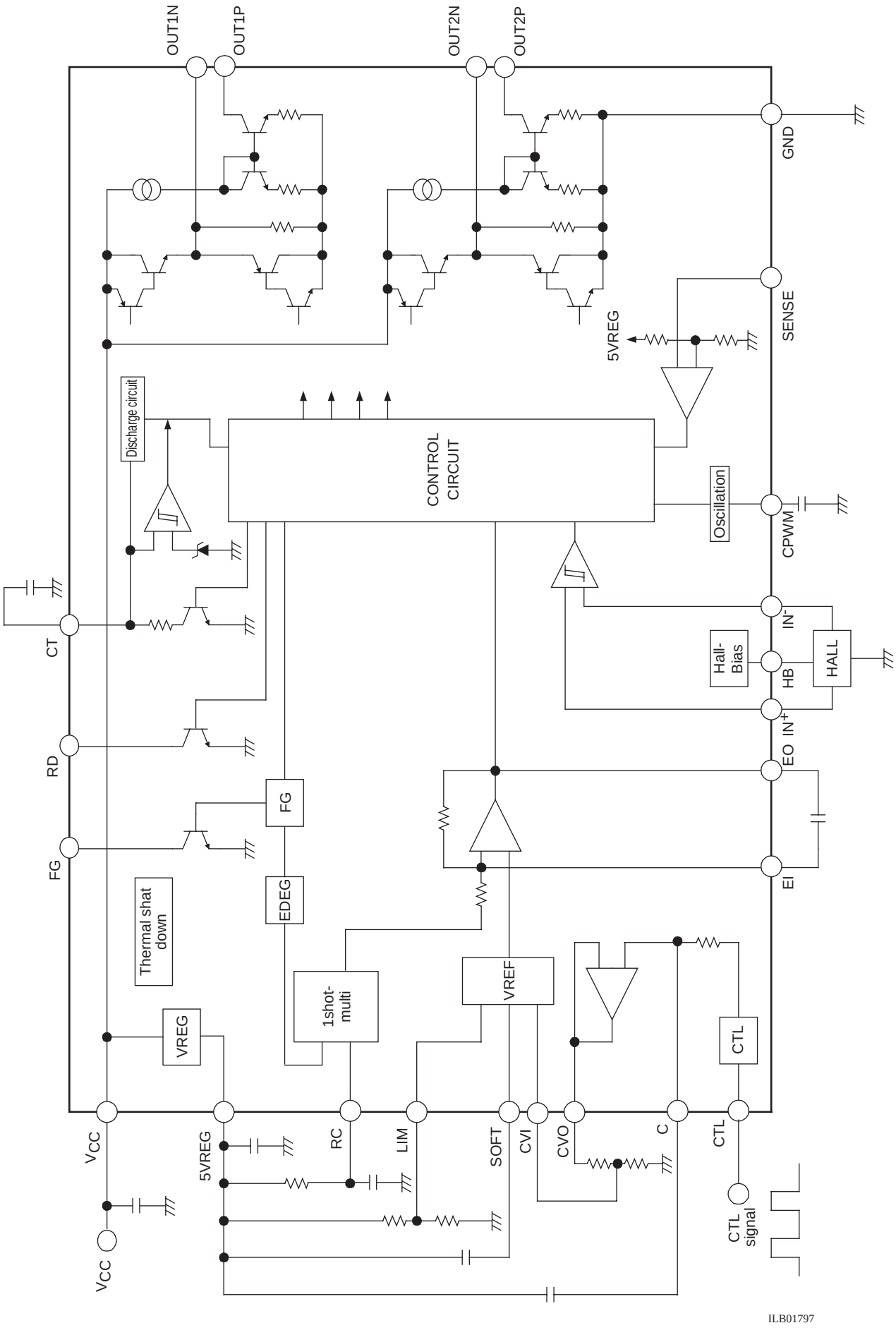
Lock protection CPWM = H

IN^-	IN^+	CT	OUT1P	OUT1N	OUT2P	OUT2N	FG	Mode
H	L	L	L	L	OFF	H	L	OUT1→2 drive
L	H		OFF	H	L	L	OFF	OUT2→1 drive
H	L	H	OFF	L	OFF	H	L	Lock protection
L	H		OFF	H	OFF	L	OFF	

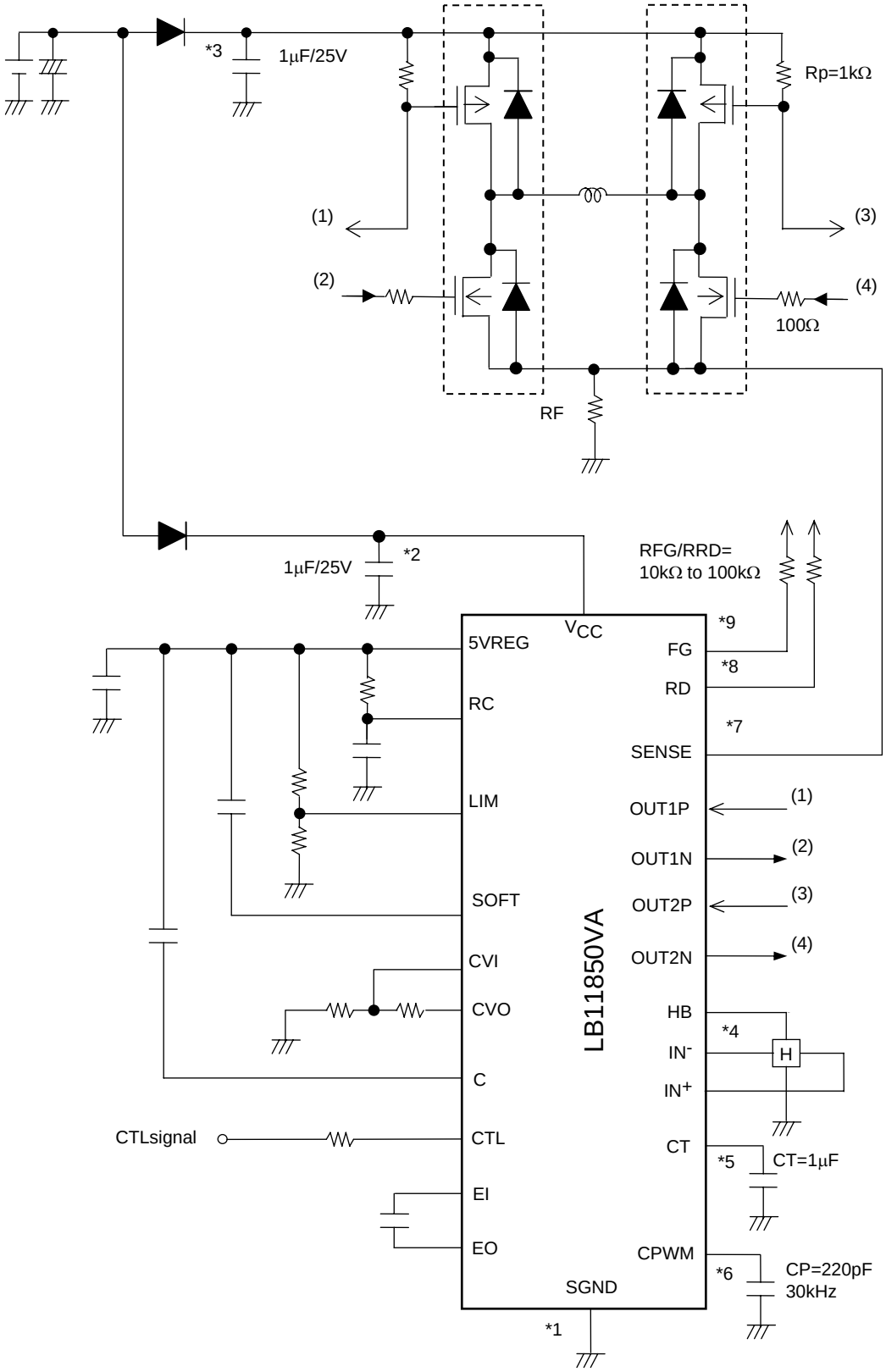
Speed control CT = L

EO	CPWM	IN^-	IN^+	OUT1P	OUT1N	OUT2P	OUT2N	Mode
L	H	H	L	L	L	OFF	H	OUT1→2 drive
		L	H	OFF	H	L	L	OUT2→1 drive
H	L	H	L	OFF	L	OFF	H	Regeneration mode
		L	H	OFF	H	OFF	L	

Block Diagram



Sample Application Circuit



Description of Pre-driver Block

*1: <Power supply-GND wiring>
SGND is connected to the control circuit power supply system.

*2: <Power stabilization capacitor>
For the signal-side power stabilization capacitor, the capacitance of more than 0.1μF is used.
Connect the capacitor between V_{CC} and GND with the thick pattern and along the shortest route.

*3: <Power-side power stabilization capacitor>
For the power-side power stabilization capacitor, the capacitance of more than 0.1μF is used.
Connect the capacitor between power-side power supply and GND with the thick pattern and along the shortest route.

*4: <IN^+, IN^- pins>
Hall signal input pins
Wiring needs to be short to prevent carrying noise. If noise is carried, insert a capacitor between IN^+ and IN^-. The Hall input circuit is a comparator having a hysteresis of 15mV.
It has a ±30mV (input signal difference voltage) soft switch zone.
It is recommended that the Hall input level is 100mV (p-p) at the minimum.

*5: <CPWM pin>
This is the pin to connect capacitor for generating the PWM basic frequency
Use of CP = 220pF produces oscillation at the frequency of 30kHz which serves as the PWM basic frequency.
Since this pin is also used for the current limiter reset signal, the capacitor must be connected without fail even when no speed control is implemented.

*6: <CT pin>
This is the pin to connect capacitor for lock detection
Constant-current charging and constant-current discharging circuits are incorporated. When the pin voltage becomes 3.0V, the safety lock is applied, and when it lowers to 1.0V, the lock protection is reset.
Connect this pin to GND when it is not in use (when lock protection is not required).

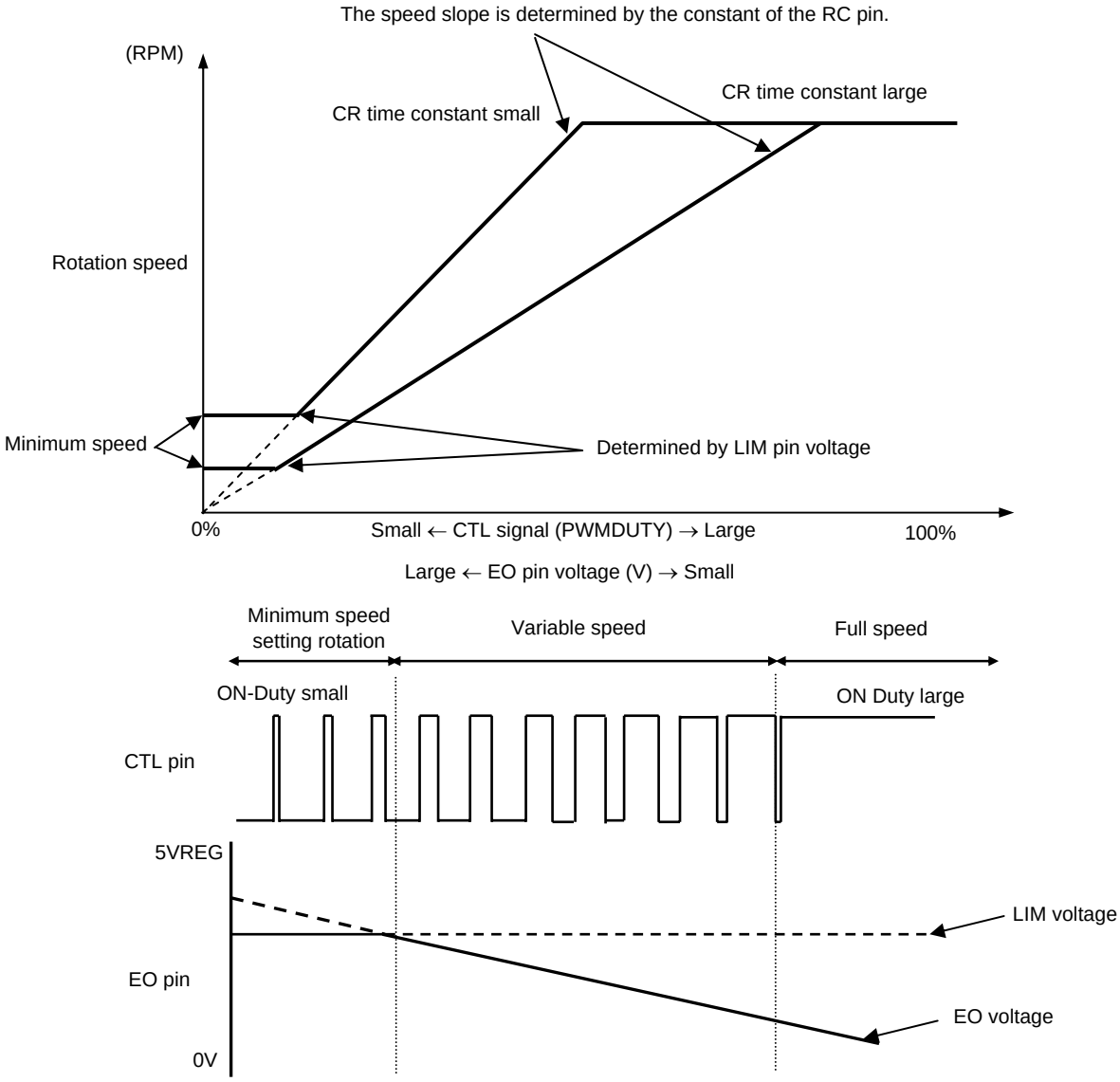
*7: <SENSE pin>
This is the pin for current limiter detection
When the pin voltage exceeds 0.21V, current limiting is applied, and the low-side regeneration mode is established.
Connect this pin to GND when it is not in use.

*8: <RD pin>
Lock detection pin
This is the open collector output, which outputs “L” during rotation and “H” at stop. This pin is left open when it is not in use.

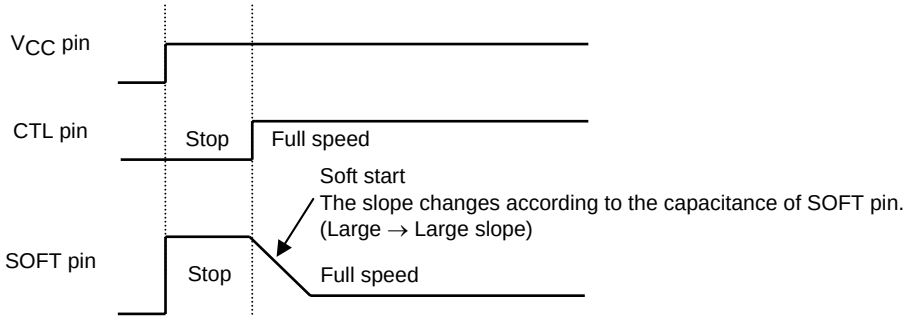
*10: <FG pin>
Speed detection pin.
This is the open collector output, which can detect the rotation speed using the FG output according to the phase change. This pin is left open when it is not in use.

Description of Speed Control Block

1) Speed control diagram

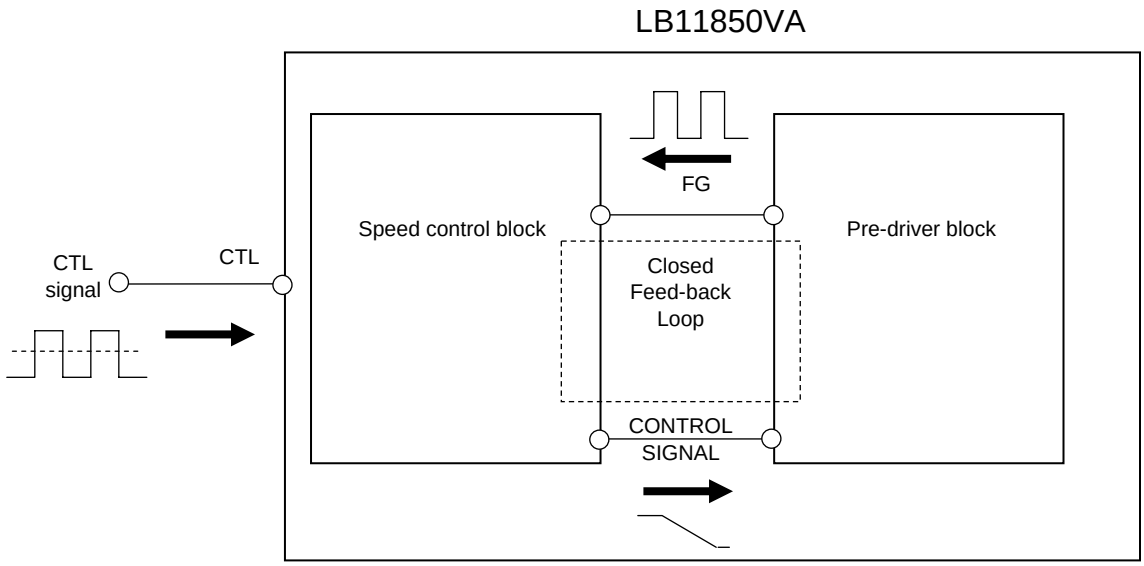


2) Timing at startup (soft start)

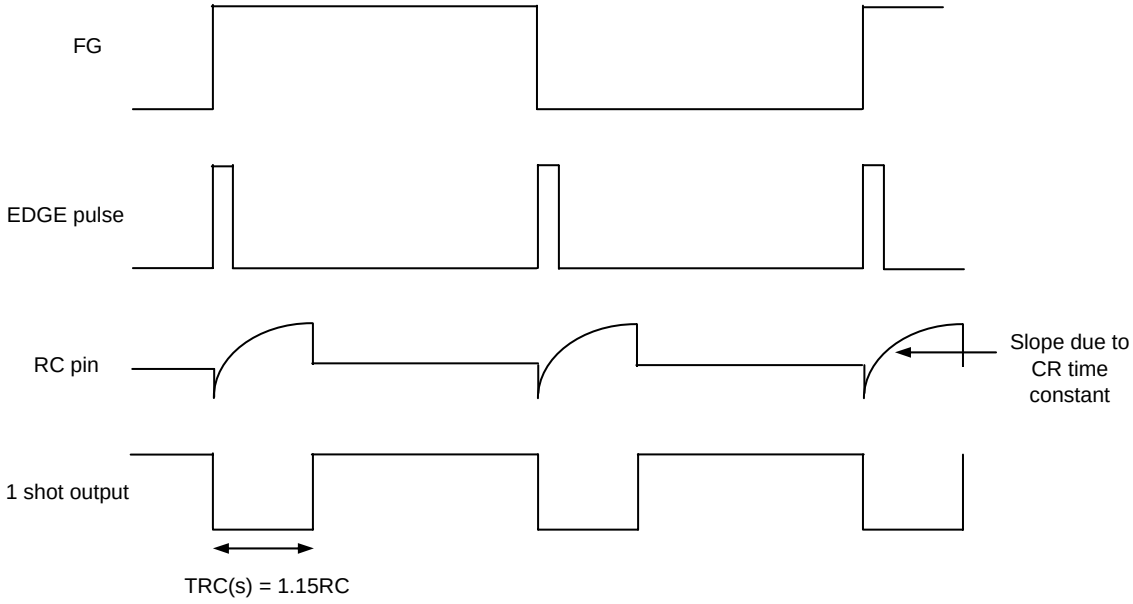


3) Additional description of operations

The LB11850 forms a feedback loop inside the IC so that the FG period (motor speed) corresponding to the control voltage is established by inputting the duty pulse.



The operation inside the IC is as follows. Pulse signals are created from the edges of the FG signals as shown in the figure below, and a waveform with a pulse width which is determined by the CR time constants and which uses these edges as a reference is generated by a one-shot multivibrator.
These pulse waveforms are integrated and the duty ratio of the pre-driver output is controlled as a control voltage.

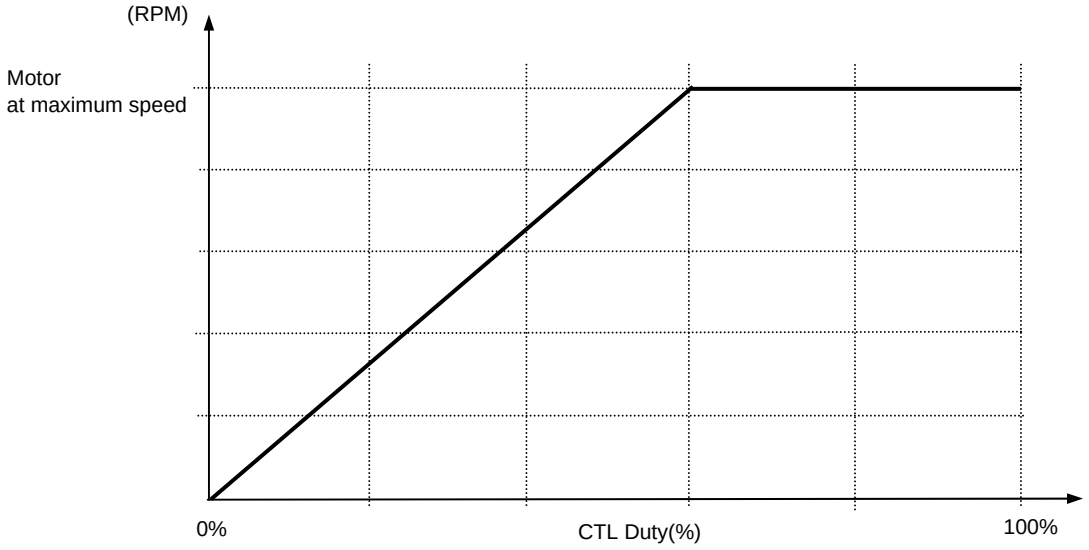


Furthermore, by changing the pulse width as determined by the CR time constant, the VCTL versus speed slope can be changed as shown in the speed control diagram of the previous section.
However, since the pulses used are determined by the CR time constant, the variations in CR are output as-is as the speed control error.

4) Procedure for calculating constants

<RC pin>

The slope shown in the speed control diagram is determined by the constant of the RC pin.



(1) Obtain FG signal frequency fFG (Hz) of the maximum speed of the motor.
(With FG2 pulses per rotation)
fFG (Hz) = 2 rpm/60 .... <1>

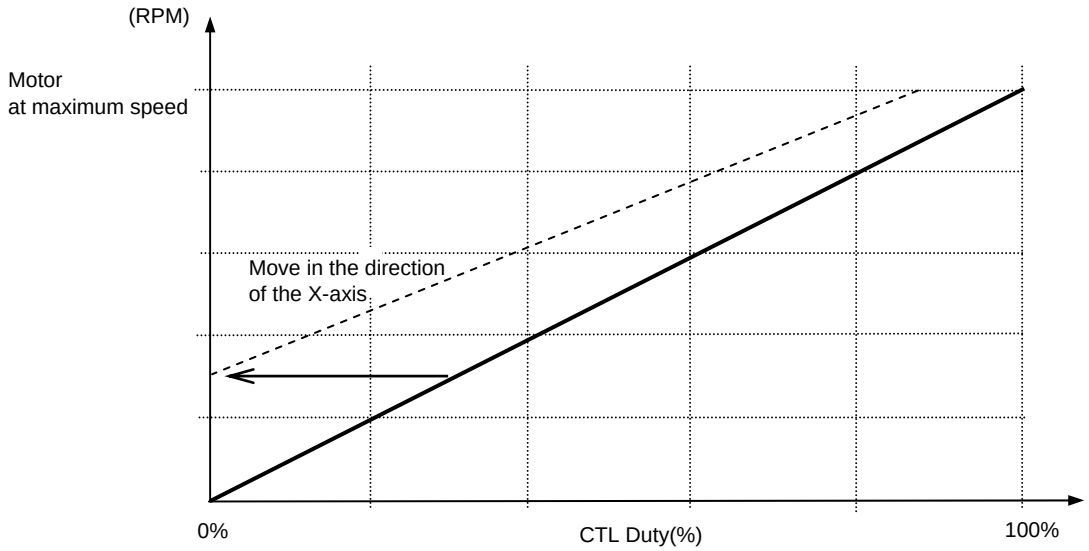
(2) Obtain the time constant which is connected to the RC pin.
(Have "DUTY" (example: 100% = 1.0, 60% = 0.6) serve as the CTL duty ratio at which the maximum speed is to be obtained.)
R×C = DUTY/(3.3×1.1×fFG) .... <2>

(3) Obtain the resistance and capacitance of the capacitor.
Based on the discharge capacity of the RC pin, the capacitance of the capacitor which can be used is 0.01 to 0.015μF. Therefore, find the appropriate resistance using equation <3> or <4> below from the result of <2> above.
R = (R×C)/0.01μF .... <3>
R = (R×C)/0.015μF .... <4>

The temperature characteristics of the curve are determined by the temperature characteristics of the capacitor of the RC pin. When temperature-caused fluctuations in the speed are to be minimized, use a capacitor with good temperature characteristics.

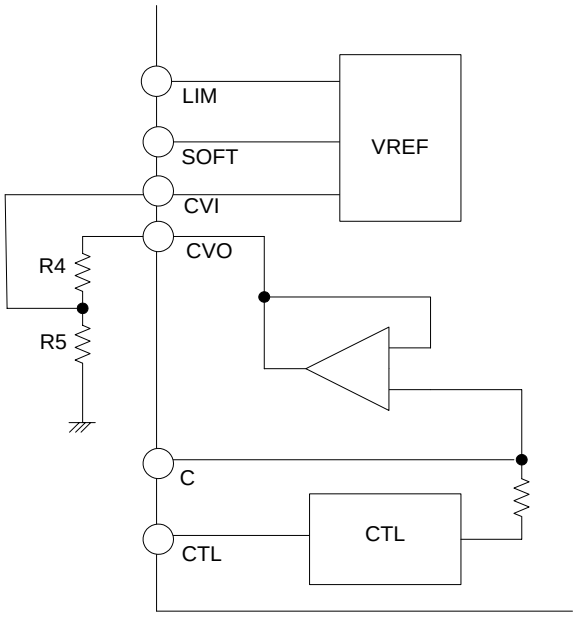
<CVO, CVI pins>
These pins determine the position of the slope origin. (When the origin point is at (0%, 0 rpm), CVO and CVI are shorted.)

(1) Movement along the X-axis (resistance divided between CVO and GND)

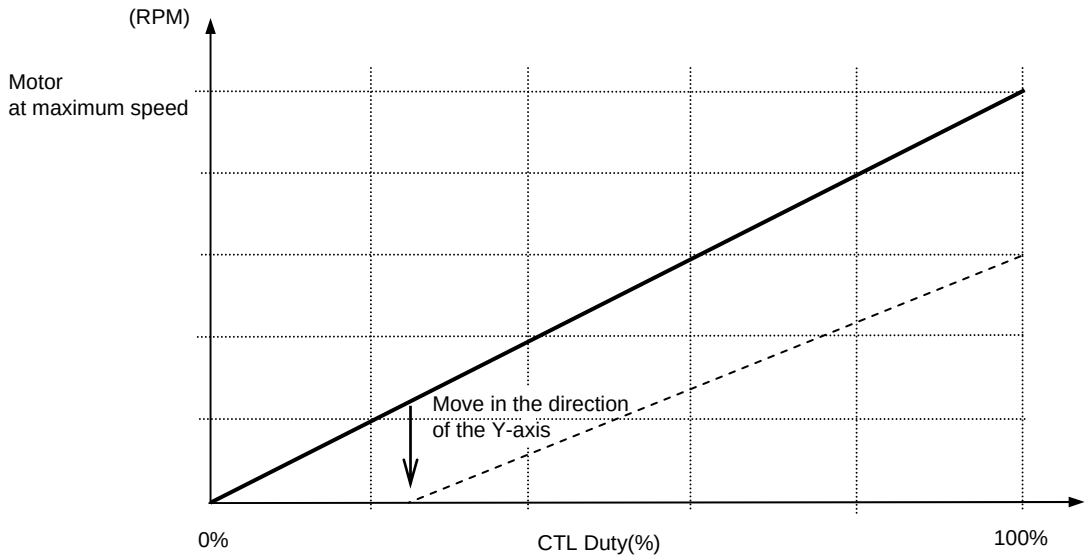


(Example) In the case where the characteristics change from ones with the origin point (0%, 0 rpm) to ones where the speed at a duty ratio of 30% becomes the speed at 0%:
First, obtain the input voltage of the CVI pin required at 0%.
CVI = 5-(3×duty ratio) = 5-(3×0.3) = 5-0.9 = 4.1V

Next, obtain the resistances at which the voltage becomes 4.1V by dividing the resistance between CVO and GND when CVO is 5V. The ratio of CVO-CVI: CVI-GND is 0.9V: 4.1V = 1: 4.5.
Based on the above, the resistance is 20kΩ between CVO and CVI and 91kΩ between CVI and GND.
Furthermore, the slope changes. (In the case of the example given, since the resistance ratio is 1: 4.5, the slope is now 4.5/5.5 = 0.8 times what it was originally.)
If necessary, change the resistance of the RC pin, and adjust the slope.

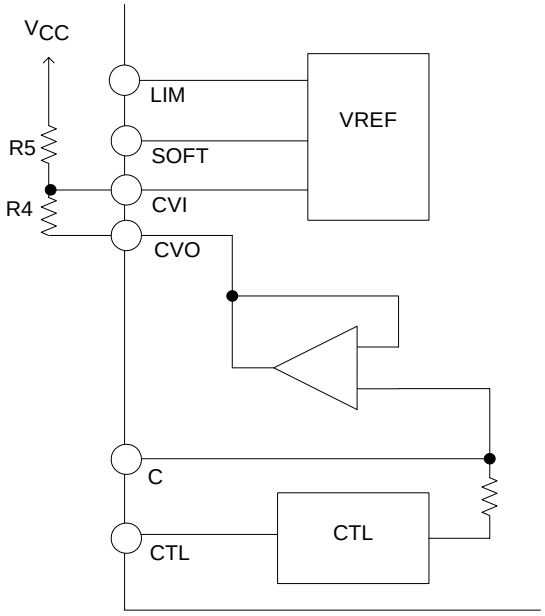


(2) Movement along the Y-axis (resistance divided between CVO and V_{CC})

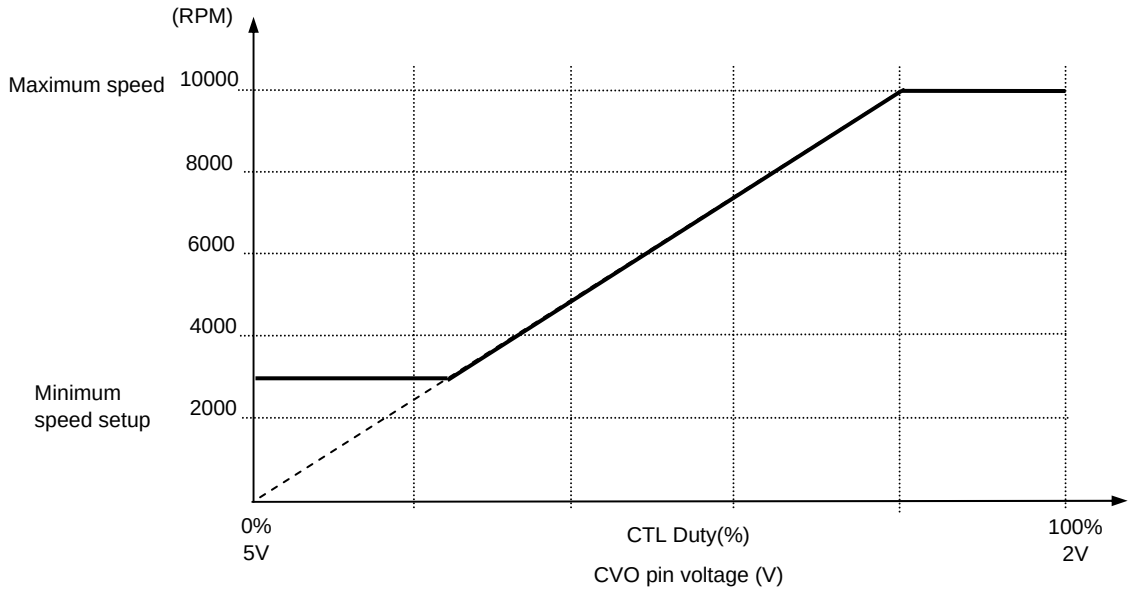


(Example) In the case where the characteristics change from ones with the origin point (0%, 0 rpm) to ones where the speed at a duty ratio of 25% becomes 0 rpm:
First, obtain the CVO pin voltage required for the CVI voltage to be 5V at 25%.
CVO = 5-(3×duty ratio) = 5-(3×0.25) = 5-0.75 = 4.25V

With CVO = 4.25V, find the resistances at which CVI = 5V.
The ratio of CVO-CVI: CVI-GND is 0.75V: 7V = 1: 9.3
Based on the above, the resistance is 20kΩ between CVO and CVI and 180kΩ between CVI and V_{CC}.
(Due to the current capacity of the CVO pin, the total resistance must be set to 100kΩ or more.)
Furthermore, the slope changes. (In the case of the example given, since the resistance ratio is 1: 9.3, the slope is now 9.3/10.3 = 0.9 times what it was originally.)
If necessary, change the resistance of the RC pin, and adjust the slope.



<LIM pin>
The minimum speed is determined by the voltage of the LIM pin.

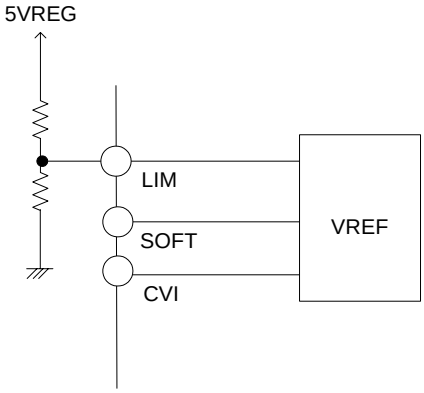


(1) Obtain the ratio of the minimum speed required to the maximum speed.
Ra = Minimum speed/maximum speed .... <1>
In the example shown in the figure above, Ra = minimum speed/maximum speed = 3000/10000 = 0.3.

(2) Obtain the product of the duty ratio at which the maximum speed is obtained and the value in equation <1>.
Ca = Duty ratio at maximum speed×Ra .... <2>
In this example, Ca = duty ratio at maximum speed×Ra = 0.8×0.3 = 0.24.

(3) Obtain the required LIM pin voltage.
LIM = 5-(3×Ca) .... <3>
In this example, LIM = 5-(3×Ca) = 5-(3×0.24) ≈ 4.3V.

(4) Divide the resistance of 5VREG, and generate the LIM voltage.
In this example, the voltage is 4.3V so the resistance ratio is 1: 6.
The resistance is 10kΩ between 5VREG and LIM and 62kΩ between LIM and GND.



<C pin>

In order to connect a capacitor capable of smoothing the pin voltage to the C pin, the correlation given in the following equation must be satisfied when f (Hz) serves as the input signal frequency of the CTL pin. (R is contained inside the IC, and is 180kΩ (typ.).)

$1/f = t < CR$

The higher the capacitance of the capacitor is, the slower the response to changes in the input signal is.