



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

Monolithic Linear IC

LA6571 — 5CH Driver for Mini Disk and Compact Disk

Overview

The LA6571 is 5-channel driver for mini disk and compact disk applications (BTL-AMP: 5CH).

Features

- Power amplifier 5-channel built-in.
- I_O max 1A
- Level shift circuit built-in.
- Mute circuit (output ON/OFF) with three built-in channels (2-2-1).
(Operates independently for each of MUTE1: CH1 and 2, MUTE2: CH3 and 4, and MUTE3: CH5.
Not operating for the regulator (REG))
- Regulator (REG) built-in (external PNP transistor).
Voltage setting (typ: 1.5V or more) with an external resistor
- Overheat protection circuit (thermal shutdown) built-in.

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Maximum output current	I_O max	Each output for channel 1 to 5.	1	A
Maximum input voltage	V_{INB}		13	V
MUTE pin voltage	V_{MUTE}		13	V
Allowable loss	P_d max	Independent IC	0.8	W
		Mounted on a specified board*	2	W
Operating temperature	T_{opr}		-30 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* Mounted on a specified board: 76.1mm×114.3mm×1.6mm glass epoxy

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC1}		4.5 to V_{CC2}	V
Supply voltage 2	V_{CC2}		6 to 13	V

■ Any and all SANYO Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO Semiconductor representative nearest you before using any SANYO Semiconductor products described or contained herein in such applications.

■ SANYO Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor products described or contained herein.

SANYO Semiconductor Co., Ltd.

<http://semicon.sanyo.com/en/network>

LA6571

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC1} = 5\text{V}$, $V_{CC2} = 12\text{V}$, $V_{REF-IN} = 1.65\text{V}$, unless especially specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[ALL Blocks]						
No-load current drain ON	$I_{CC\ ON}$	All outputs ON *1		30	50	mA
No-load current drain OFF	$I_{CC\ OFF}$	All outputs OFF *1		10	20	mA
VREF input voltage range	V_{REF-IN}		1		$V_{CC2}-1$	V
Thermal shutdown temperature	TSD	*7	150	175	200	$^\circ\text{C}$
[BTL AMP Block] (CH1 to CH5)						
Output offset voltage	V_{OFF}	Voltage difference in output between BTL AMP and each channel.	-50		50	mV
Output offset voltage	V_{OFF1}	Voltage difference in output between BTL AMP and each channel.	-80		80	mV
Output voltage	V_O	CH1,CH2 *3	3.2	4.0		V
Output voltage	V_{O1}	CH3,CH4,CH5 *4	9.7	10.5		V
Closed-circuit voltage gain	V_G1	Gain between input and output for CH1, CH2, and CH5 *2	4.2	5.0	6.0	times
Closed-circuit voltage gain	V_G3	Gain between input and output for CH3 and CH4 *2	8.2	9.0	11.0	times
Slew rate	SR	AMP Independent. Multiply 2 between outputs. *7		0.5		$\text{V}/\mu\text{s}$
MUTE ON voltage	$V_{MUTE\ ON}$	Each MUTE *6	2			V
MUTE OFF voltage	$V_{MUTE\ OFF}$	Each MUTE *6			0.5	V
[Input AMP Block]						
Input voltage range	$V_{IN\ op}$		0		$V_{CC2}-1.5$	V
Output offset voltage	$V_{OFF\ op}$		-10		10	mV
Output current (SINK)	SINK op		2			mA
Output current (SOURCE)	SOURCE op	*5	300	500		μA
[Power Supply Block] (PNP transistor: 2SB632K)						
Regulator output	V_{OUT}	For error Amp, $R_L = 10\text{k}\Omega$ at buffer	1.2	1.3	1.4	V
REG-IN SINK current	REG-IN-SINK	Base current to external PNP	5	10		mA
Line regulation	ΔV_{OLN}	$6\text{V} \leq V_{CC} \leq 12\text{V}$, $I_O = 200\text{mA}$		20	150	mV
Load regulation	ΔV_{OLD}	$5\text{mA} \leq I_O \leq 200\text{mA}$		50	200	mV

*1. Current dissipation that is a sum of V_{CC1} and V_{CC2} at no load.

*2. Input AMP is a BUFFER AMP.

*3. Voltage difference between both ends of load (8Ω). Output saturated.

*4. Voltage difference between both ends of load (12Ω). Output saturated.

*5. The source of input OP-AMP is a constant current. (See the specified block diagram.)

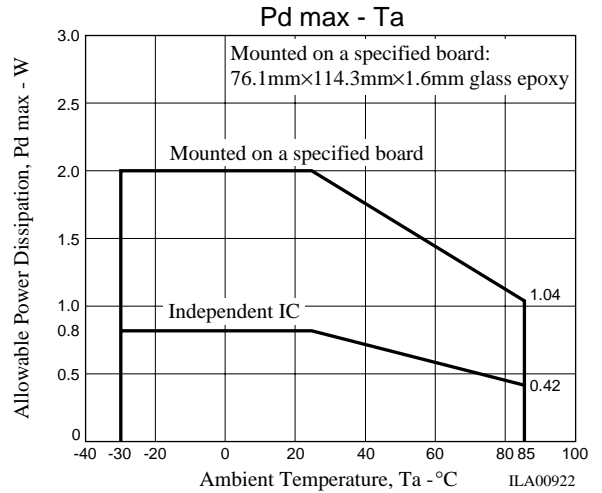
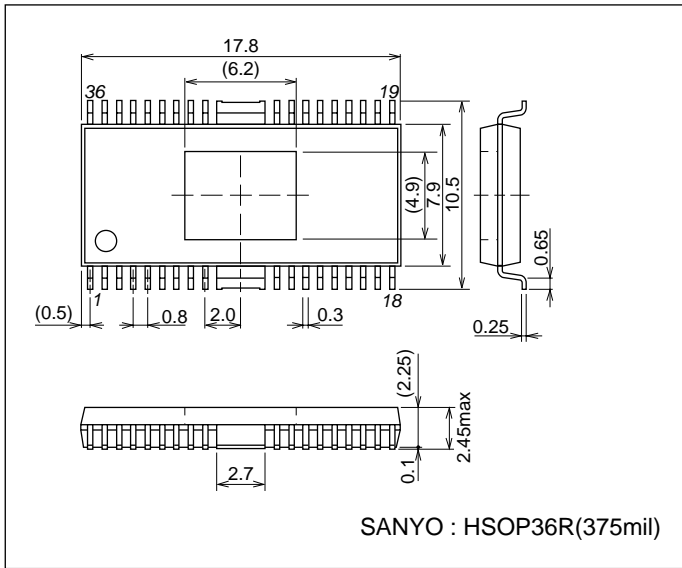
As the $11\text{k}\Omega$ resistance to the next stage is a load, pay due attention when setting the input OP-AMP gain.

*6. Output ON with MUTE: [H] and OFF with MUTE: [L] (HI impedance).

*7. Design guarantee value

Package Dimensions

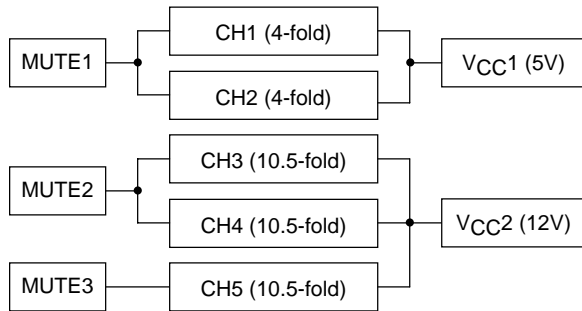
unit : mm
3251



Pin Description

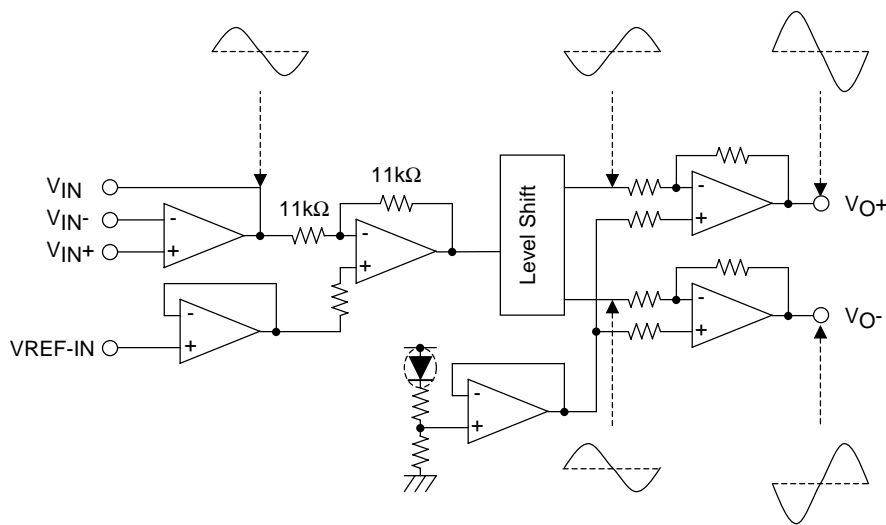
Pin Name	Pin Name	Pin No.	Equivalent Circuit Diagram	Description
Input	VIN1+ VIN1- VIN1 VIN2+ VIN2- VIN2 VIN3+ VIN3- VIN3 VIN4+ VIN4- VIN4 VIN5+ VIN5- VIN5	17 16 15 20 19 18 23 22 21 30 29 31 32 33 34		Each input pin
Output	VO1+ VO1- VO2+ VO2- VO3+ VO3- VO4+ VO4- VO5+ VO5-	12 13 10 11 8 9 6 7 5 4		Each output
MUTE	MUTE1 MUTE2 MUTE3	1 2 36		Turns ON/OFF the output for MUTE1: CH1, 2 MUTE2: CH3, 4, and MUTE3: CH5. Each MUTE operates independently. MUTE: H output ON MUTE: L output OFF With the output OFF, the output has a high impedance.

Relationship between MUTE and Power (VCC)

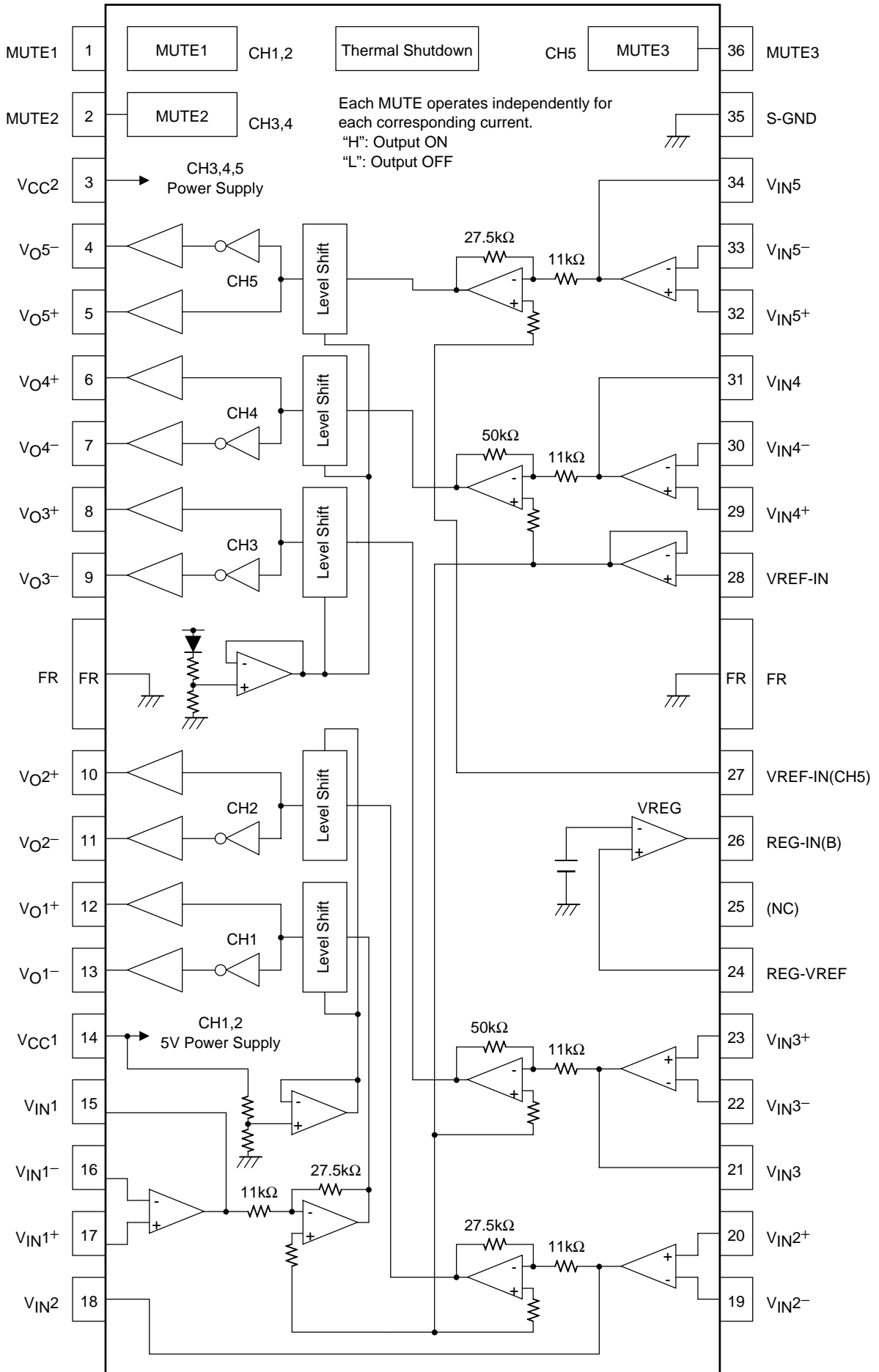


* MUTE operates independently for each corresponding channel.

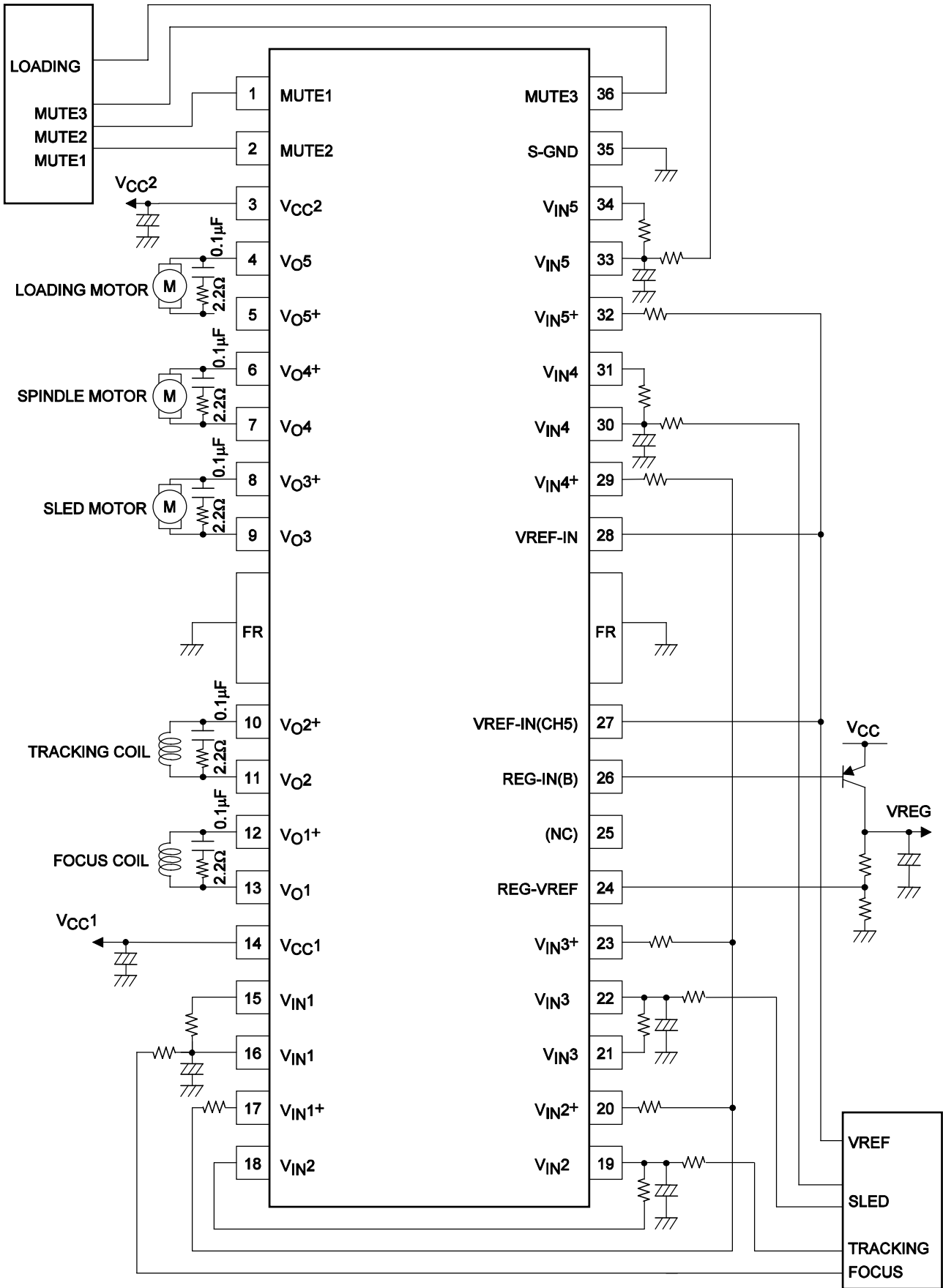
Schematic Diagram of I/O Related Components



Block Diagram



Sample Application Circuit



- Specifications of any and all SANYO Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Semiconductor Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Semiconductor Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of April, 2006. Specifications and information herein are subject to change without notice.