

SANYO	No.1958A	LA6083D
		J-FET Input Dual Operational Amplifier

The LA6083D is a J-FET input dual operational amplifier. Application areas include general-purpose control equipment, measuring equipment (very low current measurement, long-integrating circuit, sample & hold circuit, impedance converter, etc.).

Features

- . High slew rate
- . High input impedance
- . Low input bias current
- . Low input offset current
- . No phase compensation required
- . With offset null pins

Maximum Ratings at Ta=25°C

			unit
Maximum Supply Voltage	V_{CC}/V_{EE}	± 18	V
Differential Input Voltage	V_{ID}	± 30	V
Common-Mode Input Voltage	V_{IN} (Note)	± 15	V
Allowable Power Dissipation	P_d max	720	mW
Operating Temperature	T_{opr}	-30 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C

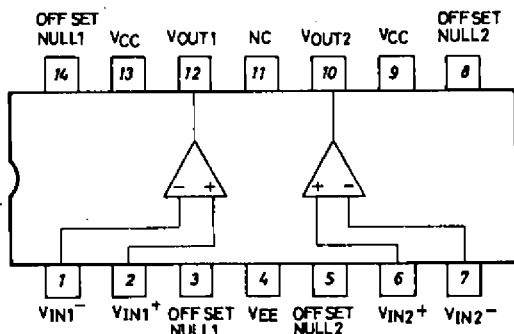
(Note) Allowable in the range of supply voltage. The above value is for $V_{CC}=+15V, V_{EE}=-15V$.

Operating Characteristics at Ta=25°C, $V_{CC}=+15V, V_{EE}=-15V$

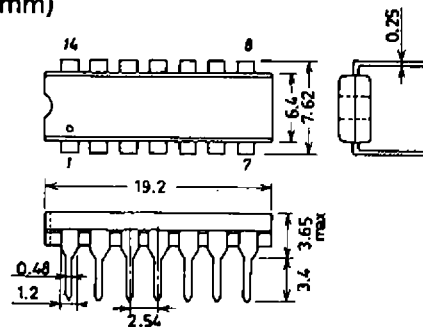
			min	typ	max	unit
Input Offset Voltage	V_{IO}	$R_S=50\text{ohms}$		5.0	15.0	mV
Input Offset Current	I_{IO}			5	200	pA
Input Bias Current	I_B			30	400	pA
Common-Mode Input Voltage Range	V_{ICM}		± 10			V
Common-Mode Rejection Ratio	CMR		70	76		dB
Large Amplitude Voltage Gain	VG	$R_L \geq 2\text{kohms}, V_o = \pm 10V$	25	200		V/mV
Maximum Output Voltage	V_{opp1}	$R_L \geq 10\text{kohms}$	± 12	± 13.5		V
	V_{opp2}	$R_L \geq 2\text{kohms}$	± 10	± 12		V

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Pin Assignment



Package Dimensions 3003A-D14IC (unit : mm)



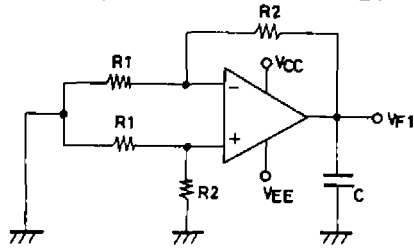
SANYO: DIP14

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			min	typ	max	unit
Supply Voltage Rejection Ratio	SVR		70	76		dB
Supply Current	I_{CC}	$R_L = \infty$		4	5.6	mA
Gain-Bandwidth Product	f_T	$A_V = 1$		3		MHz
Equivalent Input Noise Voltage	V_{NI}	$R_S = 100\text{ohms}$, $f = 10\text{Hz to } 10\text{kHz}$		4		μVrms
Input Resistance	r_i			10^{12}		ohm
Channel Separation	oh sep			120		dB
Slew Rate	S·R	$R_L = 2\text{kohms}$, $C_L = 100\text{pF}$, $A_V = 1$, $V_{IN} = 10\text{V}$		13		V/us

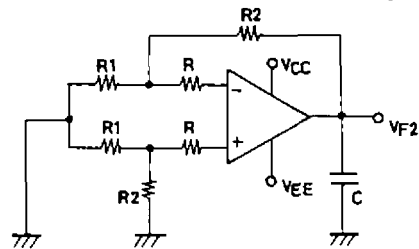
Test Circuits

1. Input Offset Voltage V_{IO}



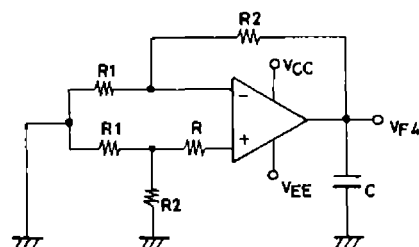
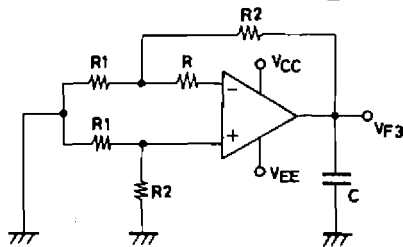
$$V_{IO} = \frac{V_{F1}}{1 + R2/R1}$$

2. Input Offset Current I_{IO}



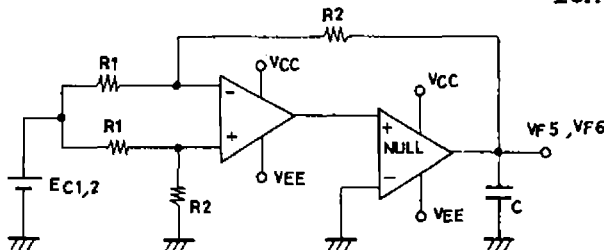
$$I_{IO} = \frac{V_{F2} - V_{F1}}{R(1 + R2/R1)}$$

3. Input Bias Current I_B



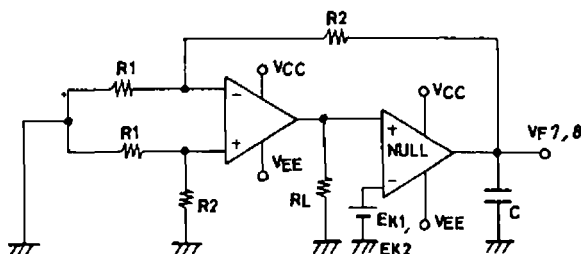
$$I_B = \frac{V_{F4} - V_{F3}}{2R(1 + R2/R1)}$$

4. Common-Mode Rejection Ratio CMR
Common-Mode Input Voltage Range V_{ICM}



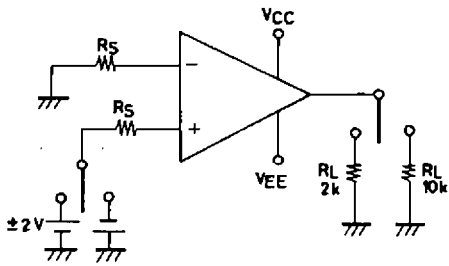
$$CMR = 20 \log \left| \frac{(E_{C1} - E_{C2})(1 + R2/R1)}{V_{F5} - V_{F6}} \right|$$

5. Voltage Gain V_G



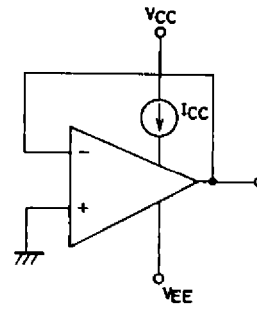
$$V_G = \frac{(E_{K1} - E_{K2})(1 + R2/R1)}{V_{F8} - V_{F7}}$$

6. Maximum Output Voltage V_{opp}

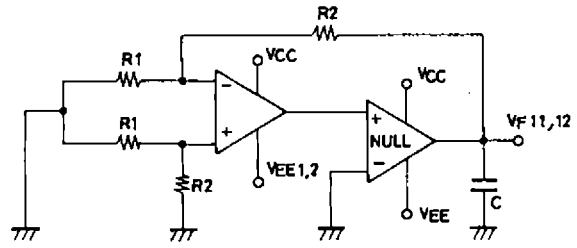
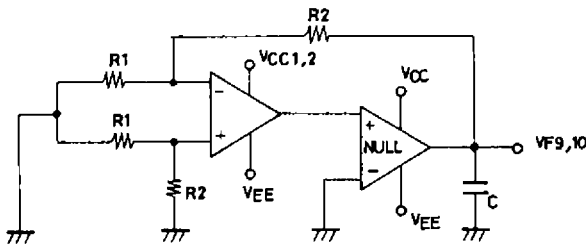


Unit (resistance: Ω)

7. Supply Current I_{CC}



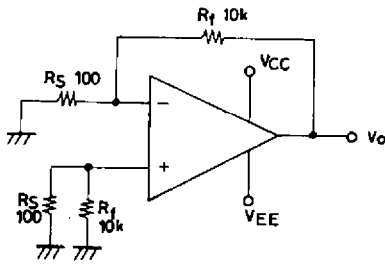
8. Supply Voltage Rejection Ratio SVR



$$SVR (+) = 20 \log \left| \frac{(1 + R2/R1) (V_{CC1} - V_{CC2})}{V_{F9} - V_{F10}} \right|$$

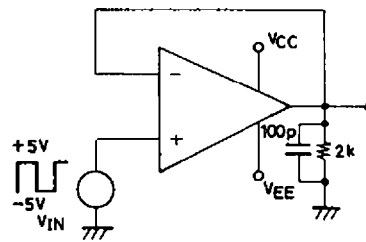
$$SVR (-) = 20 \log \left| \frac{(1 + R2/R1) (V_{EE1} - V_{EE2})}{V_{F11} - V_{F12}} \right|$$

9. Equivalent Input Noise Voltage V_{NI}



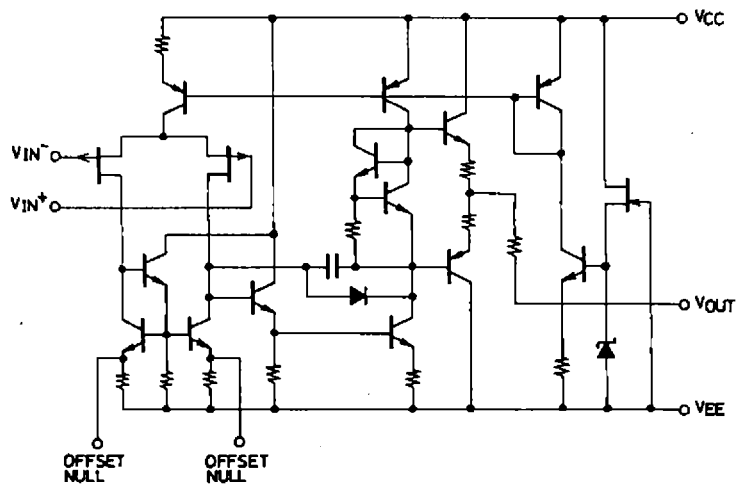
$$V_{NI} = \frac{V_o}{100}$$

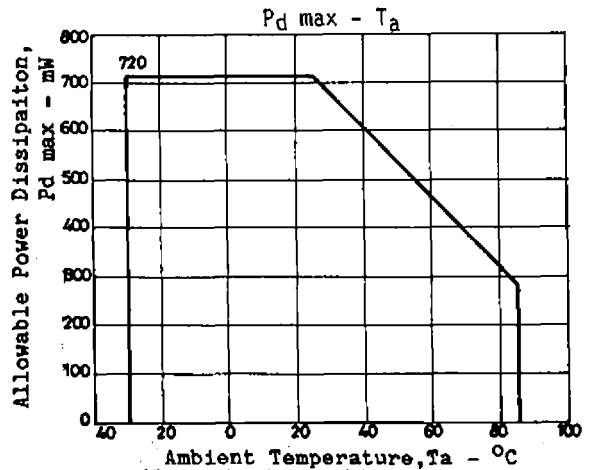
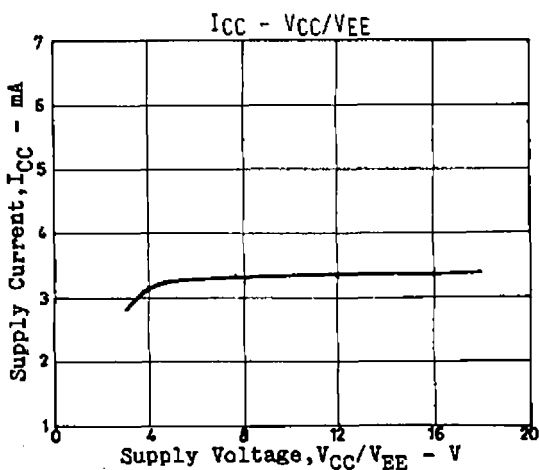
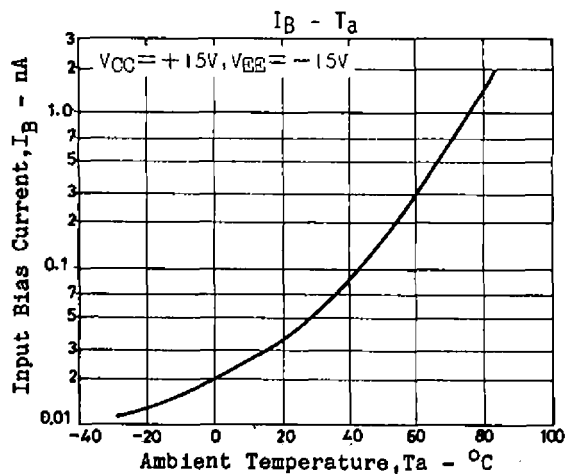
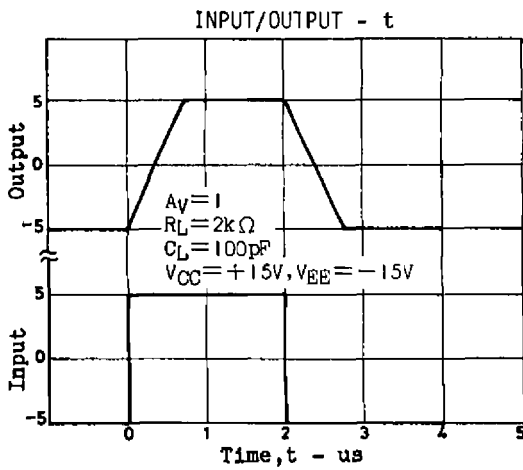
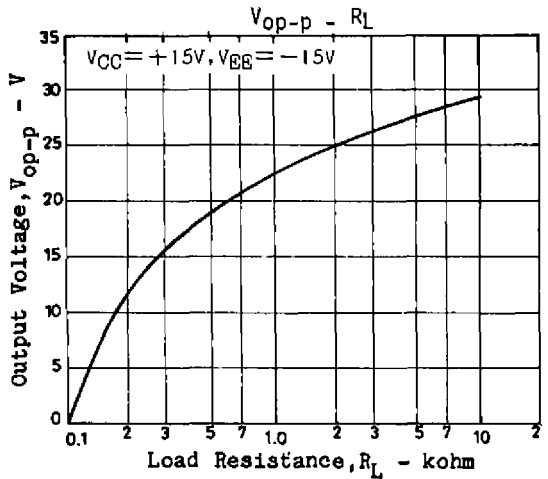
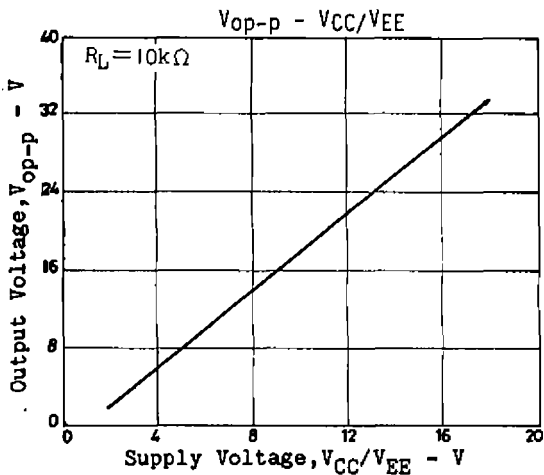
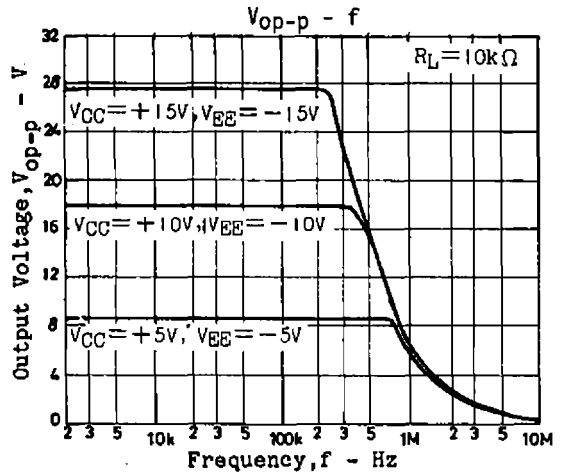
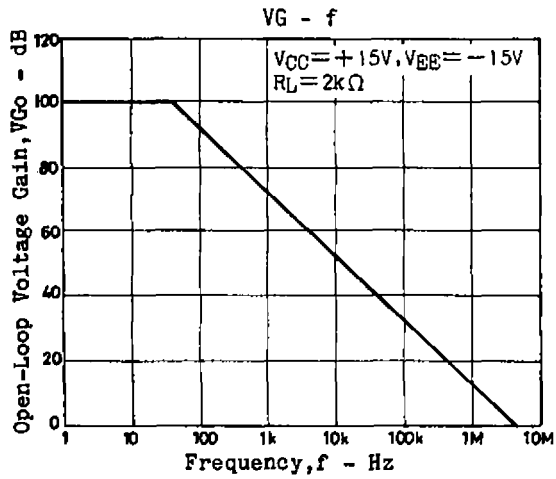
10. Slew Rate SR



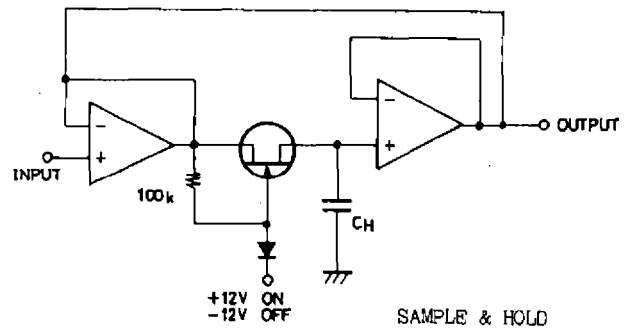
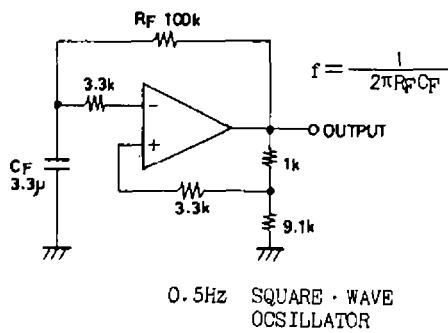
Unit (resistance: Ω capacitance: F)

Equivalent Circuit



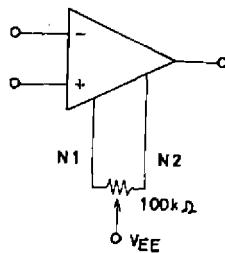


Sample Application Circuits



Unit (resistance:Ω capacitance:F)

Voltage offset adjust circuit



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