Ordering number: EN5376

Monolithic Linear IC

LA5314

Variable Divided Voltage Generator for LCD Use

Overview

The LA5314 is a valiable diveded voltage generator IC for multiple drive of LCD matrix.

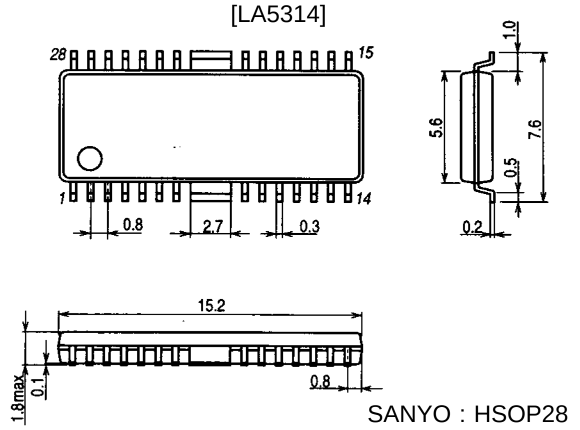
Features

- Power supply for variable bias LCD matrix. (1/5 to 1/20 bias available by built-in resistances)
- Five operational amplifiers to deliver 5 voltage outputs
- Low current drain (1.6 mA typ)
- Miniflat package for miniturization

Package Dimensions

unit : mm

3222-HSOP28



Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	$V_{CC} - V_{EE}$	38	V
Maximum output current	I_{OUT} max	V0 to V4	*±25	mA
Allowable power dissipation	Pd max		600	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–30 to +150	°C

Note: 1. Continuous operation (non breakdown) is guaranteed when operated at the maximum ratings shown above.
2. *The maximum output current is a value specified under the conditions otherwise specified separately.

Operating Conditions at Ta = 25°C

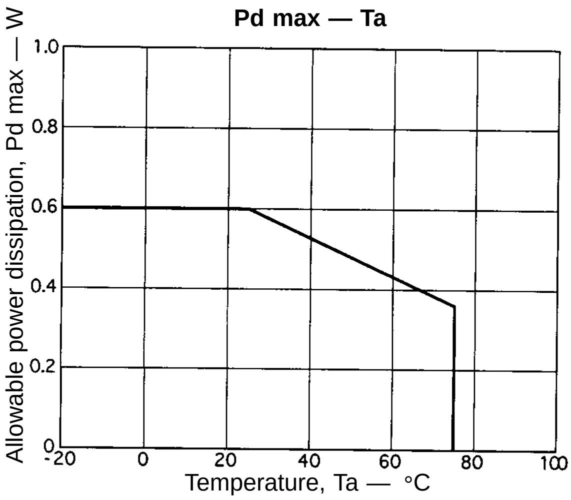
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}	$V_{CC} - V_{EE}$	10 to 35	V
Output current	$I_{OUT}0, 1$	V0, V1	–0.5 to +10	mA
	$I_{OUT}2, 3$	V2, V3	–10 to +10	mA
	$I_{OUT}4$	V4	–15 to +0.5	mA

Note: 3. Set V_{CC} and V_{EE} so that |V0–V1| and |V4| become 1V or greater.

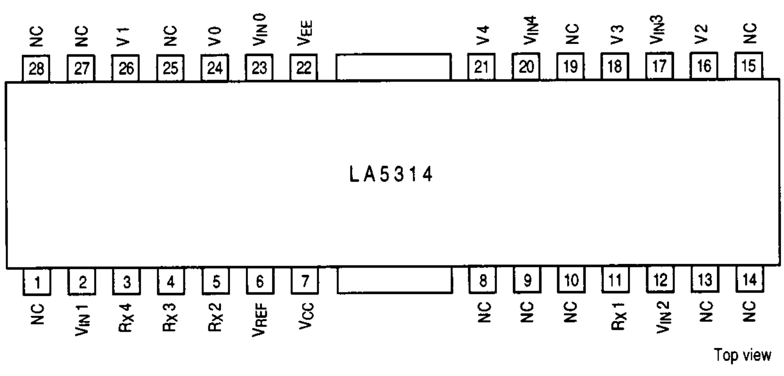
Operating Chararcteristics at Ta = 25°C, $V_{CC} - V_{EE}$ = 20 V, $V_{REF} = V_{CC}$, R_X = 8R

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I_{CC}, I_{EE}	V_{CC}, V_{EE}:$V_{CC} - V_{EE}$ = 20 V, R_X = 8R		1.6	3	mA
Output voltage difference 1	Vd1	(V0 – V1) – (V1 – V2)	–30		+30	mV
Output voltage difference 2	Vd2	(V3 – V4) – (V4 – V_{EE})	–30		+30	mV
Output voltage ratio 1	Rb1	V0/(V0 – V1)	11.64	12.00	12.36	—
Output voltage ratio 2	Rb2	V0/(V0 – V2)	5.82	6.00	6.18	—
Output voltage ratio 3	Rb3	V0/V3	5.82	6.00	6.18	—
Output voltage ratio 4	Rb4	V0/V4	11.64	12.00	12.36	—
Internal resistnace ratio 1	8R	$R_X1 - R_X2$*		8		—
Internal resistance ratio 2	12R	$R_X1 - R_X3$*		12		—
Internal resistance ratio 3	14R	$R_X1 - R_X4$*		14		—
Internal resistance ratio 4	15R	$R_X1 - V_{IN}3$*		15		—
Resistance	R	R value when 0.6 V is applied across $R_X5 - R_X6$: $R_X5 - R_X6$		20		kΩ
Load regulation 1	ΔV0	V0: –0.2 mA < $I_{OUT}0$ < +10.0 mA	–20		+20	mV
Load regulation 2	ΔV1	V1: –0.2 mA < $I_{OUT}1$ < +10.0 mA	–20		+20	mV
Load regulation 3	ΔV2	V2: –10.0 mA < $I_{OUT}2$ < +10.0 mA	–20		+20	mV
Load regulation 4	ΔV3	V3: –10.0 mA < $I_{OUT}3$ < +10.0 mA	–20		+20	mV
Load regulation 5	ΔV4	V4: –10.0 mA < $I_{OUT}4$ < +0.2 mA	–20		+20	mV

Note* : Referenced to R between R_X4 and $V_{IN}3$

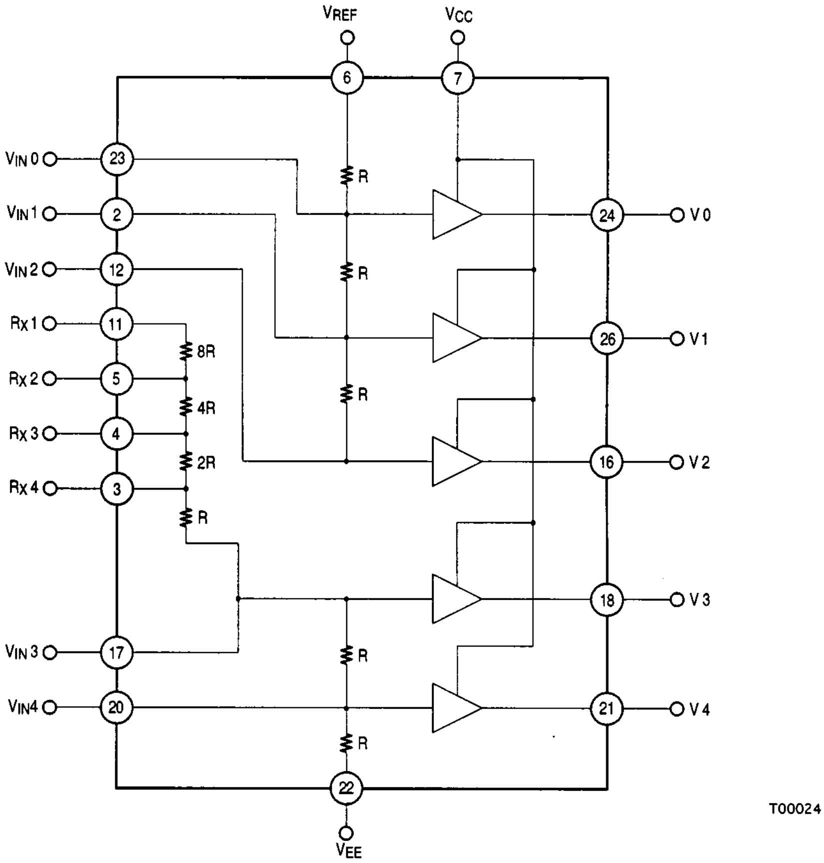


Pin Assignment



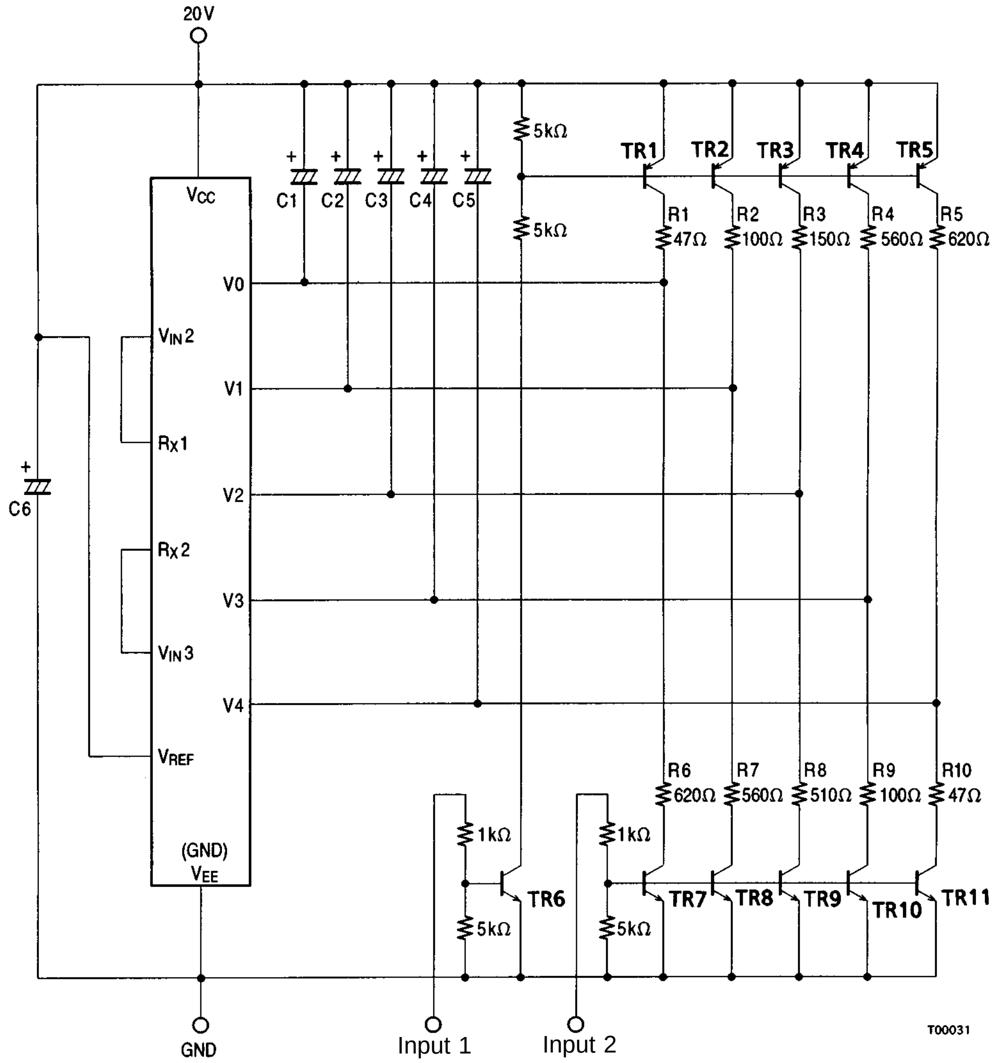
T00025

Block Diagram



Note: Use the IC so that $V_{RX}1 \geqq V_{RX}2 \geqq V_{RX}3 \geqq V_{RX}4$ is obeyed.

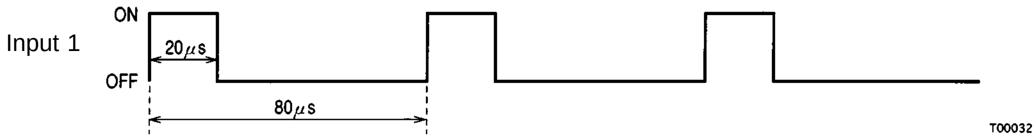
Maximum Output Current Load Test Conditions

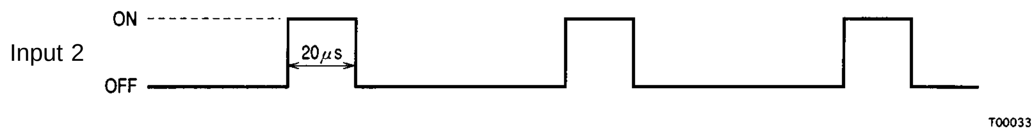


$V_{CC} - V_{EE}$ = 20 V, R_X = 8R
C1 = 5 µF, C2 = 10 µF, C3 = 10 µF, C4 = 5 µF, C5 = 10 µF, C6 = 33 µF
TR1 to TR5: 2SA984 E or F rank
TR6 to TR11: 2SC2274 E or F rank

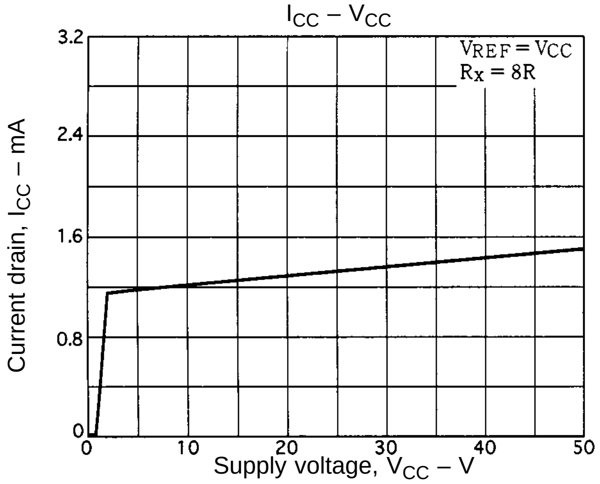
Unit (resistance: Ω, capacitance: F)

Output load resistances R1 to R10 are set in order that current of 30 mA max. are supplied to both source and sink sides when an on-level input is applied to the inputs 1 or 2.

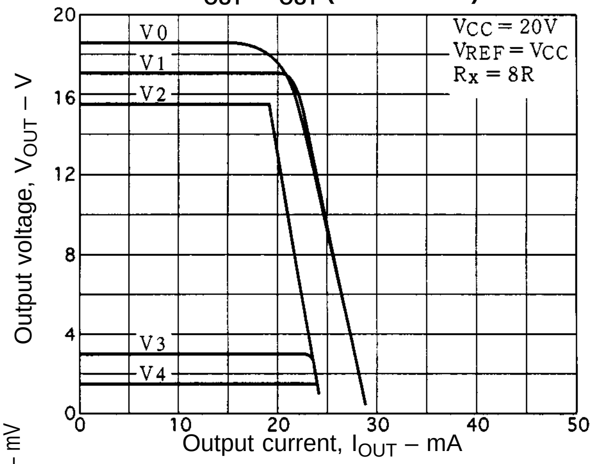




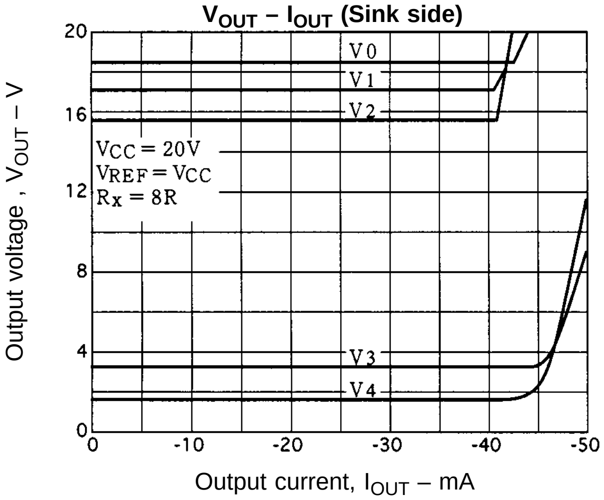
I_{CC} – V_{CC}



V_{OUT} – I_{OUT} (Source side)



V_{OUT} – I_{OUT} (Sink side)



Output voltage ratio – Ta