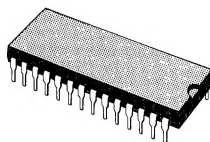


2-CHANNEL FLOPPY DISK READ/ WRITE CIRCUITS

- TWO GAIN VERSIONS (A AND B)
- COMPATIBLE WITH 8", 5.25" AND 3.5" DRIVES.
- INTERNAL WRITE AND ERASE CURRENT SOURCES, EXTERNALLY SET
- INTERNAL CENTER TAP VOLTAGE SOURCE
- CONTROL SIGNALS ARE TTL COMPATIBLE
- TTL SELECTABLE WRITE CURRENT BOOST
- OPERATES ON +12V AND +5V POWER SUPPLIES

tures a gain of 85 min and the L6570B of 300 min. All logic inputs and outputs are TTL compatible and all timing is externally programmable for maximum design flexibility.



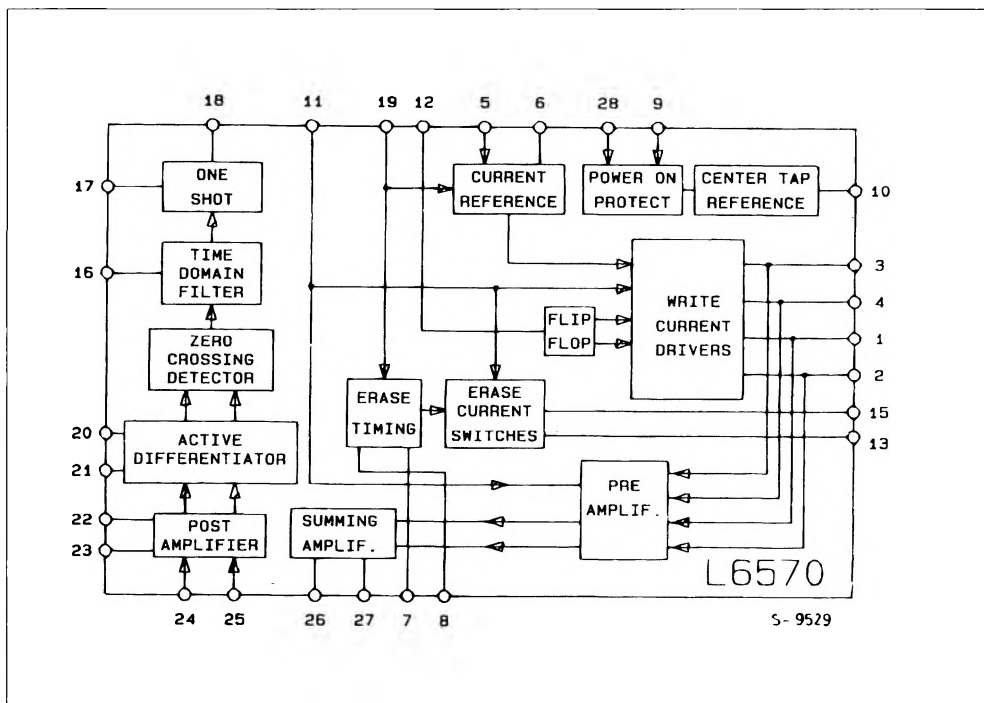
DIP-28 Plastic

ORDER CODES : L6570A
L6570B

DESCRIPTION

The L6570A/ B are integrated circuits which perform the functions of generating write signals and amplifying and processing read signals required for a double sided floppy disk drive. The L6570A fea-

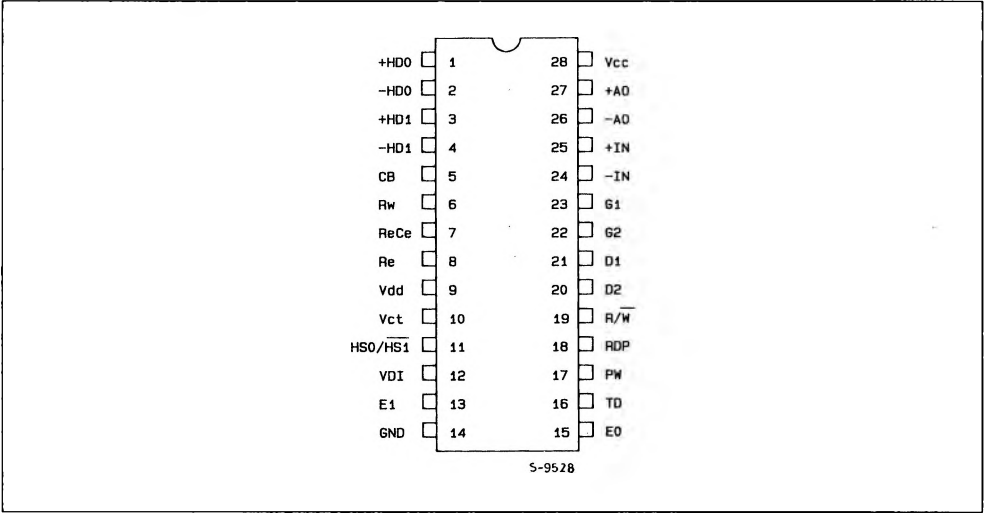
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V _{CC}	5V Supply Voltage	7	V
V _{DD}	12V Supply Voltage	14	V
T _{stg}	Storage Temperature	– 65 to 150	°C
T _{amb}	Ambient Operating Temperature	0 to + 70	°C
T _j	Junction Operating Temperature	0 to + 130	°C
V _I	Logic Input Voltage	– 0.5 to 7.0	V
P _{tot}	Power Dissipation	500	mW

CONNECTION DIAGRAM (top view)



THERMAL DATA

R _{th j-amb}	Thermal Resistance Junction-ambient	Max	100	°C/W
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ELECTRICAL CHARACTERISTICS (unless otherwise specified, $4.75V \leq V_{CC} \leq 5.25V$; $11.4V \leq V_{DD} \leq 12.6V$; $0^\circ C \leq T_{amb} \leq 70^\circ C$; $R_W = 430 \Omega$; $R_{ED} = 62 K\Omega$; $C_E = 0.012 \mu F$; $R_{EH} = 62 K\Omega$; $R_{EC} = 220\Omega$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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POWER SUPPLY CURRENTS

I_{CC}	5V Supply Current	Read Mode			35	mA
		Write Mode			38	mA
I_{DD}	12V Supply Current	Read Mode	L6570A		26	mA
			L6570B		35	mA
		Write Mode (exclude Write and Erase currents)	L6570A		24	mA
			L6570B		35	mA

LOGIC SIGNALS-READ/WRITE (R/W), CURRENT BOOST (CB)

V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Input Low Current	$V_{IL} = 0.4V$			- 0.4	mA
V_{IH}	Input High Voltage		2.0			V
I_{IH}	Input High Current	$V_{IH} = 2.4V$			20	μA

LOGIC SIGNALS-WRITE DATA INPUT (WDI), HEAD SELECT (HS0/HS1)

V_{T+}	Threshold Voltage, Positive-going		1.4		1.9	V
V_{T-}	Threshold Voltage, Negative-going		0.6		1.1	V
V_{T+}, V_{T-}	Hysteresis		0.4			V
I_{IH}	Input High Current	$V_{IH} = 2.4V$			20	μA
I_{IL}	Input Low Current	$V_{IL} = 0.4V$			- 0.4	mA

CENTER TAP VOLTAGE REFERENCE

V_{CT}	Output Voltage	$I_{WC} + I_E = 3 \text{ mA to } 60 \text{ mA}$	$V_{DD}-1.5$		$V_{DD}-0.5$	V
V_{CC}	Turn-Off Threshold		4.0			V
V_{DD}	Turn-Off Threshold		9.6			V
V_{CT}	Disabled Voltage				1.0	V

ERASE OUTPUTS (E1, E0)

	Unselected Head Leakage	$V_{EO}, V_{E1} = 12.6V$			100	μA
V_{E1}, V_{EO}	Output on Voltage	$I_E = 50 \text{ mA}$			0.5	V

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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WRITE CURRENT

	Unselected Head Leakage	$V_{E1}, V_{E0} = 12.6V$			25	μA
	Write Current Range	$R_W = 820 \Omega$ to 180Ω	3		10	mA
	Current Reference Accuracy	$I_{WC} = 2.3/R_W$ V_{CB} (current boost) = 0.5V	-5		+5	%
	Write Current Unbalanced	$I_{WC} = 3$ mA to 10 mA			1.0	%
	Differential Head Voltage Swing	$\Delta I_{WC} \leq 5 \%$	12.8			V_{pk}
	Current Boost	$V_{CB} = 2.4V$	1.25 I_{WC}		1.35 I_{WC}	

ERASE TIMING

	Erase Delay Range	$R_{ED} = 39 K\Omega$ to $82 K\Omega$ $C_E = 0.0015 \mu F$ to $0.043 \mu F$	0.1		1.0	ms
	Erase Delay Accuracy $\frac{\Delta T_{ED}}{T_{ED}} \times 100 \%$	$T_{ED} = 0.69 R_{ED} C_E$ $R_{ED} = 39 K\Omega$ to $82 K\Omega$ $C_E = 0.0015 \mu F$ to $0.043 \mu F$	- 15		+ 15	%
	Erase Hold Range	$R_{EH} + R_{ED} = 78 K\Omega$ to $164 K\Omega$ $C_E = 0.0015 \mu F$ to $0.043 \mu F$	0.2		2.0	ms
	Erase Hold Accuracy $\frac{\Delta T_{ED}}{T_{ED}} \times 100 \%$	$T_{EH} = 0.69 (R_{ED} + R_{ED}) C_E$ $R_{EH} + R_{ED} = 78 K\Omega$ to $164 K\Omega$ $C_E = 0.0015 \mu F$ to $0.043 \mu F$	- 15		+ 15	%

ELECTRICAL CHARACTERISTICS (Unless otherwise specified : V_{IN} (Preamplifier) = 10mV_{pp} sine wave, DC coupled to center tap. Summing amplifier load = 2 K Ω line-line, AC coupled. V_{IN} (Postamplifier) = 0.2 V_{pp} sine wave, AC coupled ; R_G = open ; Data pulse load = 1 K Ω to V_{CC} ; C_D = 240 pF ; C_{TD} = 100 pF ; R_{TD} = 7.5 K Ω ; C_{PW} = 47 pF ; R_{PW} = 7.5 K Ω).

READ MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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PREAMPLIFIER-SUMMING AMPLIFIER

	Diff Voltage Gain	Freq. = 250 KHz L6570A L6570B	85 300		115 400	V/V
	Bandwidth (- 3 dB)		3			MHz
	Gain Flatness	Freq. = DC to 1.5 MHz			± 1.0	dB
	Diff. Input Impedance	Freq. = 250 KHz	20			K Ω
	Max. Diff. Output Voltage Swing	$V_{IN} = 250$ KHz Sine Wave THD $\leq 5 \%$ L6570A L6570B	2.5 4.0			V _{pp}
	Small Signal Difference Output Resistance	$I_O \leq 1.0$ mA _{pp}			75	Ω
	Common Mode Rejection Ratio	$V_{IN} = 300$ mV _{pp} @ 500 KHz Inputs Shorted L6570A L6570B	50 40			dB

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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PREAMPLIFIER-SUMMING AMPLIFIER

	Power Supply Rejection Ratio	$\Delta V_{DD} = 300 \text{ mV}_{pp}$ @ 500 KHz Inputs Shorted to V_{CT}	50			dB
	Channel Isolation	Unselected Channel $V_{IN} = 100 \text{ mV}_{pp}$ @ 500 KHz. Selected Channel Input Connected to V_{CT}	40			dB
	Equivalent Input Noise	Power BW = 10 kHz to 1 MHz Inputs Shorted to V_{CT}			10	μV_{rms}
V_{CT}	Center Tap Voltage			1.5		V

POSTAMPLIFIER-ACTIVE DIFFERENTIATOR

	AO, Diff. Voltage Gain + IN, - IN to D1, D2	Freq. = 250 KHz	8.5		11.5	V/V
	Bandwidth (- 3dB) + IN, - IN to D1, D2	$C_D = 0.1 \mu F$, $R_D = 2.5 \text{ K}\Omega$	3			MHz
	Gain Flatness + IN, - IN to D1, D2	Freq. = DC to 1.5 MHz $C_D = 0.1 \mu F$, $R_D = 2.5 \text{ K}\Omega$			± 1.0	dB
	Max. Diff. Output Voltage Swing	$V_{IN} = 250 \text{ KHz}$ Sine Wave, AC Coupled. $\leq 5\%$ THD in Voltage across C_D	5.0			V_{pp}
	Max. Diff. Input Voltage	$V_{IN} = 250 \text{ KHz}$ Sine Wave, AC Coupled. $\leq 5\%$ THD in Voltage across C_D , $R_G = 1.5 \text{ K}\Omega$	2.5			V_{pp}
	Diff. Input Impedance		10			$\text{K}\Omega$
	Gain Control Accuracy $\frac{\Delta A_R}{A_R} \times 100\%$	$A_R = A_O R_G / (8 \times 10^3 + R_G)$ $R_G = 2 \text{ K}\Omega$	- 25		+ 25	%
	Threshold Differential Input Voltage	Min. diff. input voltage at post amp. that results in a change of state at RDP $V_{IN} = 250 \text{ KHz}$ square wave, $C_D = 0.1 \mu F$ $R_D = 500 \Omega$, $T_R, T_F \leq 0.2 \mu s$. No overshoot ; Data pulse from each V_{IN} transition			3.7	mV_{pp}
	Peak Differential Network Current		1.0			mA

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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TIME DOMAIN FILTER

	Delay Accuracy $\frac{\Delta T_{TD}}{T_{TD}} \times 100 \%$	$T_{TD} = 0.58 R_{TD} \cdot (C_{TD} + 10^{-11}) + 150 \text{ ns.}$ $R_{TD} = 5 \text{ K}\Omega \text{ to } 10 \text{ K}\Omega$ $C_{TD} = 56 \text{ pF}$ $V_{IN} = 50 \text{ mV}_{pp} @ 250 \text{ KHz sq. wave}$ $T_R, T_F \leq 20 \text{ ns, AC coupled.}$ Delay measured from 50 % input amplitude to 1.5 V data pulse	- 15		+ 15	%
	Delay Range	$T_{TD} = 0.58 R_{TD} \cdot (C_{TD} + 10^{-11}) + 150 \text{ ns.}$ $R_{TD} = 5 \text{ K}\Omega \text{ to } 10 \text{ K}\Omega$ $C_{TD} = 56 \text{ pF to } 240 \text{ pF}$ $R_D = 500 \Omega$ $C_D = 0.1 \mu\text{F.}$	240		2370	ns

DATA PULSE

	Width Accuracy $\frac{\Delta T_{PW}}{T_{PW}} \times 100\%$	$T_{PW} = 0.58 R_{PW} \times (C_{PW} + 8 \times 10^{-12}) + 20 \text{ ns}$ $R_{PW} = 5 \text{ K}\Omega \text{ to } 10 \text{ K}\Omega$ $C_{PW} \geq 36 \text{ pF}$ with measured at 1.5V amplitudes	- 20		+ 20	%
	Active Level Output Voltage	$I_{OH} = 400 \mu\text{A}$	2.7			V
	Inactive Level Output Leakage	$I_{OL} = 4 \text{ mA}$			0.5	V
	Pulse Width	$T_{PW} = 0.58 R_{PW} \times (C_{PW} + 8 \times 10^{-12}) + 20 \text{ ns}$ $R_{PW} = 5 \text{ K}\Omega \text{ to } 10 \text{ K}\Omega$ $C_{PW} = 36 \text{ pF to } 200 \text{ pF}$	145		1225	ns

TEST SCHEMATICS

Figure 1 : Preamplifier Characteristics.

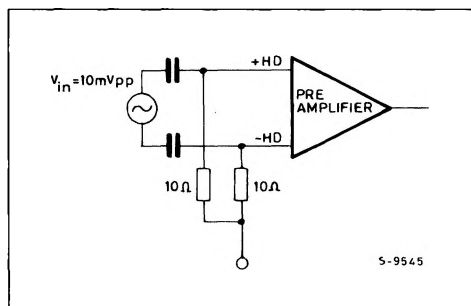
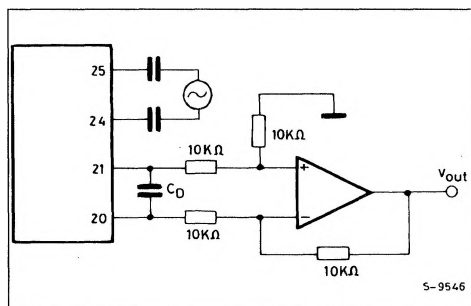


Figure 2 : Postamplifier Differential Output Voltage Swing and Voltage Gain.



TEST SCHEMATICS (Continued)

Figure 3 : Postamplifier Threshold Differential Input Voltage.

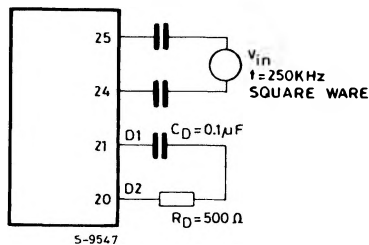


Figure 4 : Complete Test Circuit.

