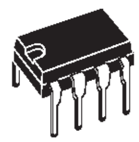
SGS-THOMSON MICROELECTRONICS

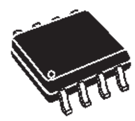
L6569
L6569A

HIGH VOLTAGE HALF BRIDGE DRIVER WITH OSCILLATOR

- TECHNOLOGY: BCD ”OFF-LINE”
- FLOATING SUPPLY VOLTAGE UP TO 600V
- GND REFERRED SUPPLY VOLTAGE UP TO 18V
- DRIVER CURRENT CAPABILITY:
  - SINK CURRENT = 270mA
  - SOURCE CURRENT = 170mA
- VERY LOW START UP CURRENT: 150µA
- VERY LOW OPERATING CURRENT: <2mA
- UNDERVOLTAGE LOCKOUT
- PROGRAMMABLE OSCILLATOR FREQUENCY
- dV/dt IMMUNITY UP TO ± 50V/ns



Minidip



SO8

ORDERING NUMBERS:

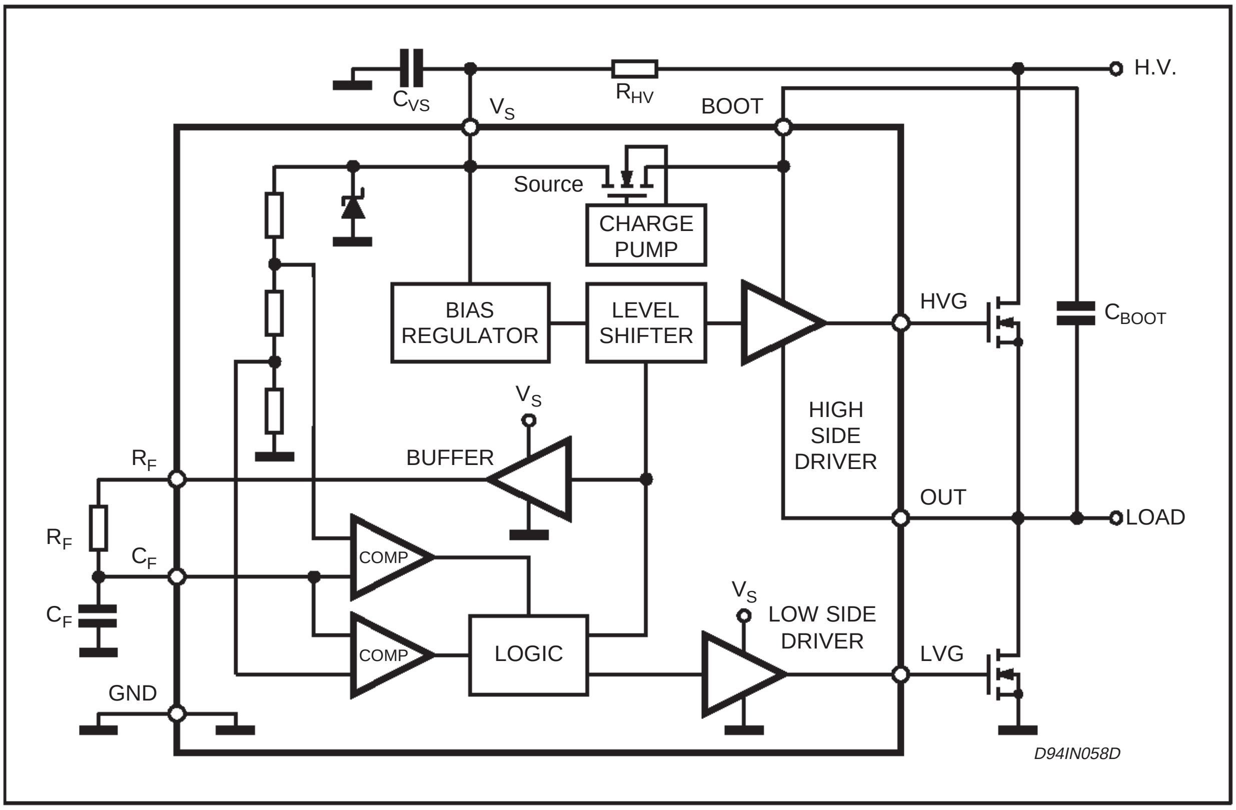
L6569/L6569A	L6569D/L6569AD

DESCRIPTION

The device is a high voltage half bridge driver with built-in oscillator. The frequency of the oscillator can be programmed using external resistor and capacitor.

The output drivers are designed to drive external n-channel power MOSFET and IGBT. The internal logic assures a dead time to avoid cross-conduction of the power devices.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_S (*)	Supply Current	25	mA
V_{CF}	Oscillator Resistor Voltage	18	V
V_{LVG}	Low Side Switch Gate Output	14.6	V
V_{OUT}	High Side Switch Source Output	-1 to V_{BOOT} - 18	V
V_{HVG}	High Side Switch Gate Output	-1 to V_{BOOT}	V
V_{BOOT}	Floating Supply Voltage	618	V
$V_{BOOT/OUT}$	Floating Supply vs OUT Voltage	18	V
dV_{BOOT}/dt	V_{BOOT} Slew Rate (Repetitive)	± 50	V/ns
dV_{OUT}/dt	V_{OUT} Slew Rate (Repetitive)	± 50	V/ns
T_{stg}	Storage Temperature	-40 to 150	°C
T_j	Junction Temperature	-40 to 150	°C
T_{amb}	Ambient Temperature (Operative)	-40 to 125	°C

(*) The device has an internal zener clamp between GND and V_S (typical 15.6V).
Therefore the circuit should not be driven by a DC low impedance power source.

Note: ESD immunity for pins 6, 7 and 8 is guaranteed up to 900 V (Human Body Model)

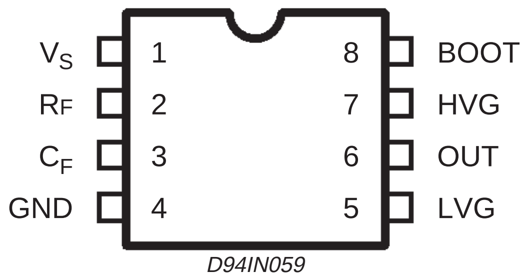
THERMAL DATA

Symbol	Parameter		Minidip	SO8	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-Ambient	Max	100	150	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_S	Supply Voltage	10	V_{CL}	V
V_{BOOT}	Floating Supply Voltage	-	500	V
V_{OUT}	High Side Switch Source Output	-1	V_{BOOT} - V_{CL}	V
f_{out}	Oscillation Frequency		200	kHz

PIN CONNECTION



ELECTRICAL CHARACTERISTICS (V_S = 12V; V_{BOOT} - V_{OUT} = 12V; T_j = 25°C; unless otherwise specified.)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{SUVP}	1	V_S Turn On Threshold		8.3	9	9.7	V
V_{SUVN}		V_S Turn Off Threshold		7.3	8	8.7	V
V_{SUVH}		V_S Hysteresis		0.7	1	1.3	V
V_{CL}		V_S Clamping Voltage	I_S = 5mA	14.6	15.6	16.6	V
I_{SU}		Start Up Current	$V_S < V_{SUVN}$		150	250	µA
I_q		Quiescent Current	$V_S > V_{SUVP}$		500	700	µA
I_{BOOTLK}	8	Leakage Current BOOT pin vs GND	V_{BOOT} = 580V			5	µA
I_{OUTLK}	6	Leakage Current OUT pin vs GND	V_{OUT} = 562V			5	µA
$I_{HVG\ SO}$	7	High Side Driver Source Current	V_{HVG} = 6V	110	175		mA
$I_{HVG\ SI}$		High Side Driver Sink Current	V_{HVG} = 6V	190	275		mA
$I_{LVG\ SO}$	5	Low Side Driver Source Current	V_{LVG} = 6V	110	175		mA
$I_{LVG\ SI}$		Low Side Driver Sink Current	V_{LVG} = 6V	190	275		mA
V_{RFON}	2	RF High Level Output Voltage	I_{RF} = 1mA	V_S -0.05		V_S -0.2	V
$V_{RF\ OFF}$		RF Low Level Output Voltage	I_{RF} = -1mA	50		200	mV
V_{CFU}	3	CF Upper Threshold		7.7	7.95	8.2	V
V_{CFL}		CF Lower Threshold		3.80	4.05	4.3	V
t_d		Internal Dead Time		0.85	1.25	1.65	µs
D_C		Duty Cycle, Ratio Between Dead Time + Conduction Time of High Side and Low Side Drivers		0.45	0.5	0.55	
R_{ON}		On resistance of Boostrap LDMOS			120		Ω
V_{BC}		Boostrap Voltage before UVLO	VS = 8.2	2.5	3.6		V
I_{AVE}	1	Average Current from Vs	No Load, fs = 60KHz		1.2	1.5	mA
fout	6	Oscillation Frequency	RT = 12k CT = 1nF	57	60	63	kHz

OSCILLATOR FREQUENCY

The frequency of the internal oscillator can be programmed using external resistor and capacitor. The nominal oscillator frequency can be calculated using the following equation:

$$f_{OSC} = \frac{1}{2 \cdot R_F \cdot C_F \cdot \ln 2} = \frac{1}{1.3863 \cdot R_F \cdot C_F}$$

where R_F and C_F are the external resistor and capacitor

Bootstrap Function

The L6569 has an internal Bootstrap structure that enables the user to avoid the external diode needed, in similar devices, to perform the charge of the bootstrap capacitor that, in turns, provide an appropriate driving to the Upper External Mosfet. The operation is achieved with an unique structure (patented) that uses a High Voltage Lateral DMOS driven by an internal charge pump (see Block Diagram) and syncronized, with a 50 nsec delay, with the Low Side Gate driver (LVG pin), actually working as a syncronous rectifier . The charging path for the Bootstrap capacitor is closed via the Lower External Mosfet that is driven ON (i.e. LVG High) for a time interval:

$$T_c = R_F \cdot C_F \cdot \ln 2 \cong 1.1 R_F \cdot C_F$$

starting from the time the Supply Voltage Vs has reached the Turn On Voltage (Vsup = 9 V typical value).

After time T1 (see Waveform Diagram) the LDMOS that charges the Bootstrap Capacitor, is on on with a Ron=120 ohm (typical value).

In the L6569A a different start up procedure is followed (see Waveform Diagram). The Lower External Mosfet is drive OFF untill Vs has reached the Turn On Threshold (Vsuvp), then again the Tc time interval starts as above.

Being the LDMOS used to implement the bootstrap operation a "bidirectional" switch the current flowing into the Vboot pin can lead an undue stress to the LDMOS itself if a ZERO VOLTAGE SWITCHING operations is not ensured, and then an high voltage is applied to the Vboot pin. This condition can occur, for example, when the load is removed and an high resistive value is placed in series with the gate of the external Power Mos. To help the user to secure his design a SAFE OPERATING AREA for the Bootstrap LDMOS is provided (fig. 6). Let's consider the steps that should be taken.

1) Calculate the Turn on delay (td) of your Lower Power MOS:

$$t\,d = (Rg + Rid) \cdot Ciss \ln(1/(1-V_{TH}/V_S))$$

2) Calculate the Fall time (tf) of your Lower Power MOS:

$$tf = (V_S-V_{TH}) / (Rg+Rid) \cdot Qgd$$

where:

Rg= External gate resistor

Rid = 50 ohm , typical equivalent output resistance of the driving buffer (when sourcing current)

V_{TH}, Ciss and Qgd are Power MOS parameters

V_S = Low Voltage Supply.

3) Sketch the Vboot waveform (using log-log scales) starting from the Drain Voltage of the Lower Power MOS (remember to add the Vs, your Low Voltage Supply, value) on the Bootstrap LDMOS SOA . On fig. 7 an example is given where:

Vs = Low Voltage Supply
V_{HV} = High Voltage Supply Rail

The Vboot voltage swing must fall below the curve identified by the actual operating frequency of your application.

DEMO BOARD

To allow an easy evaluation of the device, a P.C. board dedicated to lamp ballast application has been designed.

Fig.10 shows the electrical schematic of a typical ballast application, while the PC and component layout is given in Fig11. This application has been designed to work with both the 110+/-20%V and the 220 +/- 20%V mains by means of a voltage doubler configuration at the bulk capacitor. The ballast inductance and the operating frequency are especially designed for a 18 W Sylvania Deluxe T/E type bulb. The PTC for preheat at the start up and the two back to back synchronization diodes, makes this application easy to implement and safe in operation.

Figure 1: WAVEFORMS (L6569)

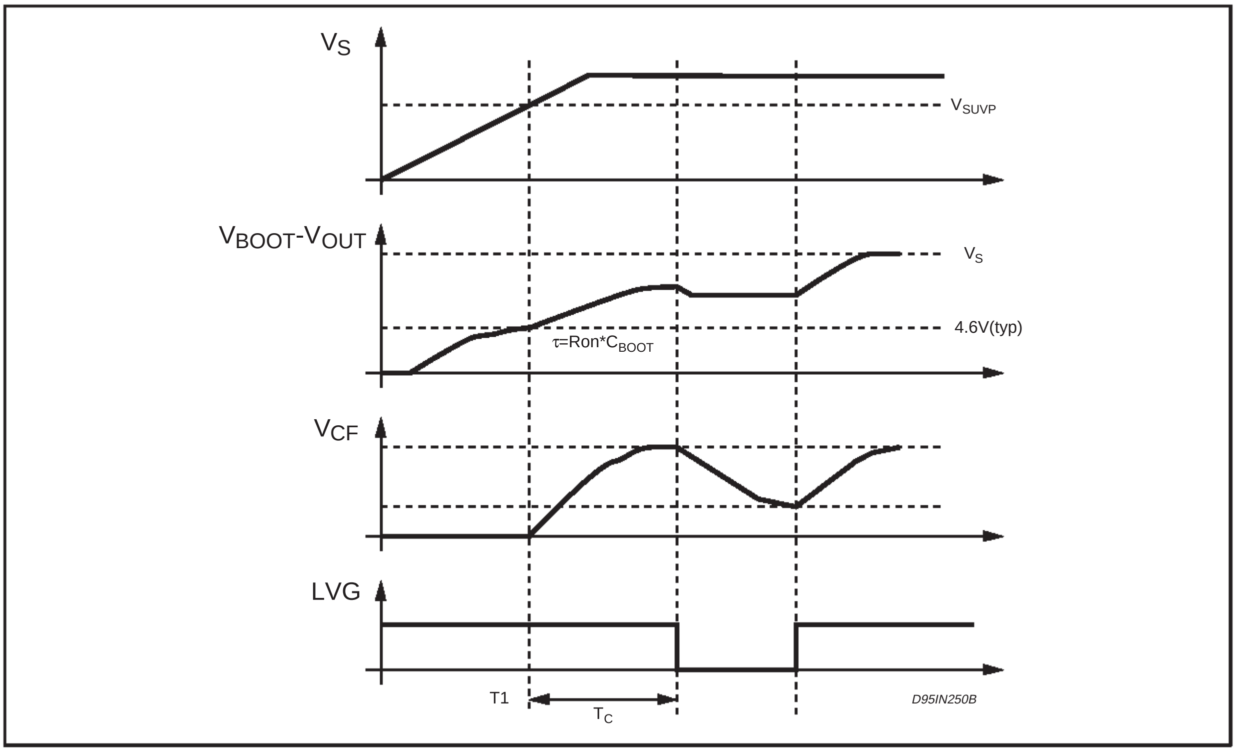


Figure 2: WAVEFORMS (L6569A)

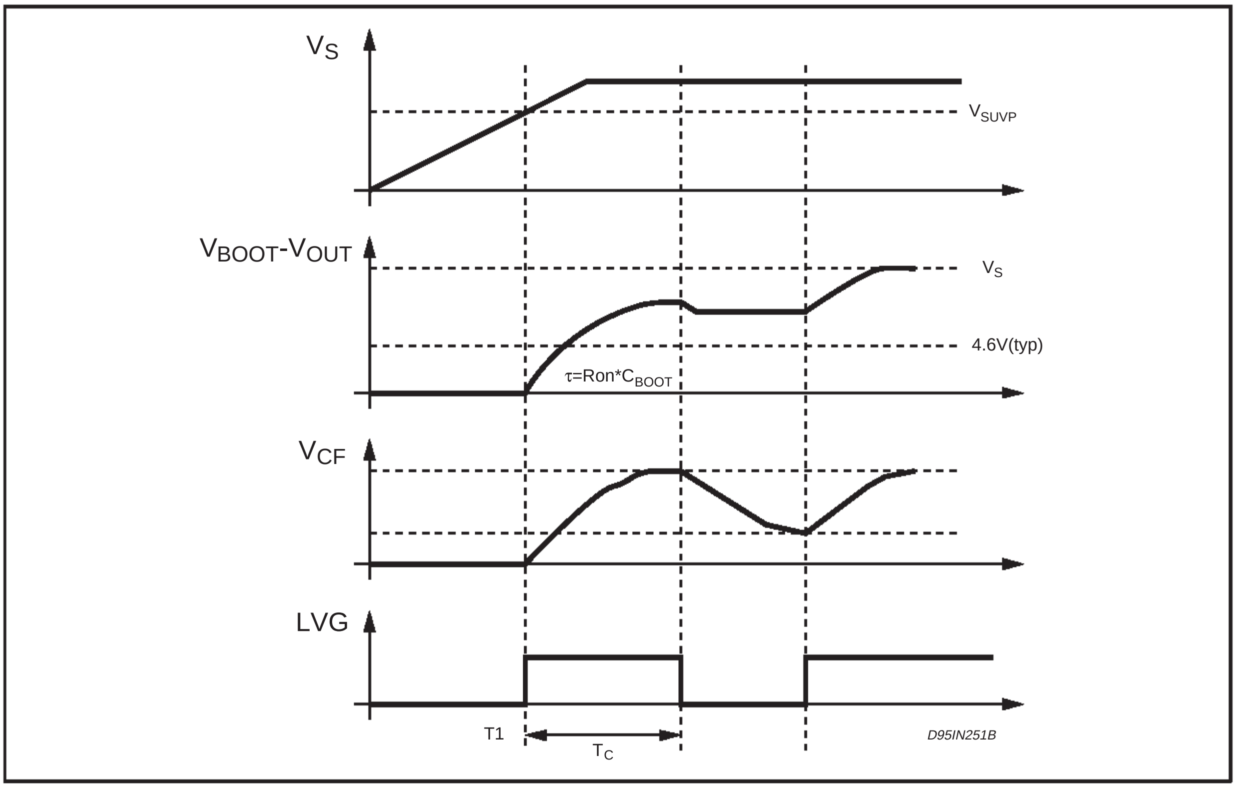


Figure 3: Typical Dead Time vs. Temperature Dependency

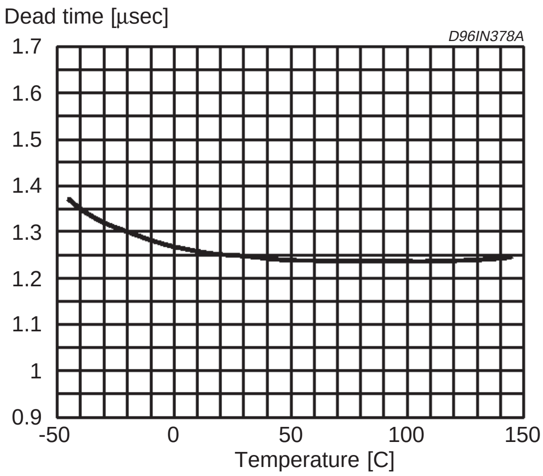


Figure 4: Typical Frequency vs Temperature Dependency

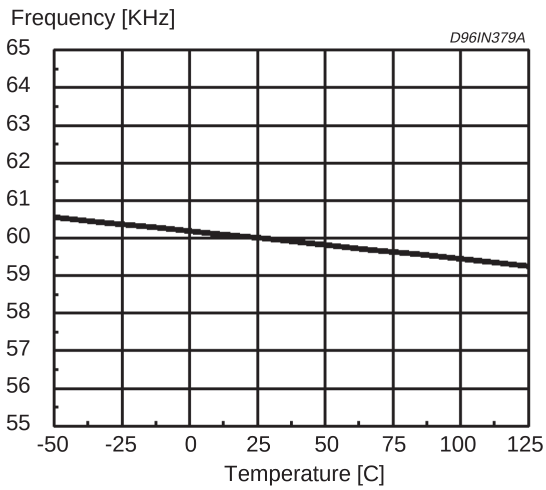


Figure 5: Typical and Theoretical Oscillator Frequency vs Resistor Value

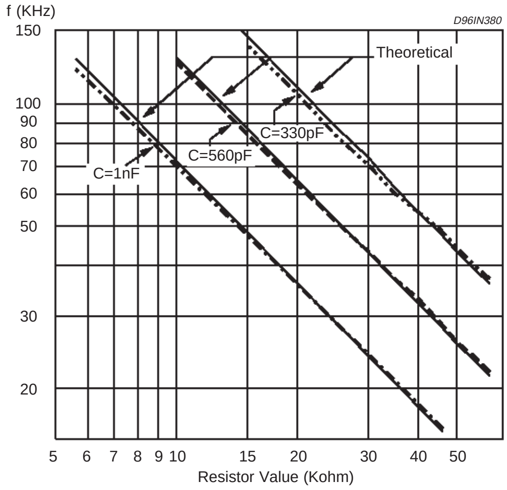


Figure 6: V_{boot} pin SOA for different Operating Frequency @ Tj = 125°C

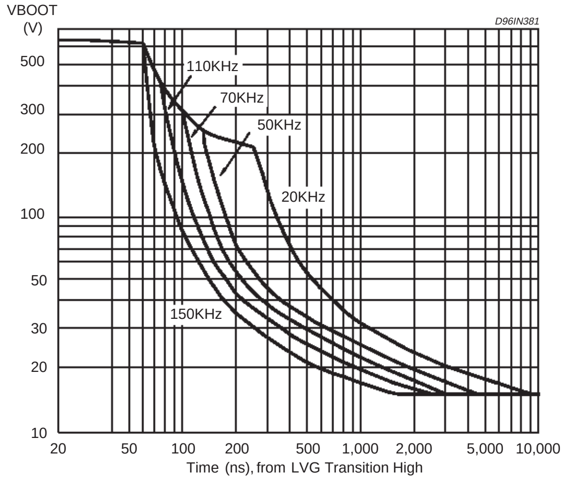


Figure 7: V_{boot} pin SOA @ Tj = 125°C

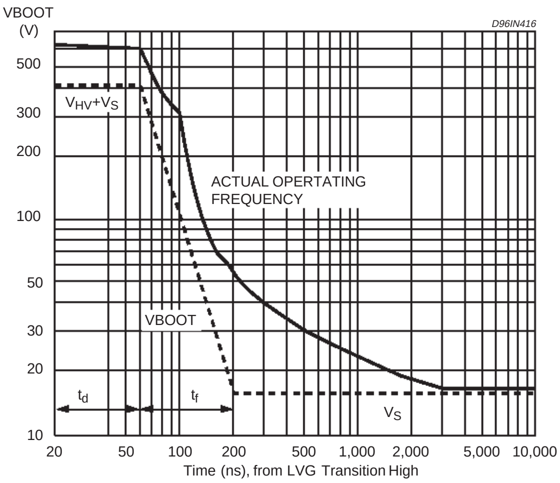
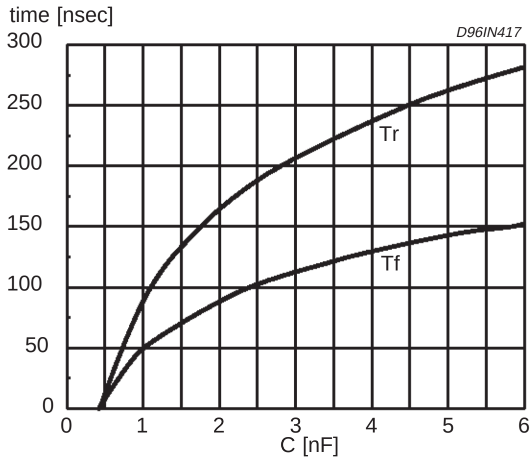


Figure 8: Typical Rise and Fall Times vs. Load Capacitance



For both high and low side buffers @25°C Tamb

Figure 9: Quiescent Current vs. Supply Voltage.

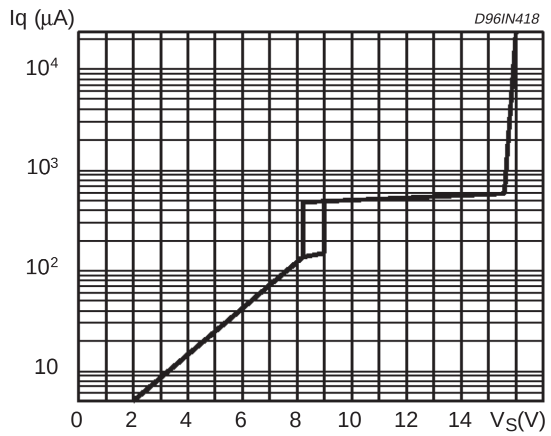


Figure 10: CFL Demoboard 110/220V Inputs.

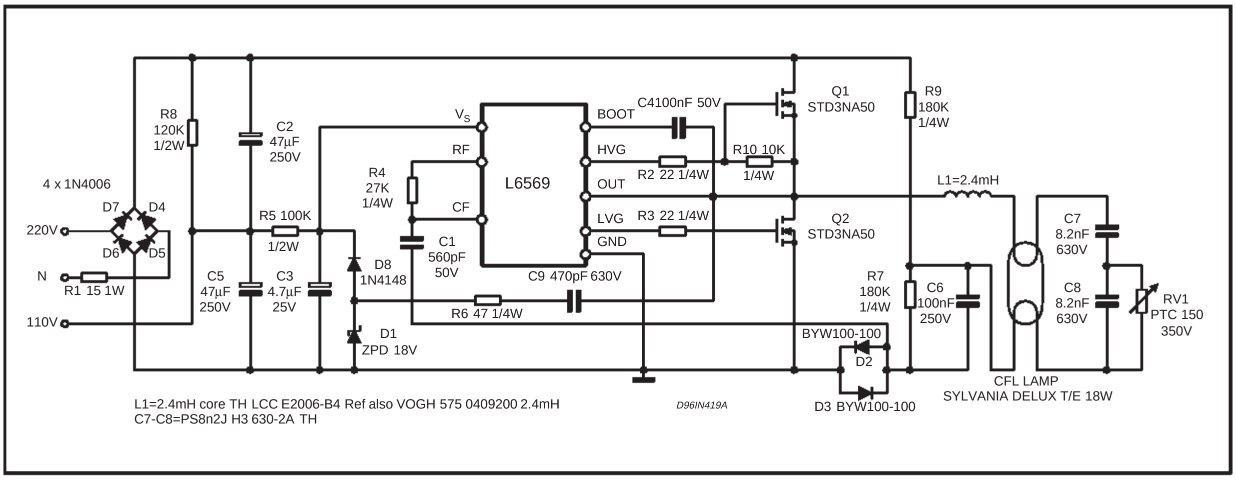
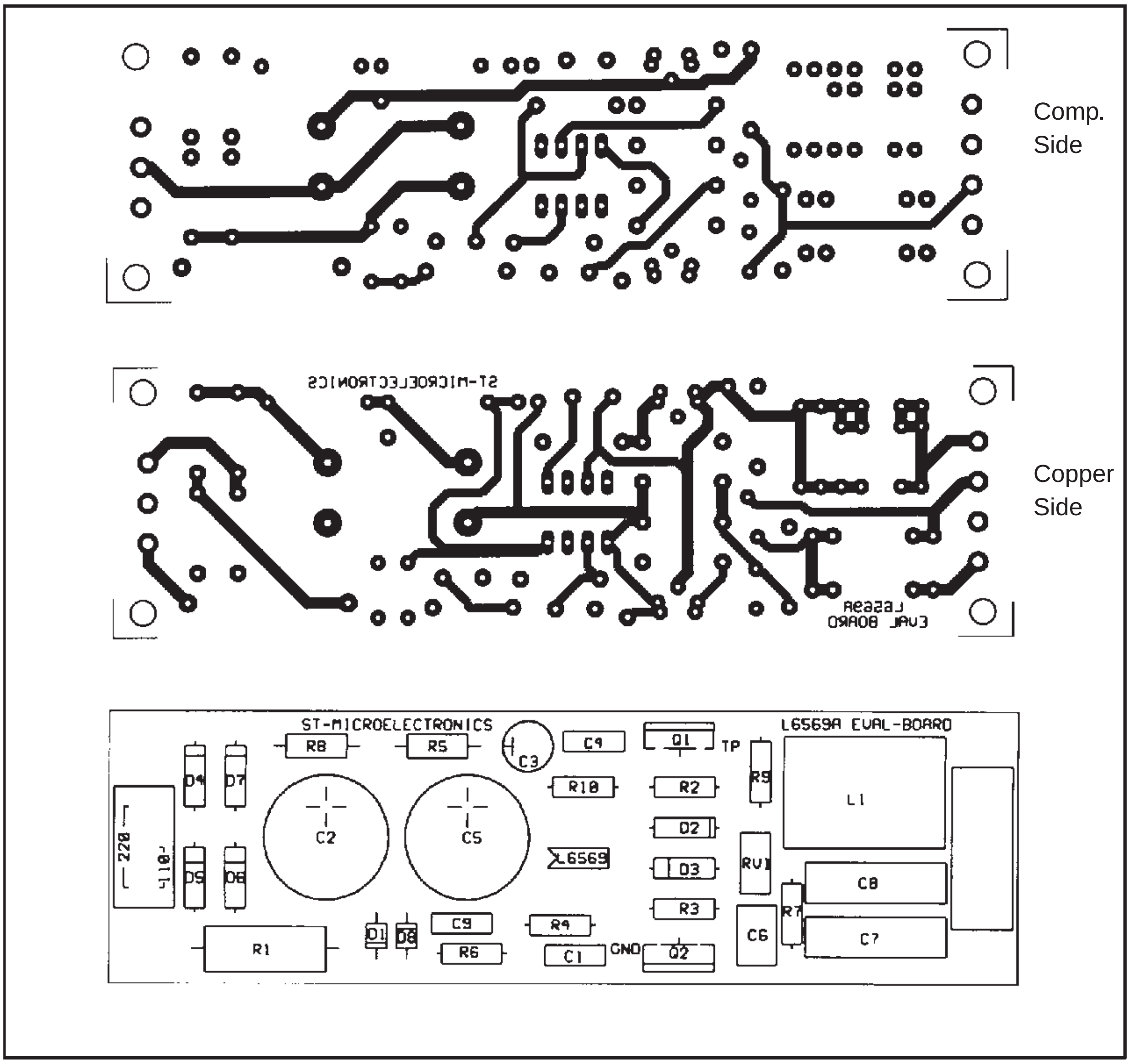
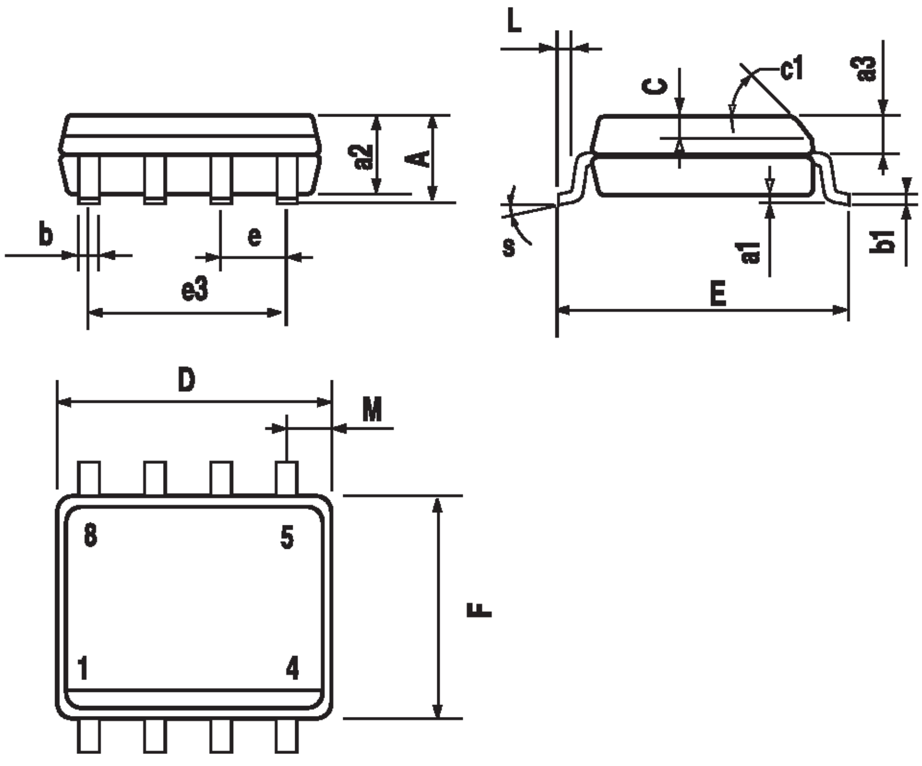


Figure 11: PC Board and Components Layout.



SO8 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					



SGS-THOMSON MICROELECTRONICS

MINIDIP PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060