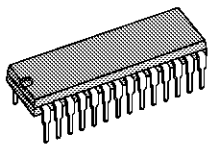
SGS-THOMSON MICROELECTRONICS

L6180
L6181

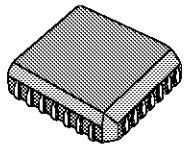
OCTAL LINE RECEIVER

ADVANCE DATA

- OCTAL LINE RECEIVER FOR:
  - EIA STD RS232D, RS423A, RS422A
  - CCIT V.10, V.11, V.28, X.26
- NO EXTERNAL COMPONENTS
- INPUT FAIL SAFING CAPABILITY
- HIGH CROSSTALK REJECTION
- L6180 DATA RATE < 100KBIT/S
- L6181 DATA RATE < 1MBIT/S
- 50V EOS OUTPUT PROTECTION



DIP 28



PLCC 28

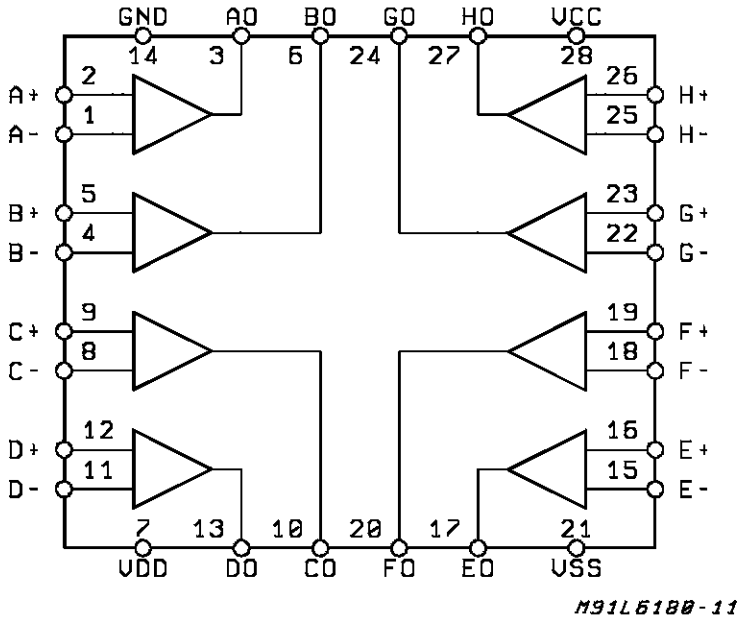
ORDERING NUMBER: L6180A DIP 28
L6180D PLCC28
L6181A DIP 28
L6181D PLCC28

DESCRIPTION

L6180/1 is an octal line receiver in a plastic DIP or PLCC designed to meet a wide range of digital communications requirements as outlined in the EIA standards RS232A without additional components, as well as the low speed applications of RS422A.

The receiver meets the CCIT recommendations V.10, V.11, X.26 and V.28 low speed applications (below 100KBS).
A low pass filter on the input starts to roll off at a frequency of 100KHz.

BLOCK DIAGRAM

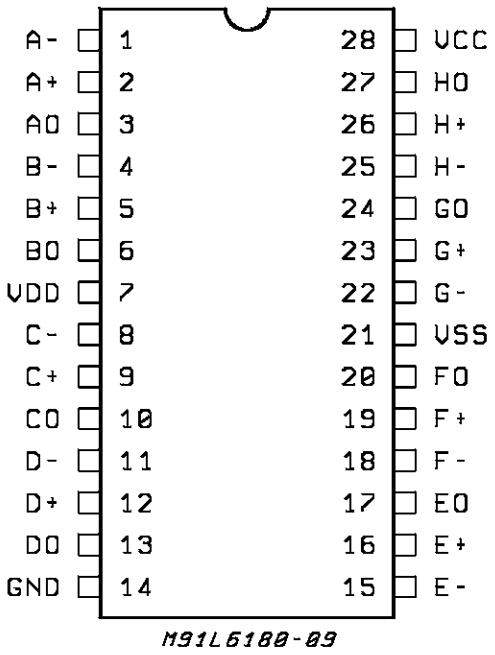


ABSOLUTE MAXIMUM RATINGS

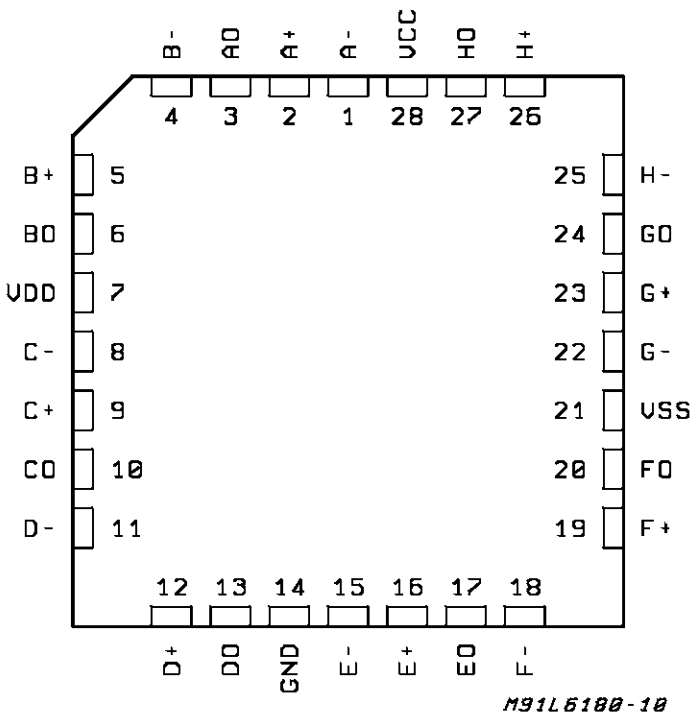
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7	V
V_{DD}	Supply Voltage	13.5	V
V_{SS}	Logic Supply Voltage	-13.5	V
C_{RR}	Common Mode Range	±15	V
V_{ID}	Differential Input Voltage	±25	V
P_{tot}	Power Dissipation (PLCC 28)	800	mW
	Power Dissipation (DIP 28)	1200	mW
I_{OS}	Output Sink Current	50	mA
t	Output Short Circuit Time	1	sec
T_{op}	Operating Free Air Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	-65 to 150	°C
	ESD	2KV max ESD 50µJ	
	Input Transient Protection	50V min EOS 100µs	

PIN CONNECTIONS (Top views)

DIP28



PLCC28



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±5%; V_{CM} = -7 to 7V; Tamb = 0 to 70°C; V_{SS} = -9 to 13.5V; V_{DD} = 9 to 13.5V; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IN}	Input Current	(See Fig.1 and note2) V_{CC} = 0 to 5.25V; V_{SS}, V_{DD} = 0 to 13.5V V_{IN} = - 10 to 10V V_{IN} = - 15 to 15V			 ±3 ±4.25	 mA mA
R_I	Input Resistance	V_{IA} or V_{IB} = 3 to 15V; (see fig.1) $R_I = \frac{[(V_{IA} \text{ or } V_{IN}) - V_{IOC}]}{I_{IN}}$	3		7	KΩ
V_{FS}	Failsafe Output Voltage	I_O = -440µA (See Fig.3)	2.7			V
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V; V_{ID} = -1V; I_{OH} = -440µA	2.7			V
V_{OL}	Low Level Output Voltage	V_{CC} = 5.25V; V_{ID} = -1V; I_{OL} = 2mA			0.4	V
V_{IT2}	V_{IOH} Comparator Threshold Voltage	(See Fig.4)	1.8	2.2	2.6	V
I_{IH2}	High Operating Threshold Voltage	V_{OL} = 0.4V; I_{OL} = 2mA; (See Fig.4)	-25		-75	mV
I_{IH1}	Low Operating Threshold Voltage	V_{OH} = 2.7V; I_O = -440µA (See Fig.4)	-125		-175	mV
V_H	Input Hysteresis Voltage	$\lvert V_{TH2} - V_{TH1} \rvert$	50		150	mV
V_{IOC1}	Open Circuit Input Voltage	Measured in accordance with V.28 and RS-232D (see note 4 and 7)		0.6	2	V
V_{IOCH}	Open Circuit Input Voltage	Measured in presence of AC Input Signal (see note 7)	3.5	4	4.5	V
I_{OS}	Open Short Circuit Current	V_{CC} = 5.25V; V_O = 0; V_{ID} = 1V; (see note 5)	20		100	mA
V_{IBV}	Input for Balance Test	(see Figure 7 and note 11)			0.4	V
C_I	Input Capacitance				100	pF
V_{CC}	Supply Current	V_{CC} = 4.75V to 5.25V; (see note 6)			100	mA
V_{dd}	Supply Current	V_{dd} = 9 to 3.5V; (see note 6)			30	mA
V_{SS}	Supplyt Current	V_{SS} = -9 to 13.5V; (see note 6)			30	mA
I_{OS}	Open Short Circuit Current	V_{CC} = 5.25V; V_O = 0; V_{ID} = 1V; (see note 5)	20		100	mA
T_{plh}	Propagation Delay Low to High	R_L = 390Ω; C_L = 50pF; $\lvert V_{IN}$ = 1V|; (see fig 5 test Circuit Fig. 6)	0		1500	ns
T_{phl}	Propagation Delay Low to High	R_L = 390Ω; C_L = 50pF; $\lvert V_{IN}$ = 1V|; (see fig 5 test Circuit Fig. 6)	0		1500	ns
V_{IOCH}	Delay V_{IOCL} to V_{IOCH} Switching	(see note 7A)			5	ms
V_{IOCL}	Delay V_{IOCH} to V_{IOCL} Switching	(see note 7B)	200			ms
V_{ist}	$\lvert T_{plh} - T_{phl} \rvert$	R_L = 390Ω; C_L = 50pF; $\lvert V_{IN} \rvert$ = 1V;(see fig. 5; Test Circuit Fig. 6)	0		500	ns
T_{SKEW1}	Skew between rec's in PKg Tp (1) hl/1h - Tp (2) hl/1h	R_L = 390Ω; C_L = 50pF; $\lvert V_{IN} \rvert$ = 1V;(see fig. 5; Test Circuit Fig. 6)	0		300	ns
f_A	Frequency Accepted (Receiver will Output)	V_{IN} = 200mVpp; (see fig. 8 and note 7;	100			KHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±5%; V_{CM} = -7 to 7V; Tamb = 0 to 70°C; V_{SS} = -9 to 13.5V; V_{DD} = 9 to 13.5V; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_R	Frequency Rejected (No Receiver Output)	V_{IN} = 2Vpp; (see fig. 8 and note 7)		5		MHz

Note:

1) The algebric convention, where the less positive (more negative) is designed the minimum

2) With the voltage V_{IA} or (V_{IB}) ranging between ±15V, while V_{IB} or (V_{IA}) is open or grounded, the resultant input current I_{IA} or (I_{IB}) shall remain within the shaded region shown in the graph in Fig.1.

3) Either Point B' or Point A' is grounded in Figure 1

4) V_{ICC} measured from grounded to (+) input with (-) input grounded
V_{ICC} measured from grounded to (+) input with (-) input grounded

5) Not more than one output should be shorted at a time and for less than 1 seond

6) The sum of the product of the maximum supply currents and voltages cannot exceed themaximum power dissipation

7) A: The conditions for the inpit switching from V_{IOCL} to V_{IOCH} mode is: V_{id} in start bit "spacing condition"for less than TpV_{ioch} (5ms).
B: The conditions for the input switching from V_{IOCH} to V_{IOCL} mode is: Vid > W_{W2} for greater than TpV_{IOCL} (200ms)

8) An example of a frequency response plot meeting the rejection/acceptance requirements is provided in figure 8.

LINE TRANSIENT IMMUNITY (Considering the following cases; powered ON, Powered OFF-LOW impedance power supply and powered OFF-HIGH impedance supply)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ESD	Static	tested per MIL-STD-883 (see note 9)	2			KV
EOS	Stress	transient pulse both polarities for 100µs (see note 9 and Fig. 2)	50			V

Note:

9) All pins are required to withstand this parameters.

10) Input pins are required to withstand fig.2 without any degradation to the circuit.

11) The balance test requirement can be met by use of a current limit circuit which reduces the input bias current I_{ib} (see figure 7) for input voltages below a threshold voltage given by (I_{ib} x 1K) - 400mV.

Figure 1: Input Current Voltage Mesurements

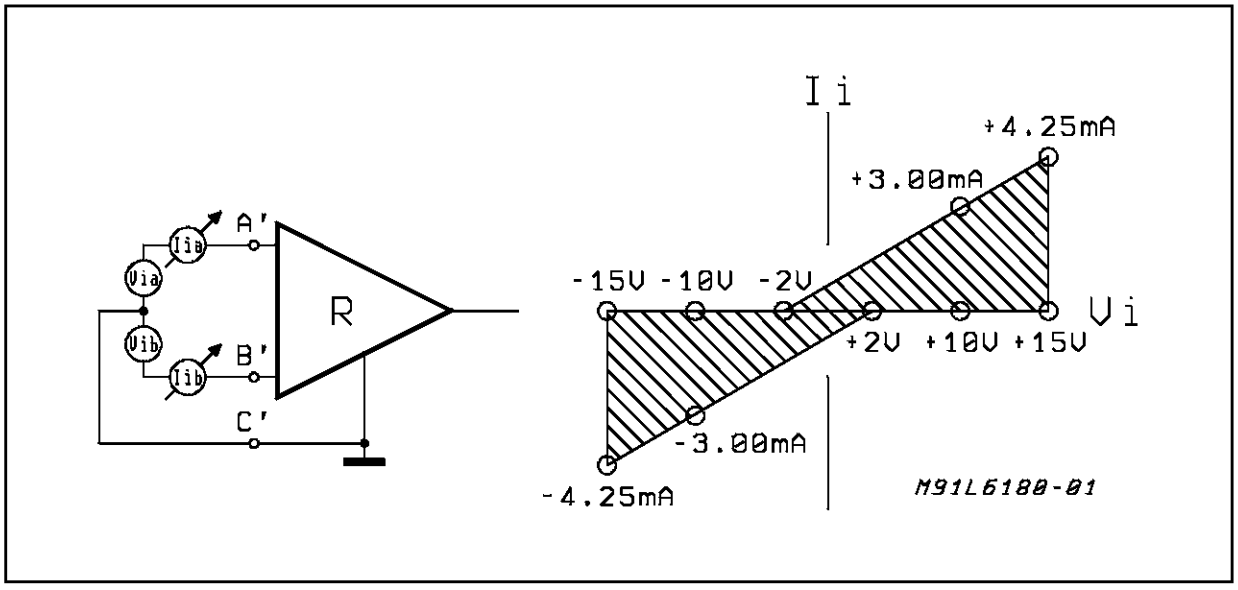


Figure 2: EOS Requiremets

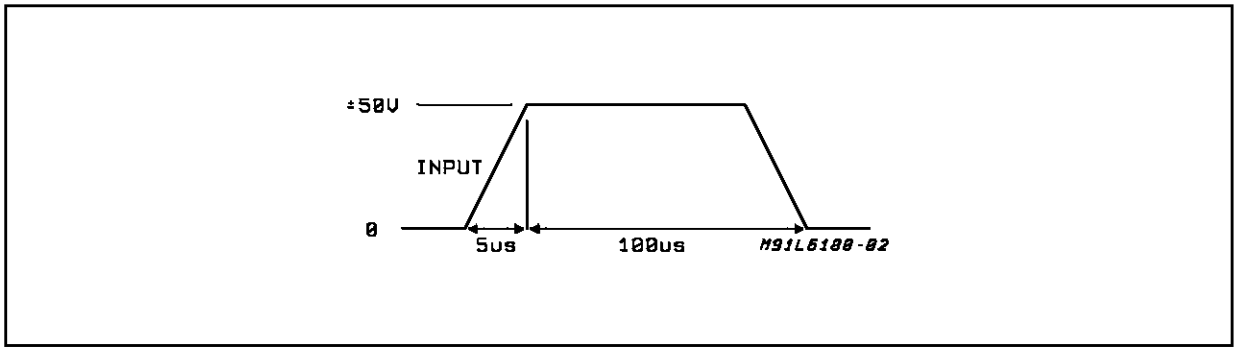
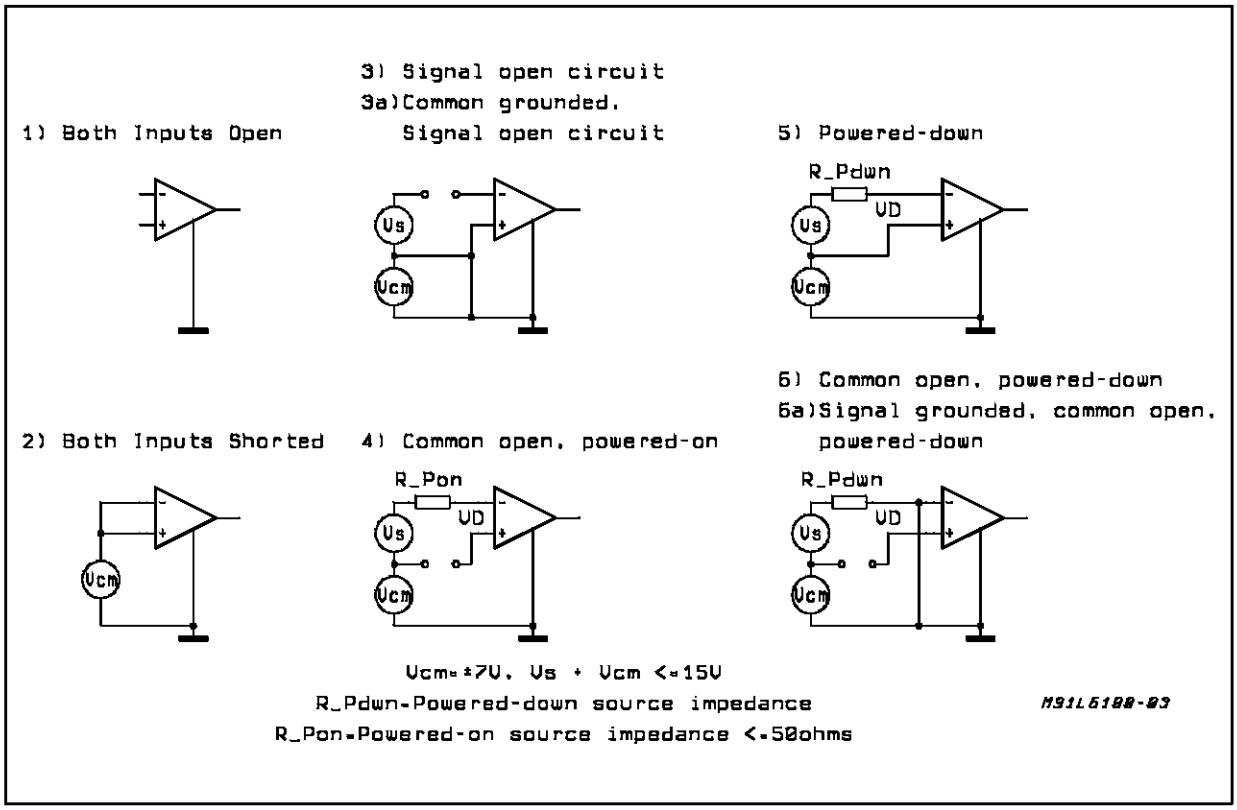


Figure 3: Output Failsafing



The output assumes a logic ”1”under the following conditions, (see figure 3)

1 Both inputs open
2 Both inputs shorted
3 Signal Opencircuit
3a Common grounded, signal open circuit
4 Common open, generator powered-on
5 Generator powered-down (see note 7)
6 Common open, generator powered-down
6a Signal grounded, common open, generator powered-down
7 Less than 250mVpp differential signal

Figure 4: Threshold voltage definition

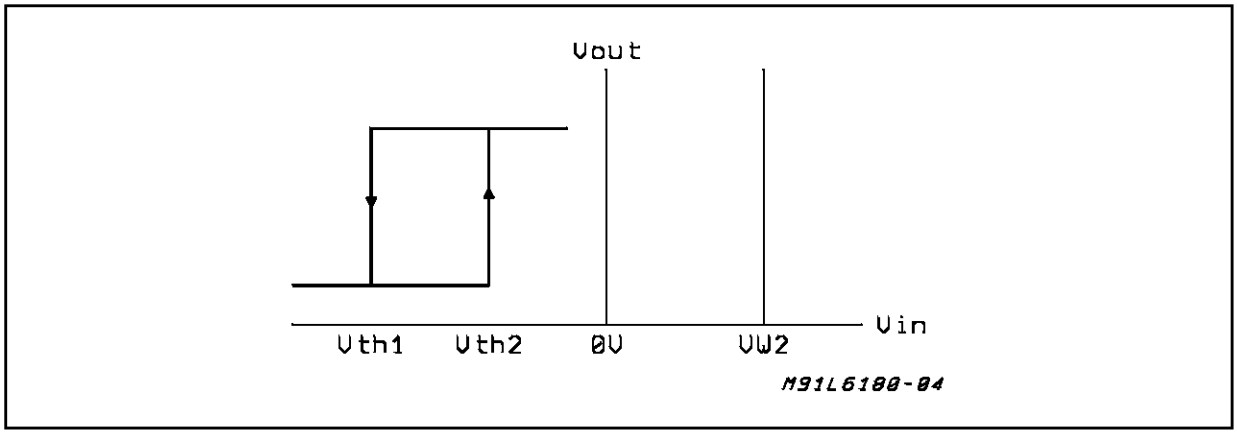


Figure 5: Propagation Delay

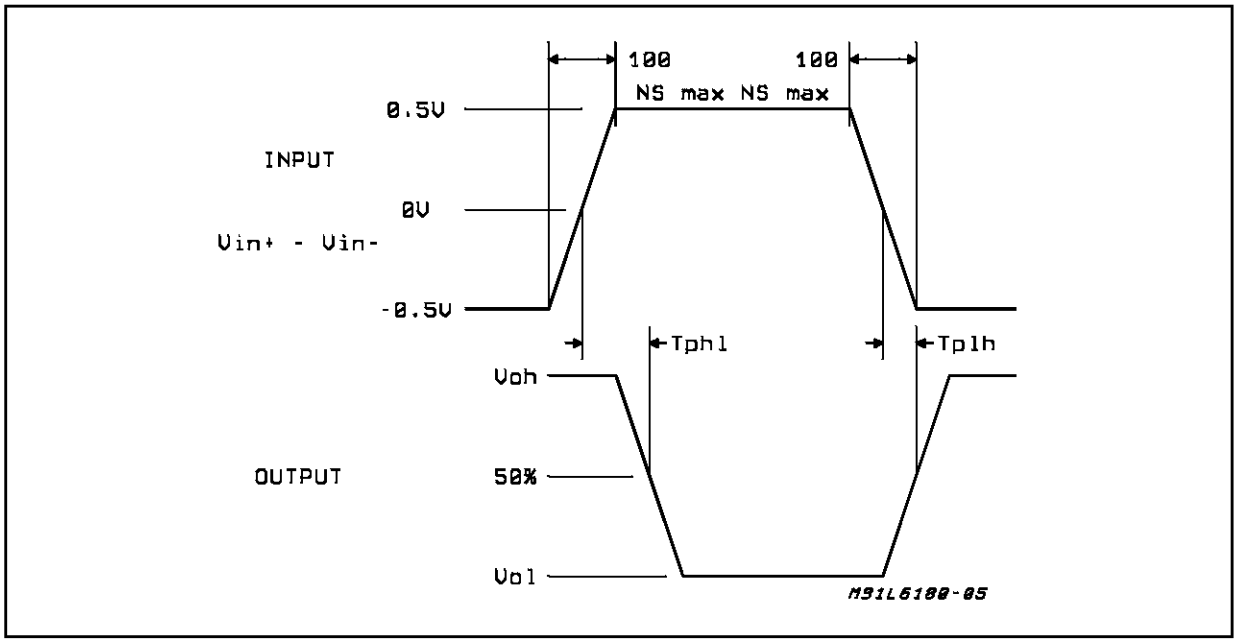


Figure 6: AC Test Circuit

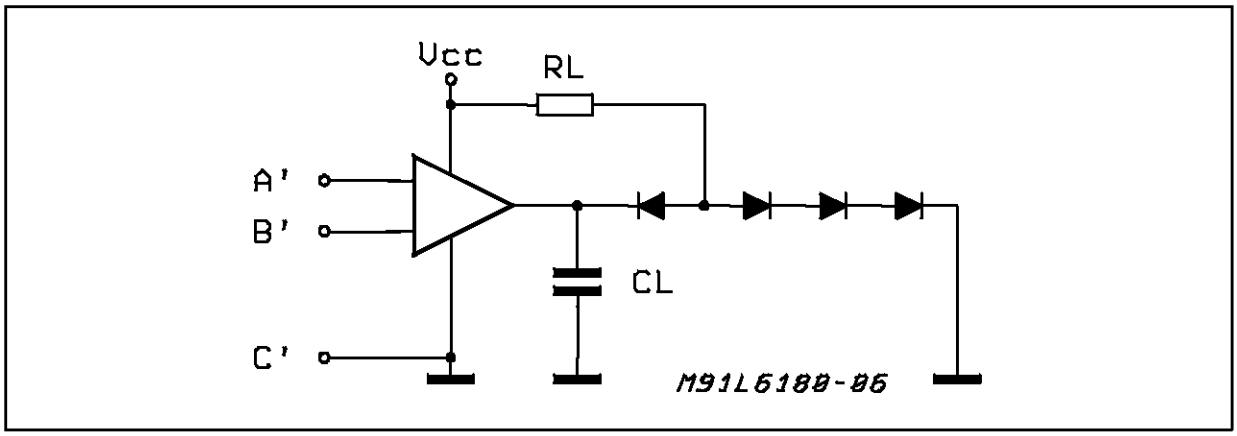


Figure 7: Receiver input Balance Measurement

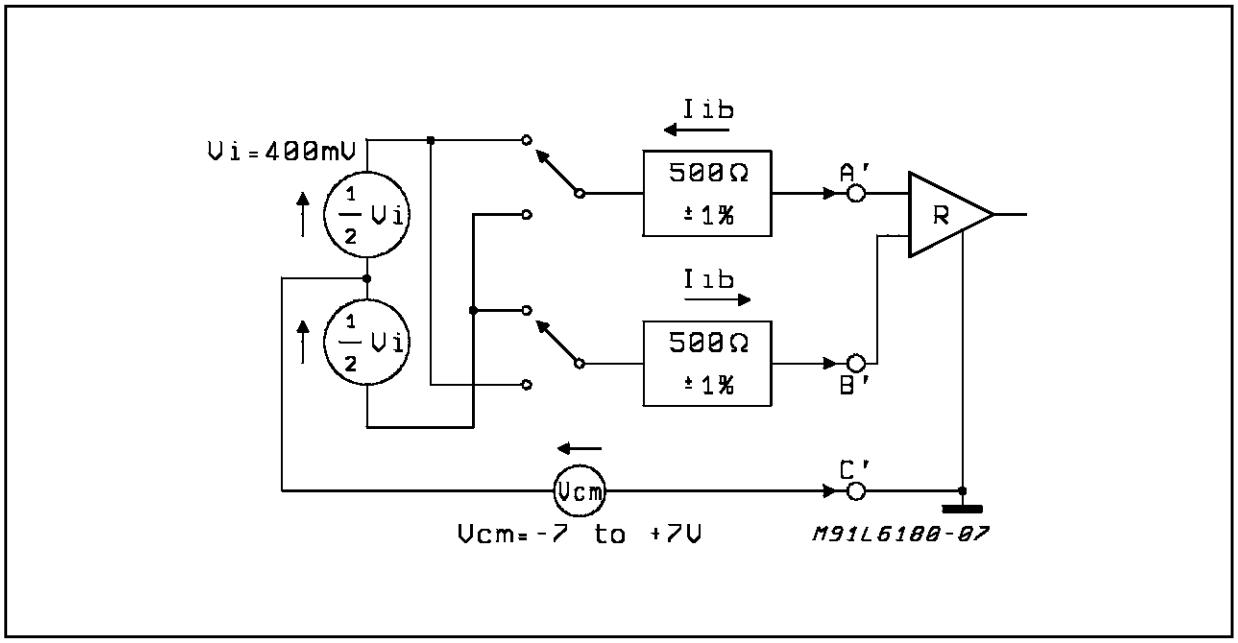
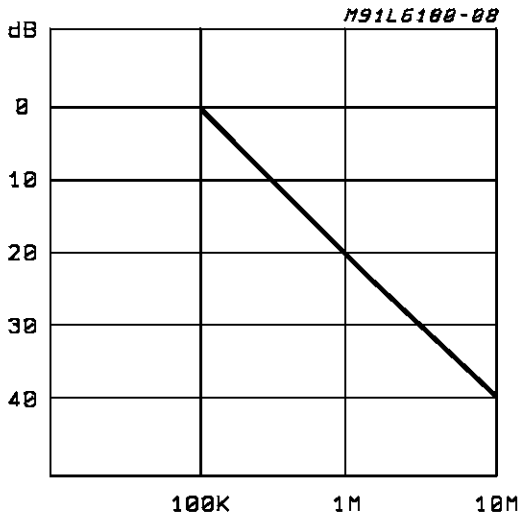


Figure 8: High Frequency Signal Rejection



INPUT BALANCE MEASUREMENT

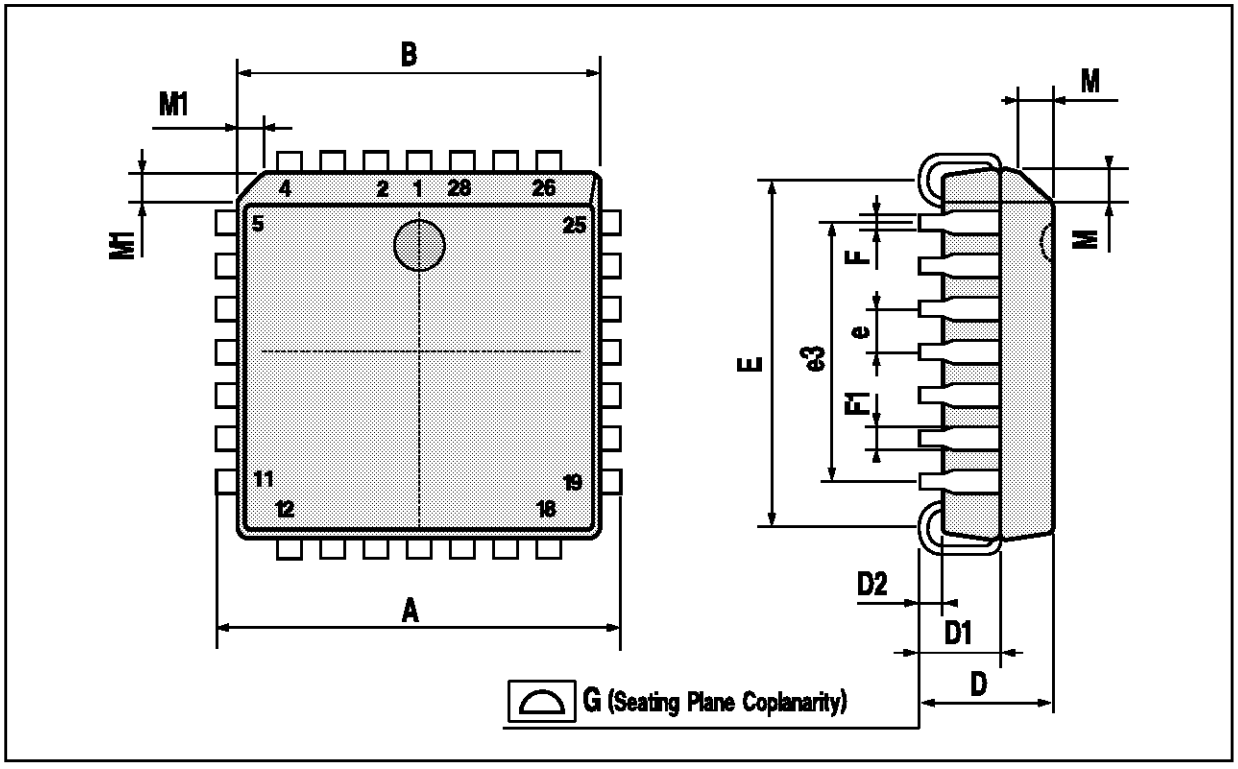
The balance of the receiver input voltage-current characteristics and bias voltages shall be such that the receiver will remain in the intended binary state when a differential voltage Vi of 400mV is applied through 500Ω ±1% to each input terminal, as shown above, and Vcm is varied between -7 and +7V.

When the polarity of Vi is reversed, the opposite binary state shall be maintained under the same conditions. Maintain input balance with input B common with another receiver.

The voltage input (V_{IN}) rejection is checked at the center point between the High Operating Threshold (V_{th2}) and the Low OperatingThreshold (V_{th1})

PLCC28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	



DIP28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130