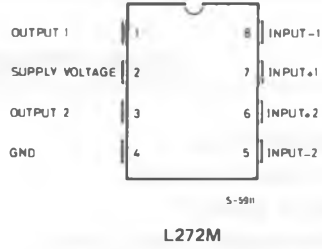
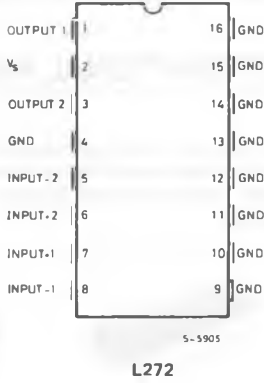
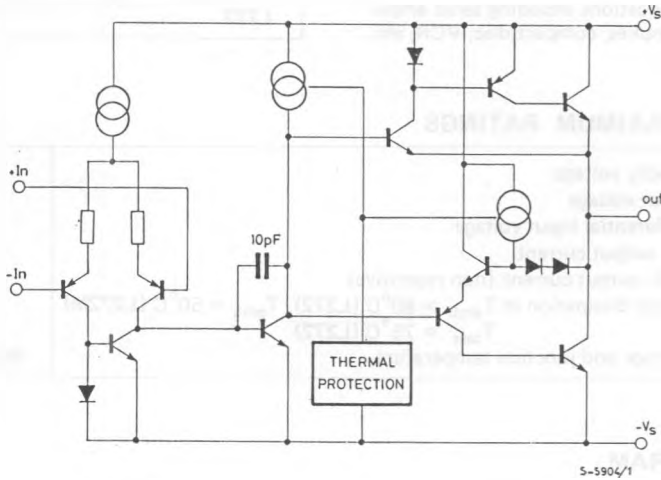


CONNECTION DIAGRAM

(Top view)



SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j-case}$	Thermal resistance junction-pins	max	15°C/W	* 70°C/W
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS ($V_s = 24V$, $T_{amb} = 25^\circ C$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage		4		28	V
I_s Quiescent drain current	$V_o = \frac{V_s}{2}$	$V_s = 24V$	8	12	mA
		$V_s = 12V$	7.5	11	mA
I_b Input bias current			0.3	2.5	μA
V_{os} Input offset voltage			15	60	mV
I_{os} Input offset current			50	250	nA
SR Slew rate			1		V/ μs
B Gain-bandwidth product			350		KHz
R_i Input resistance		500			K Ω
G_v O.L. voltage gain	$f = 100Hz$	60	70		dB
	$f = 1KHz$		50		dB
e_N Input noise voltage	$B = 20KHz$		10		μV
I_N Input noise current	$B = 20KHz$		200		pA
CRR Common Mode rejection	$f = 1KHz$	60	75		dB
SVR Supply voltage rejection	$f = 100Hz$ $R_G = 10K\Omega$ $V_R = 0.5V$	$V_s = 24V$	70		dB
		$V_s = \pm 12V$	62		dB
		$V_s = \pm 6V$	56		dB
V_o Output voltage swing		$I_p = 0.1A$	23		V
		$I_p = 0.5A$	22.5		V
C_s Channel separation	$f = 1KHz$; $R_L = 10\Omega$; $G_v = 30dB$ $V_s = 24V$ $V_s = \pm 6V$		60		dB
			60		dB
d Distortion	$f = 1KHz$ $V_s = 24V$	$G_v = 30dB$ $R_L = \infty$	0.5		%
T_{sd} Thermal shutdown junction temperature			145		$^\circ C$

Fig. 1 - Quiescent current vs. supply voltage

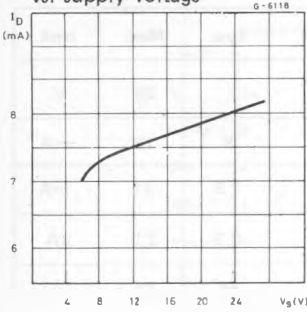


Fig. 2 - Quiescent drain current vs. temperature

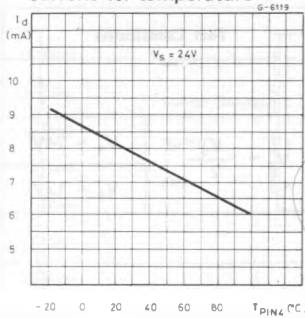


Fig. 3 - Open loop voltage gain

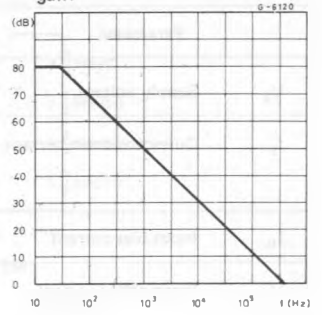


Fig. 4 - Output voltage swing vs. load current

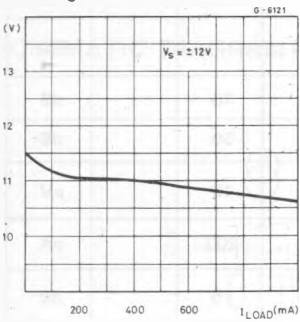


Fig. 5 - Output voltage swing vs. load current

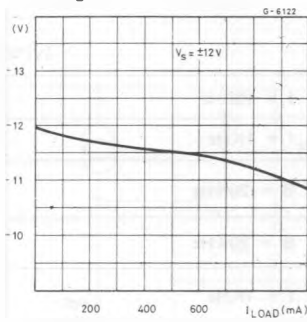


Fig. 6 - Supply voltage rejection vs. frequency

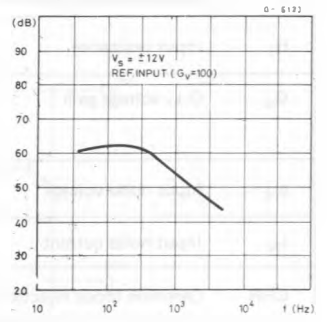


Fig. 7 - Channel separation vs. frequency

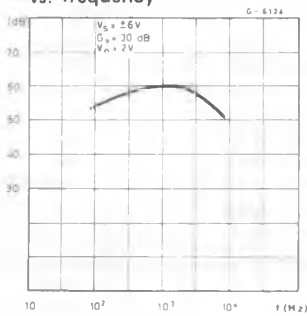
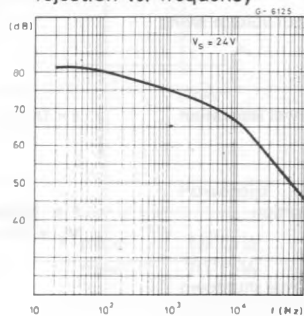


Fig. 8 - Common mode rejection vs. frequency



APPLICATION SUGGESTION

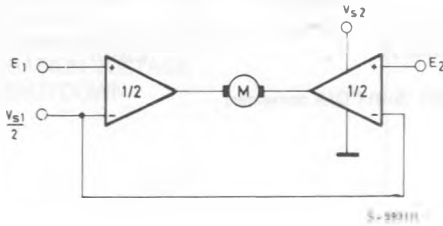
NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

– layout accuracy;

- A 100nF capacitor connected between supply pins and ground;
- bocherot cell (0.1 to 0.2 μ F + 1 Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μ P compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

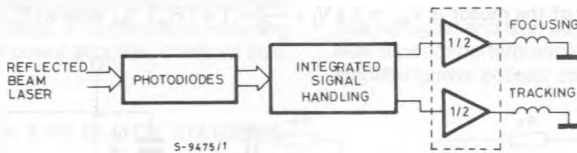


Fig. 11 - Capstan motor control in video recorders

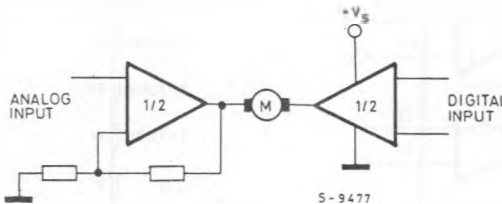
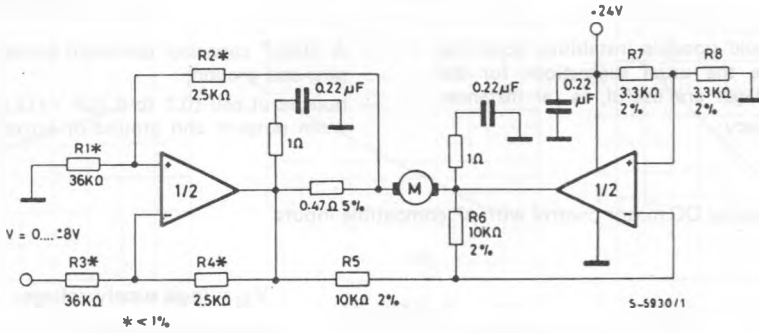


Fig. 12 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_x > \frac{2R_3 \cdot R_1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2 \left(V_i - \frac{V_s}{2} \right) + |R_o| \cdot I_M$ where $|R_o| = \frac{2R_3 \cdot R_1}{R_x}$ and I_M is the motor current.

