Data Sheet August 2000 File Number 3033.4

Radiation Hardened 2K x 8 CMOS PROM

The Intersil HS-6617RH is a radiation hardened 16K CMOS PROM, organized in a 2K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and is designed to be functionally equivalent to the HM-6617. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structure, such as the HS-80C85RH or HS-80C86RH. The output enable control ($\overline{G}$) simplifies microprocessor system interfacing by allowing output data bus control, in addition to, the chip enable control. Synchronous operation of the HS-6617RH is ideal for high speed pipe-lined architecture systems and also in synchronous logic replacement functions.

Applications for the HS-6617RH CMOS PROM include low power microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95708. A “hot-link” is provided on our homepage for downloading.
http://www.intersil.com/spacedefense/space.htm

Ordering Information

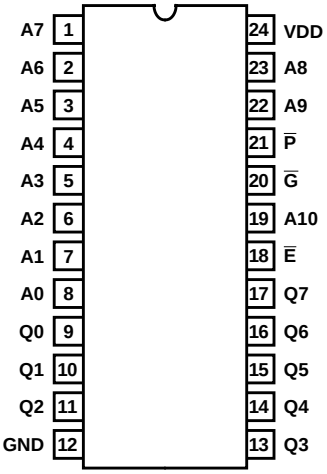
ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^{o}C)
5962R9570801QJC	HS1-6617RH-8	-55 to 125
5962R9570801QXC	HS9-6617RH-Q	-55 to 125
5962R9570801VJC	HS1-6617RH-Q	-55 to 125
5962R9570801VXC	HS9-6617RH-Q	-55 to 125
HS1-6617RH/PROTO	HS1-6617RH/PROTO	-55 to 125
HS9-6617RH/PROTO	HS9-6617RH/PROTO	-55 to 125

Features

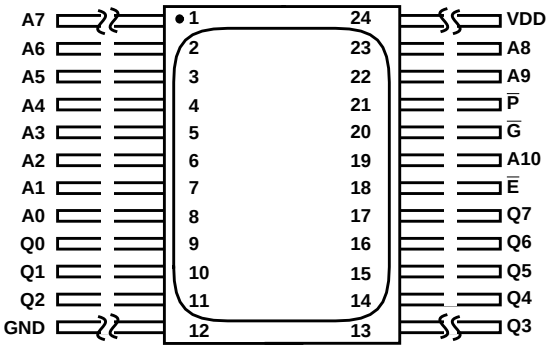
- Electrically Screened to SMD # 5962-95708
- QML Qualified per MIL-PRF-38535 Requirements
- Total Dose . . . . . 100 krad(Si) (Max)
- Latch-Up Free. . . . . >1 x 10^{12} rad(Si)/s
- Field Programmable
- Functionally Equivalent to HM-6617
- Pin Compatible with Intel 2716
- Low Standby Power . . . . . 1.1mW (Max)
- Low Operating Power . . . . . 137.5mW/MHz (Max)
- Fast Access Time . . . . . 100ns (Max)
- TTL Compatible Inputs/Outputs
- Synchronous Operation
- On Chip Address Latches
- Three-State Outputs
- Nicrome Fuse Links
- Easy Microprocessor Interfacing
- Military Temperature Range . . . . . -55^{o}C to 125^{o}C

Pinouts

24 LEAD CERAMIC DUAL-IN-LINE (SBDIP)
MIL-STD-1835 CDIP2-T24
TOP VIEW

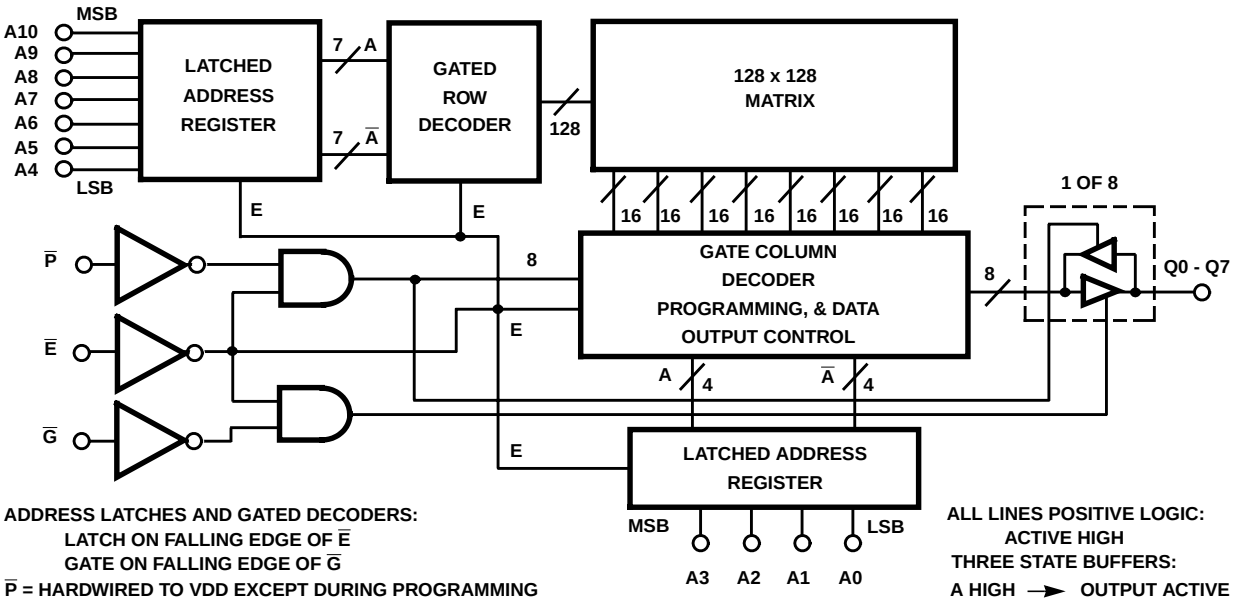


24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP4-F24
TOP VIEW



PIN	DESCRIPTION
A	Address Input
Q	Data Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program Enable ($\overline{P}$ Hardwired to VDD, except during programming)

Functional Diagram



ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF $\overline{E}$
GATE ON FALLING EDGE OF $\overline{G}$
$\overline{P}$ = HARDWIRED TO VDD EXCEPT DURING PROGRAMMING

ALL LINES POSITIVE LOGIC:
ACTIVE HIGH
THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

TRUTH TABLE

$\overline{E}$	$\overline{G}$	MODE
0	0	Enabled
0	1	Output Disabled
1	X	Disabled

Timing Waveform

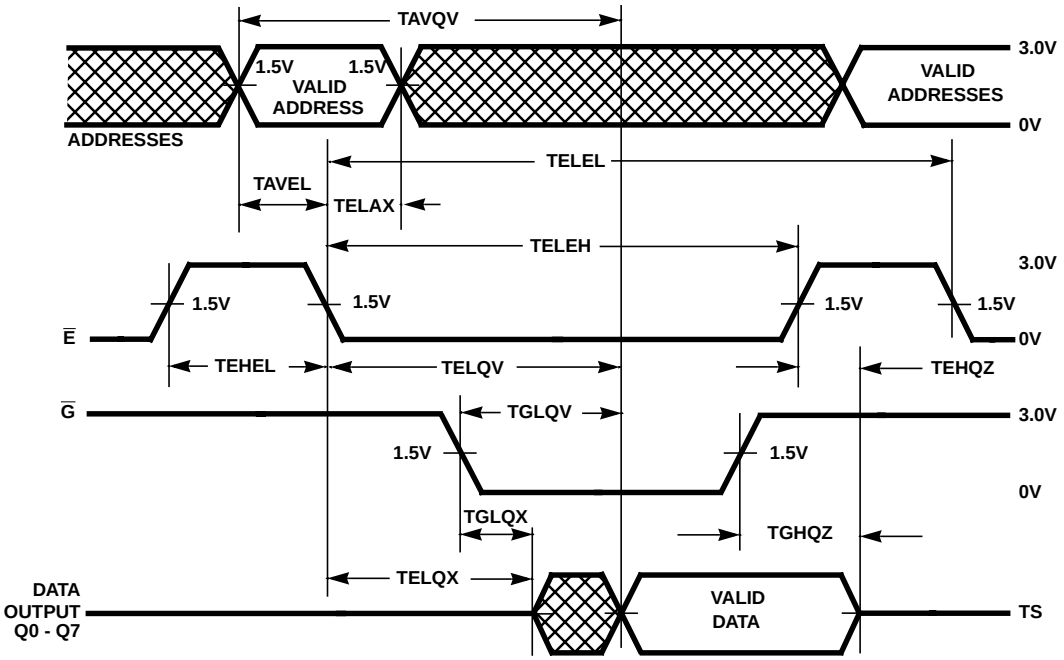
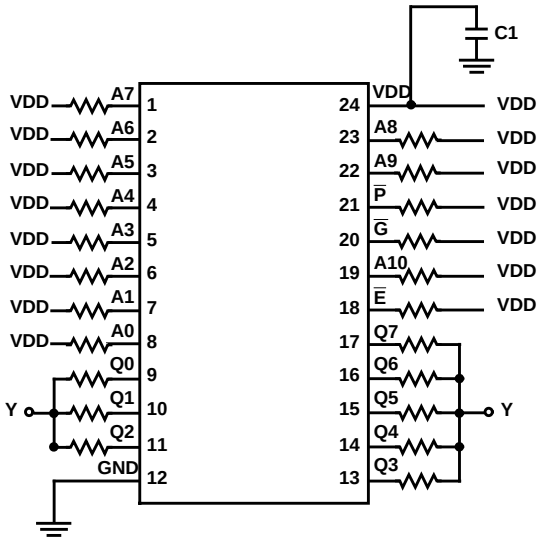


FIGURE 1. READ CYCLE

Burn-In Circuits

HS-6617RH 24 LEAD SBDIP AND FLATPACK

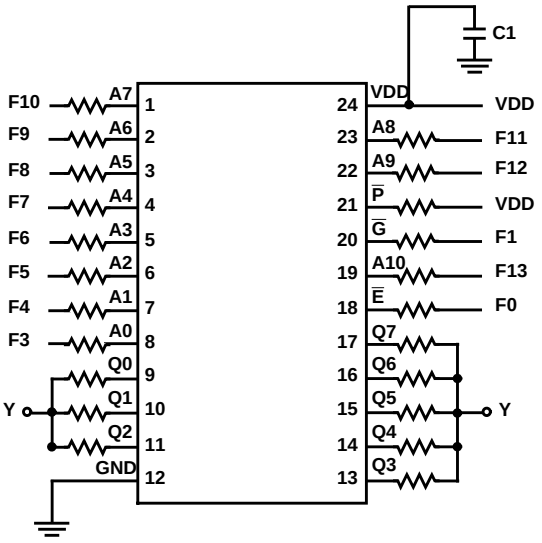


STATIC CONFIGURATION

NOTES:

1. VDD = 6.0V ± 0.5V
2. C1 = 0.01µF (Min)
3. All Resistors = 47kΩ ± 5%
4. Y = 2.7V ± 10%

HS-6617RH 24 LEAD SBDIP AND FLATPACK



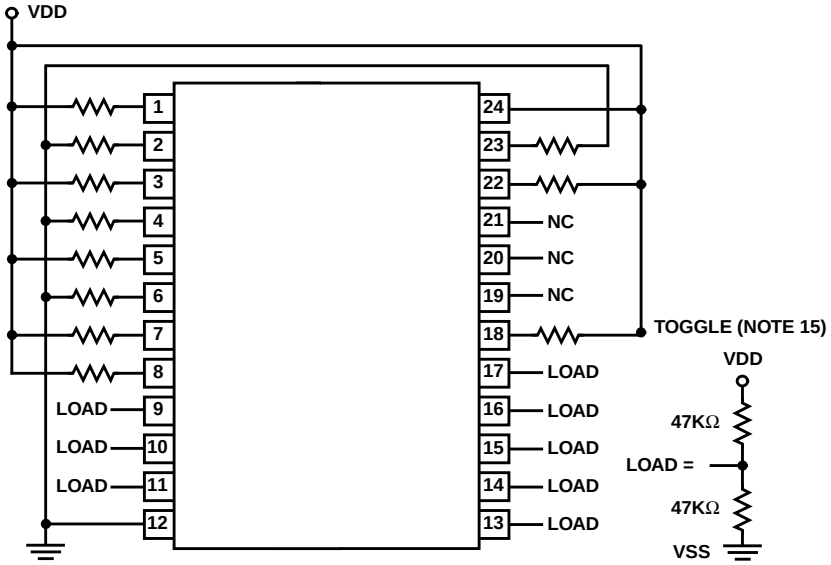
DYNAMIC CONFIGURATION

NOTES:

5. VDD = 6.0V ± 0.5V
6. VIH = 4.5V± 10%
7. VIL = 0.8V (Max)
8. C1 = 0.01µF (Min)
9. All Resistors = 47kΩ ± 5%
10. F0 = 100KHz ± 10%, 40 - 60% duty cycle
11. F1 = F0/2 . . . F13 = F12/2
12. Y = 2.7V ± 10%

Irradiation Circuit

HS-6617RH 24 LEAD FLATPACK



NOTES:

13. Power Supply: VDD = 5.5V
14. All Registors = 47kΩ
15. Pin 18 is toggled from VSS to VDD then back to VSS and held at VSS during irradiation.

Die Characteristics

DIE DIMENSIONS:

164mils x 250mils x 19mils ±1mils

INTERFACE MATERIALS:

Glassivation:

Type: SiO_2
Thickness: 8kÅ ± 1kÅ

Top Metallization:

Type: Silicon-Aluminum
Thickness: 13kÅ ± 2kÅ

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

V_{DD}

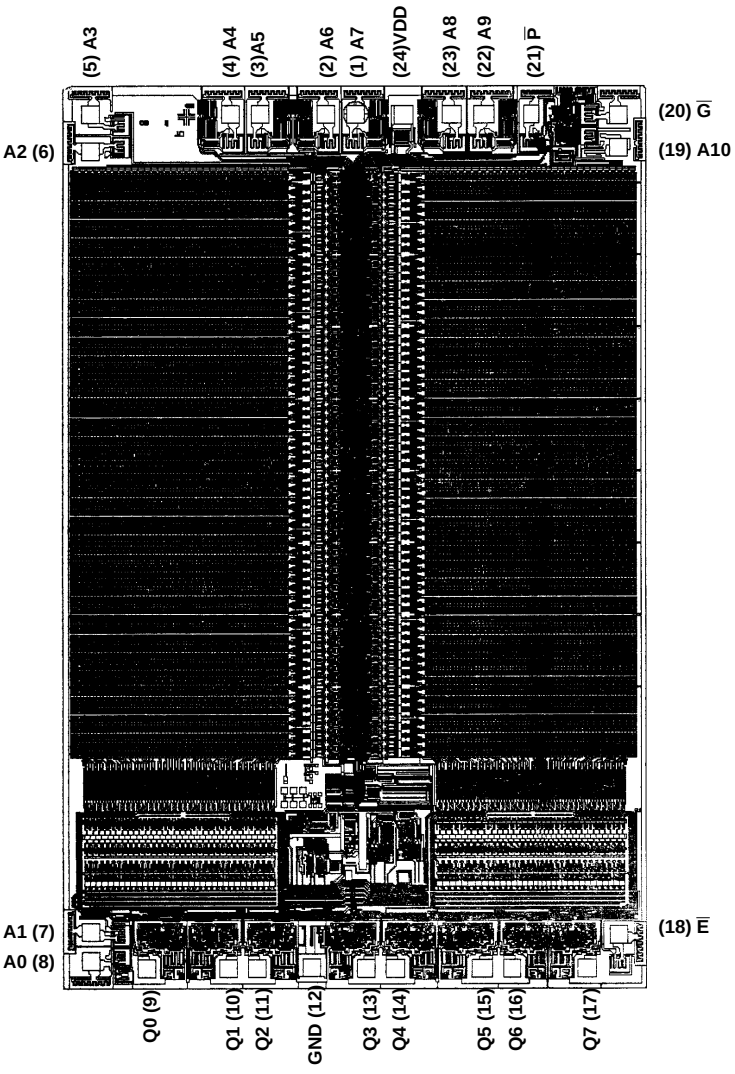
ADDITIONAL INFORMATION:

Worst Case Current Density:

1×10^5 A/cm^2

Metallization Mask Layout

HS-6617RH



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.