HM 65799

64 K × 4 with $\overline{OE}$ High Speed CMOS SRAM

Introduction

The HM 65799 is a high speed CMOS static RAM organized as 65,536 × 4 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast 20 ns are available with maximum power consumption of only 770 mW.

The HM 65799 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 71 % when the circuit is deselected.

Easy memory expansion is provided by two active low chip selects ($\overline{CS1}$, $\overline{CS2}$), an active low output enable ($\overline{OE}$) and three state drivers.

All inputs and outputs of the HM 65799 are TTL compatible and operate from single 5 V supply thus simplifying system design.

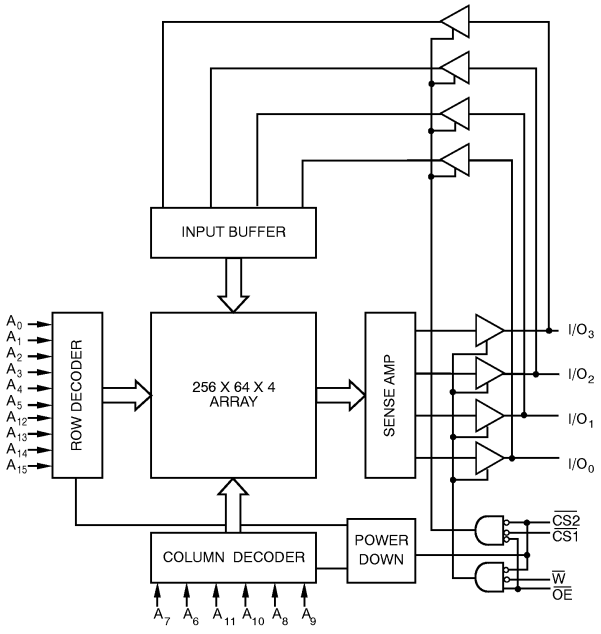
The HM 65799 is processed following the test methods of MIL STD 883 and/or ESA/SCC 9000 making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

Features

- Fast access time
  Commercial/industrial : 20/25/35/45/55 ns (max)
  Military : 25/35/45/55 ns (max)
- Low power consumption
  Active : 770 mW
  Standby : 220 mW
- Wide temperature range : –55°C to + 125°C
- 300 mils width package
- TTL compatible inputs and outputs
- Asynchronous
- Capable of withstanding greater than 2000V electrostatic discharge
- Output enable
- Single 5 volt supply

Interface

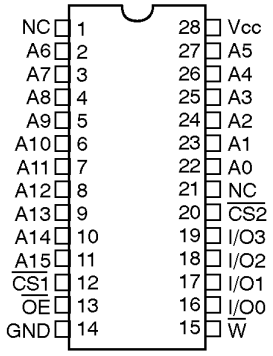
Block Diagram



HM 65799

Pin Configuration

Plastic 300 mils, 28 pins, DIL
Ceramic 300 mils, 28 pins, DIL
SO/SOJ 300 mils, 28 pins



Pinout DIL/SO 24 pins (top view)

Pin Names

A0–A15: Address inputs		$\overline{OE}$	: Output enable
I/00–I/03	: Input/Output	W	: Write enable
$\overline{CS1}$	: Chip select 1	Vcc	: Power
$\overline{CS2}$	: Chip Select 2	GND	: Ground

Truth Table

$\overline{CS1}$	$\overline{CS2}$	$\overline{W}$	$\overline{OE}$	INPUT/ OUTPUTS	MODE
H X	X H	X X	X X	High Z	Deselect/ Power Down
L	L	H	L	Data Out	Read
L	L	L	X	Data In	Write
L	L	H	H	High Z	Deselected

L = Low, H = High, X = H or L, Z = High impedance.

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential : . . . . . –0.5 V to +7.0 V
DC input voltage : . . . . . –3.0 V to +7.0 V
DC output voltage in high Z state : . . . . . –0.5 V to +7.0 V

Storage temperature : . . . . . –65°C to +150°C
Output current into outputs (low) : . . . . . 20 mA
Electro Static Discharge Voltage . . . . . > 2000 V
(MIL STD 883C METHOD 3015-5)

Operating Range

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	– 0°C to + 70°C

Recommended DC Operating Conditions

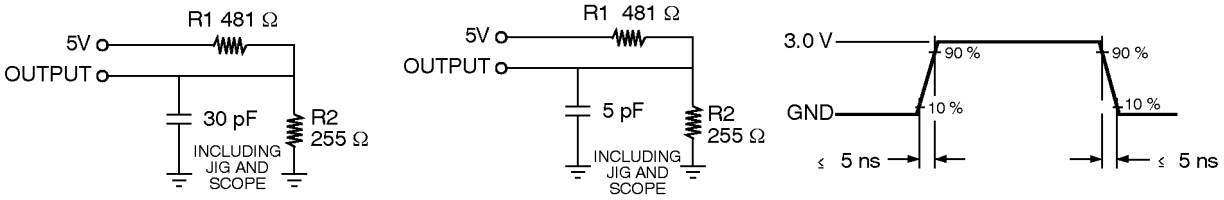
PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

Capacitance

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (1)	Input capacitance	–	–	5	pF
Cout (1)	Output capacitance	–	–	7	pF

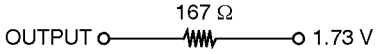
Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

AC Test Loads and Waveforms



(a) **(b)**

Equivalent to : THEVENIN EQUIVALENT



DC Parameters

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 10.0	–	10.0	µA
IOZ (2)	Output leakage current	– 10.0	–	10.0	µA
IOS (3)	Output short circuit current	–	–	– 350.0	mA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (5)	Output high voltage	2.4	–	–	V

Note : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = –4.0 mA.

Consumption for Commercial (–5) Specification

SYMBOL	PARAMETER	65799 F–5	65799 H–5	65799 K–5	65799 M–5	65799 N–5	UNIT	VALUE
ICCSB (6)	Standby supply current	40	35	35	35	35	mA	max
ICCSB1 (8)	Standby supply current	20	20	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	140	120	120	120	120	mA	max

Consumption for Industrial (–9) and Military (–2) Specification

SYMBOL	PARAMETER	65799 F–9	65799 H–9/–2	65799 K–9/–2	65799 M–9/–2	65799 N–9/–2	UNIT	VALUE
ICCSB (6)	Standby supply current	40	35	35	35	35	mA	max
ICCSB1 (8)	Standby supply current	20	20	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	150	130	130	130	130	mA	max

Note : 6. $\overline{CS} \geq$ VIH, a pull-up resistor to Vcc on the $\overline{CS}$ is required to keep the device unselected during the Vcc power-up. Otherwise IccSB will exceed the above values. Min duty cycle = 100 %.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
8. $\overline{CS} \geq$ Vcc – 0.3 V Iout = 0 mA.

AC Parameters

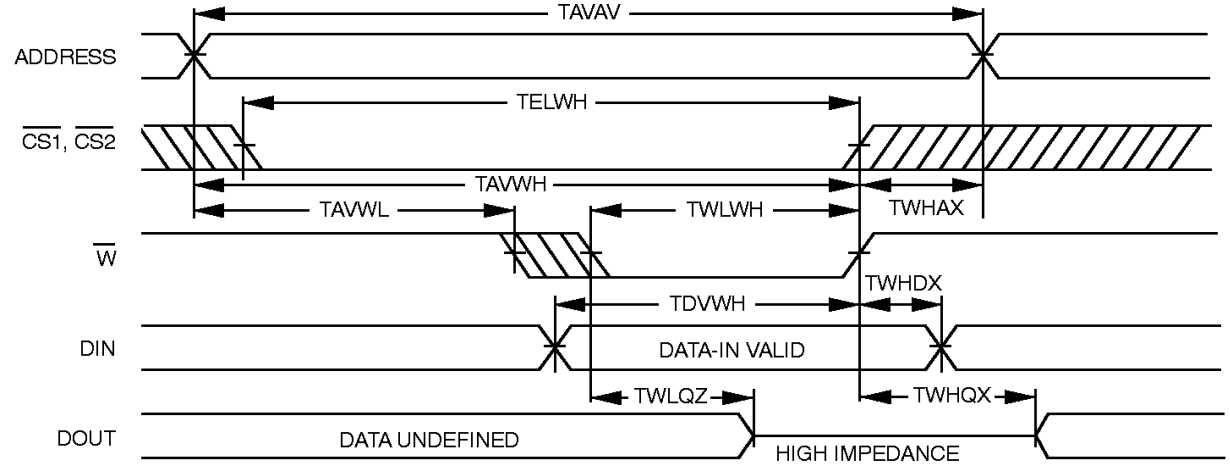
Input pulse levels : . . . . . Gnd to 3.0 V
Input rise : . . . . . 5 ns
Input timing reference levels : . . . . . 1.5 V
Output loading IOL/IOH *(see figure 1a and 1b)* : . . . . . +30 pF

Write Cycle : Commercial, Industrial and Military Specification

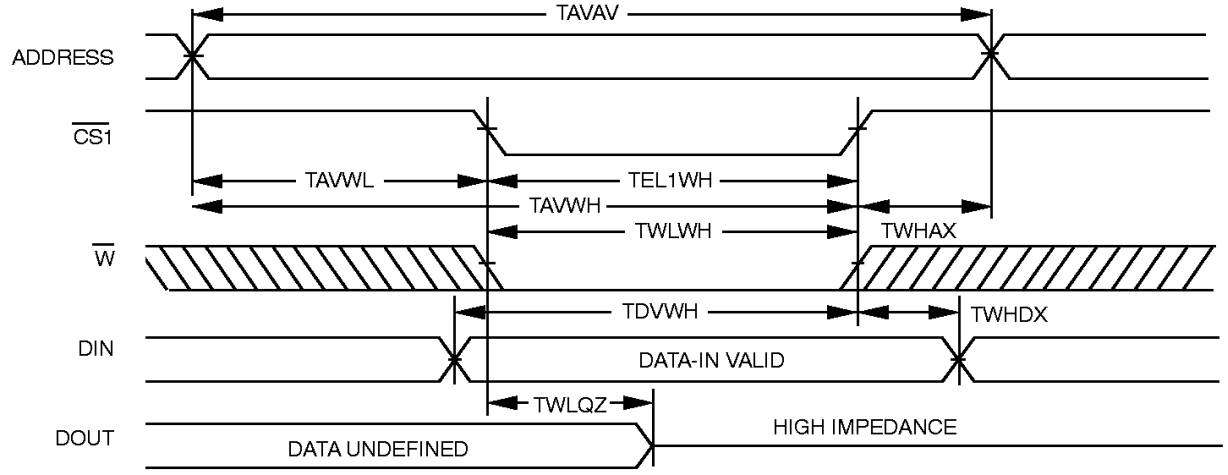
SYMBOL	PARAMETER	65799 F–5/–9	65799 H–5/–9 /–2	65799 K–5/–9 /–2	65799 M–5/–9 /–2	65799 N–5/–9 /–2	UNIT	VALUE
TAVAV	Write cycle time	20	20	30	40	50	ns	min
TAVWL	Address set–up time	0	0	0	0	0	ns	min
TAVWH	Address valid to write end	15	20	25	35	40	ns	min
TDVWH	Data set–up time	10	15	17	20	25	ns	min
TELWH	$\overline{CS1}$, $\overline{CS2}$ low to write end	15	20	30	40	50	ns	min
TWLQZ(9)	Write low to high Z	10	13	15	20	25	ns	max
TWLWH	Write pulse width	15	20	25	30	35	ns	min
TWHAX	Address hold from write end	0	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	0	ns	min
TWHQX (9)	Write high to low Z	3	3	3	3	3	ns	min

Note : 9. The data input set-up and hold timing should be referenced to rising edge of the signal that terminates the write.

Write Cycle 1 : $\overline{W}$ Controlled (note 10)



Write Cycle 2 : $\overline{CS}$ controlled (note 10)

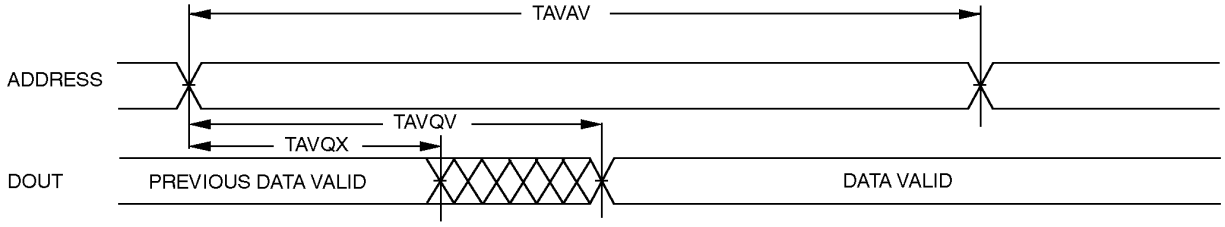


Note : 10. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write.
Data out will be high impedance if $\overline{OE}$ = VIH.

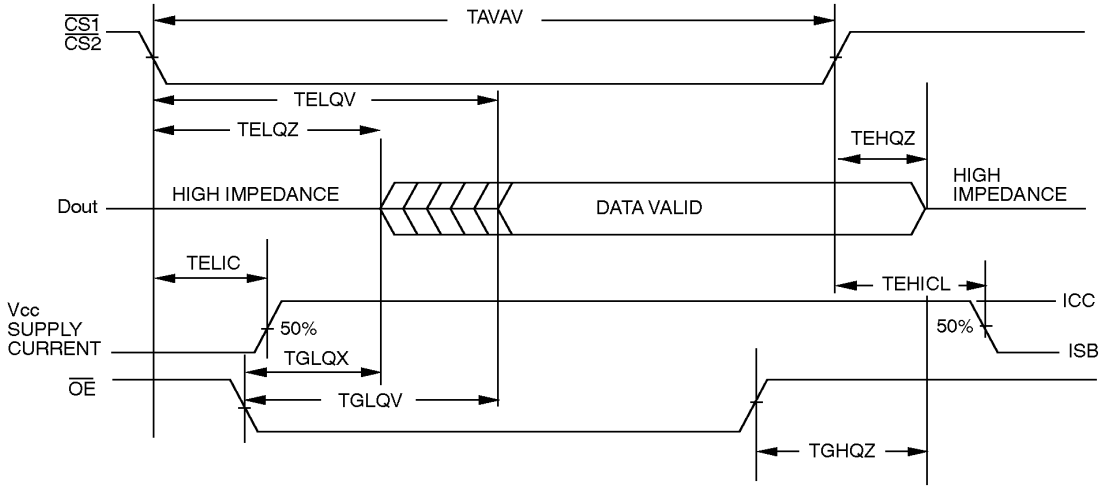
Read Cycle : Commercial, Industrial and Military Specification

SYMBOL	PARAMETER	65799 F–5/–9	65799 H–5/–9 /–2	65799 K–5/–9 /–2	65799 M–5/–9 /–2	65799 N–5/–9 /–2	UNIT	VALUE
TAVAV	READ cycle time	20	25	35	45	55	ns	min
TAVQV	Address access time	20	25	35	45	55	ns	min
TAVQX	Address valid to low Z	3	3	3	3	3	ns	min
TELQV	$\overline{CS1}$ and CS2 access time	20	25	35	45	55	ns	max
TELQX	$\overline{CS1}$ and CS2 low to low Z	3	3	3	3	3	ns	min
TEHQZ	$\overline{CS1}$ and CS2 high to high Z	10	13	15	20	25	ns	max
TGLQV	$\overline{OE}$ access time	10	15	20	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	13	15	20	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power up	20	25	35	45	55	ns	max

Read Cycle 1 : (note 11, 12, 13)



Read Cycle 2 : (note 11, 13)



Notes : 11. $\overline{W}$ is high for read cycle.
12. Device is continuously selected, $\overline{CS1}$ = VIL, $\overline{CS2}$ = VIL, $\overline{OE}$ = VIL.
13. Address valid prior or coincident with $\overline{CS1}$, $\overline{CS2}$ transition low.

Ordering Information

PACKAGE | DEVICE TYPE | GRADE | LEVEL

HM 3 65799 H −5 : R

65799: 64 K × 4 high speed static RAM with $\overline{OE}$

3:
0 – Chip form
1 – Ceramic 24 pins 300 mils
3 – Plastic 24 pins 300 mils
T – SOIC 24 pins 300 mils
U – SOJ 24 pins

H:
F = 20 ns
H = 25 ns
K = 35 ns
M = 45 ns
N = 55 ns

−5 : R:
–2 : Military
–5 : Commercial
–6 : 100% 25°C Probe
–9 : Industrial
/883 : MIL STD 883 Class B or S
DB : Dice Military program
R : Tape & Reel option
RD : Tape & Reel/Dry pack option
D : Dry pack option