HARRIS SEMICONDUCTOR

HIP2060

May 1997

60V, 10A Half Bridge Power MOSFET Array

Features

- **Two 10A Power MOS N-Channel Transistors**
- **Output Voltage to 60V**
- **$r_{DS(ON)}$ .....0.135Ω Max Per Transistor at V_{GS} = 15V**
- **$r_{DS(ON)}$ .....0.15Ω Max Per Transistor at V_{GS} = 10V**
- **Pulsed Current.....25A Each Transistor**
- **Avalanche Energy ..... 100mJ Each Transistor**
- **Grounded Tab Eliminates Heat Sink Isolation**

Description

The HIP2060 is a power half-bridge MOSFET array that consists of two matched N-Channel enhancement-mode MOS transistors. The advanced Harris PASIC2 process technology used in this product utilizes efficient geometries that provides outstanding device performance and ruggedness.

The HIP2060 is designed to integrate two power devices in one chip thus providing board layout area and heat sink savings for applications such as Motor Controls, Uninterruptible Power Supplies, Switch Mode Power Supplies, Voice Coil Motors, and Class D Power Amplifier.

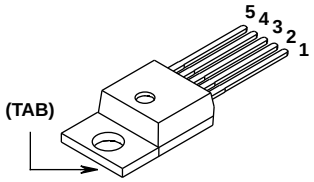
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HIP2060AS1	-40 to +125	5 Ld SIP	Z5.067C
HIP2060AS2	-40 to +125	5 Ld Gullwing SIP	Z5.067A

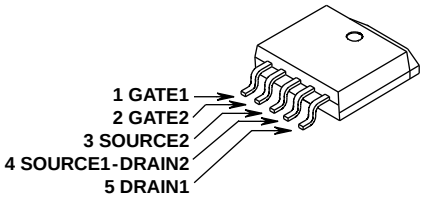
NOTE: When ordering use the entire part number.

Packages

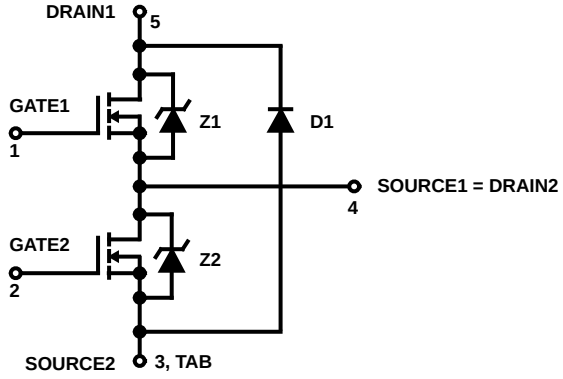
JEDEC TS-001AA (ALTERNATE VERSION)
HIP2060 AS1



JEDEC MO-169 HIP2060 AS2



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HIP2060	UNITS
Continuous Drain-Source Voltage Over Operating Junction and Case Temperature Range	V_{DS}	60	V
Drain-Gate Voltage	V_{DGR}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Source-Drain Diode Current (Note 2)	I_{SD}	10	A
Pulsed Drain Current, each Output, all Outputs on (Notes 1, 2)	I_{DM}	25	A
Continuous Drain Current, each Output, all Outputs on (Note 2)	I_{DS}	10	A
Single Pulse Avalanche Energy (Note 3) Refer to UIS Curve	E_{AS}	100	mJ
Continuous Power Dissipation at T_C = + 25°C (Infinite Heatsink)	P_D	46	W
Continuous Power Dissipation, Derate above T_C = + 25°C		0.37	W/°C
Thermal Information	θ_{JA}	60	°C/W
Operating Case Temperature Range	T_C	-40 to +125	°C
Junction and Storage Temperature Range	T_J, T_{STG}	-40 to +150	°C
Lead Temperature (For Soldering, 10s)(Lead Tips Only)	T_L	300	°C
Continuous Drain1-Source2 Voltage Over Operating Junction Temperature Range	V_{D1S2}	60	V

NOTES:
1. Pulse width limited by maximum junction temperature.
2. Drain current limited by package construction.
3. V_{DD} = 25V, Start T_J = + 25°C, L = 1.5mH, R_{GS} = 50Ω, R = 0. See Figures 2, 12, and 13.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3983.3**

Electrical Specifications

T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 100µA, V_{GS} = 0V	T_C = -40°C to +125°C	60	-	-	V
			T_C = 25°C	-	70	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA		1.8	2.3	2.7	V
Drain1-Source2 Breakdown Voltage (Across D1)	BV_{D1S2}	I_{D1S2} = 1µA, V_{G1S1}, V_{G2S2} = 0V	T_C = 25°C	-	105	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = 25°C	-	-	1	µA
Drain1-Source2 Current (Through D1)	I_{D1S2}	V_{D1S2} = 60V, V_{G1S1} = 0V, V_{G2S2} = 0V	T_C = 25°C	-	0.3	1	µA
			T_C = 125°C	-	1	-	µA
Drain-Source On-State Voltage (Note 1)	$V_{DS(ON)}$	I_D = 10A, V_{GS} = 15V		-	0.9	1.25	V
		I_D = 10A, V_{GS} = 10V		-	1.1	1.5	V
Forward Gate Current, Drain Short Circuited to Source	I_{GSSF}	V_{DS} = 0V, V_{GS} = 20V		-	-	100	nA
Reverse Gate Current, Drain Short Circuited to Source	I_{GSSR}	V_{DS} = 0V, V_{GS} = -20V		-	-	-100	nA
Drain-Source On Resistance (Note 1)	$r_{DS(ON)}$	V_{GS} = 15V, I_D = 10A	T_C = +25°C	-	0.09	0.135	Ω
		V_{GS} = 15V, I_D = 10A	T_C = +125°C	-	0.15	0.21	Ω
		V_{GS} = 10V, I_D = 10A	T_C = +25°C	-	0.11	0.15	Ω
		V_{GS} = 10V, I_D = 10A	T_C = +125°C	-	0.19	0.25	Ω
Forward Transconductance (Note 1)	G_{FS}	V_{DS} = 15V, I_D = 5A		-	4.5	-	S
Turn-On Delay Time (Note 2)	$t_{D(ON)}$	V_{DD} = 30V, R_L = 3Ω, I_D = 10A, V_{GS} = 10V, R_G = 50Ω, See Figure 14		-	4	-	ns
Rise Time (Note 2)	t_R			-	5	-	ns
Turn-Off Delay Time (Note 2)	$t_{D(OFF)}$			-	12	-	ns
Fall Time (Note 2)	t_F			-	6	-	ns
Total Gate Charge (Note 2)	$Q_{G(TOT)}$	V_{DS} = 50V, V_{GS} = 10V, I_D = 10A, See Figures 16 and 17		-	10.5	12.0	nC
Gate-Source Charge (Note 2)	Q_{GS}			-	1.4	2.0	nC
Gate-Drain Charge (Note 2)	Q_{GD}			-	4.9	5.5	nC
Short-Circuit Input Capacitance, Common Source	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	230	-	pF
Short-Circuit Output Capacitance, Common Source for Upper FET	$C_{OSS(U)}$			-	150	-	pF
Short Circuit Output Capacitance Common Source for Lower FET	$C_{OSS(L)}$			-	225	-	pF
Short-Circuit Reverse Transfer Capacitance, Common Source	C_{RSS}			-	40	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	2.7	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	60	°C/W

Source-Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SOURCE-TO-DRAIN DIODE SPECIFICATIONS (ACROSS Z1 AND Z2)						
Forward Voltage (Note 1)	V_{SD}	I_{SD} = 10A, V_{GS} = 0V	-	1.05	1.25	V
Reverse Recovery Time (Across Z1)	$t_{RR(S1-D1)}$	I_{SD} = 10A, dI_{SD}/dt = 100A/µs	-	50	-	ns
Reverse Recovery Time (Across Z2)	$t_{RR(S2-D2)}$	I_{SD} = 10A, dI_{SD}/dt = 100A/µs	-	75	-	ns
SOURCE2-TO-DRAIN1 DIODE SPECIFICATIONS D (ACROSS D1)						
Forward Voltage (Note 1)	V_{SD}	I_{SD} = 10A, V_{GS} = 0V	-	8.5	9.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 10A, dI_{SD}/dt = 100A/µs	-	200	-	ns
DEVICE MATCHING						
Drain-Source On Resistance Match	$r_{DS(ON)M}$	V_{GS} = 10V, I_D = 10A, T_C = +25°C	-	90	-	%

NOTES:

1. Pulse test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
2. Independent of operating temperature.

Typical Performance Curves

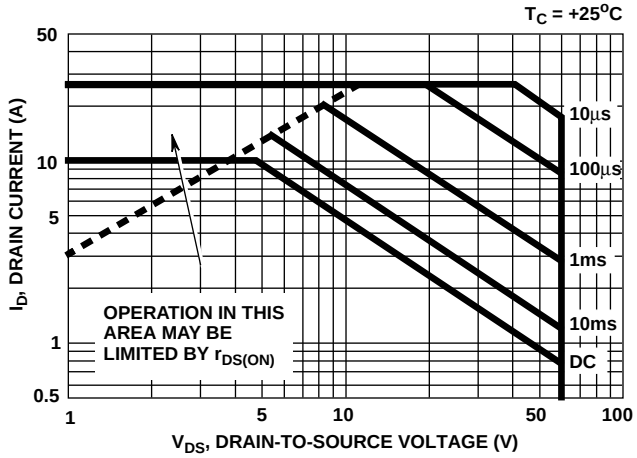


FIGURE 1. SAFE-OPERATING AREA CURVE

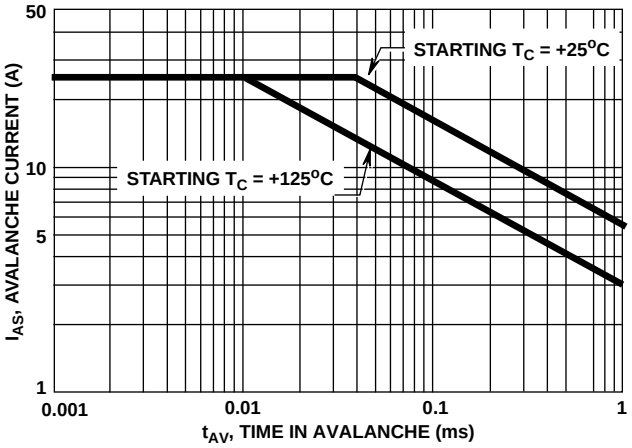


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

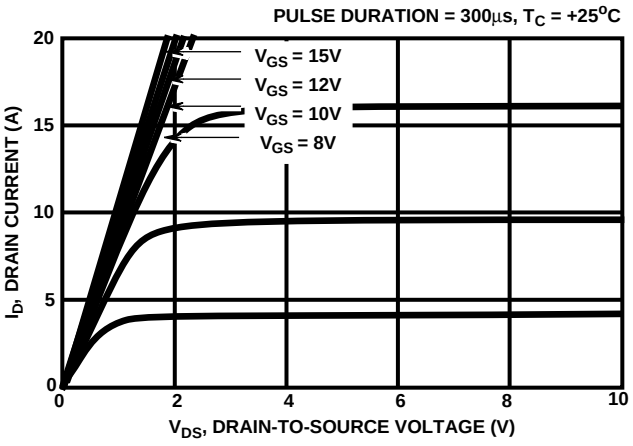


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

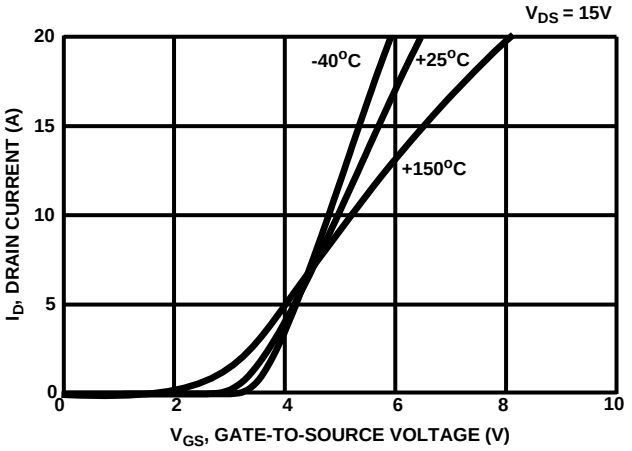


FIGURE 4. TYPICAL TRANSFER CHARACTERISTICS

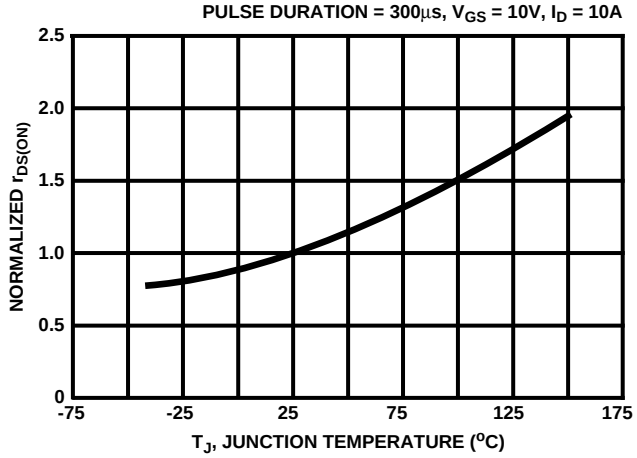


FIGURE 5. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

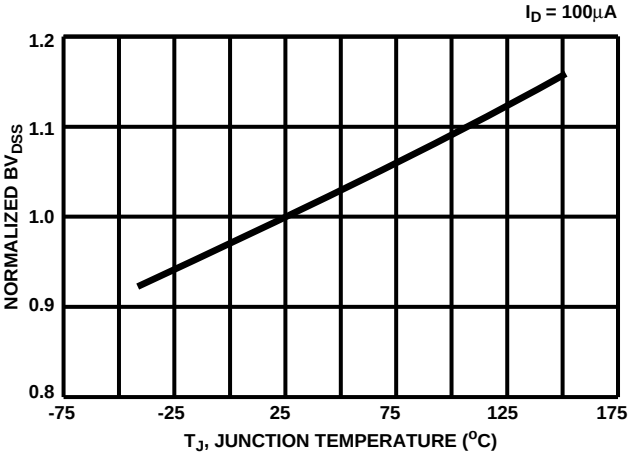


FIGURE 6. NORMALIZED BV_{DSS} vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

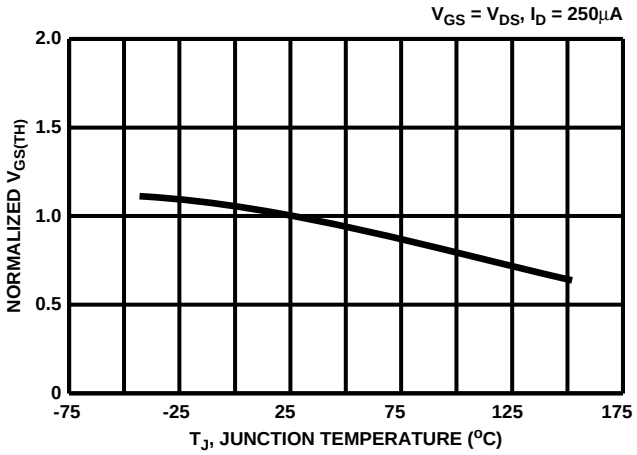


FIGURE 7. NORMALIZED $V_{GS(TH)}$ vs JUNCTION TEMPERATURE

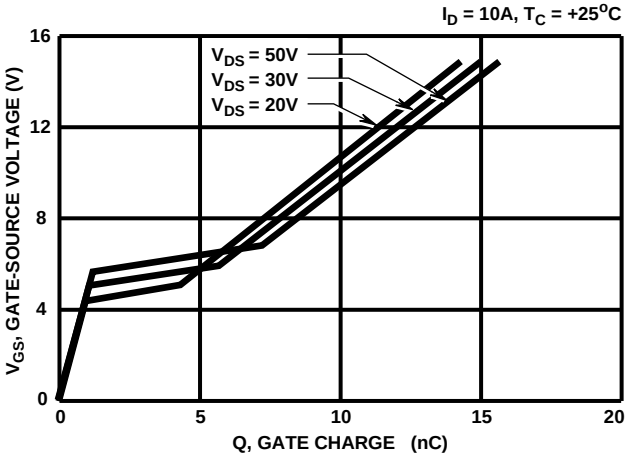


FIGURE 8. GATE-SOURCE VOLTAGE vs GATE CHARGE

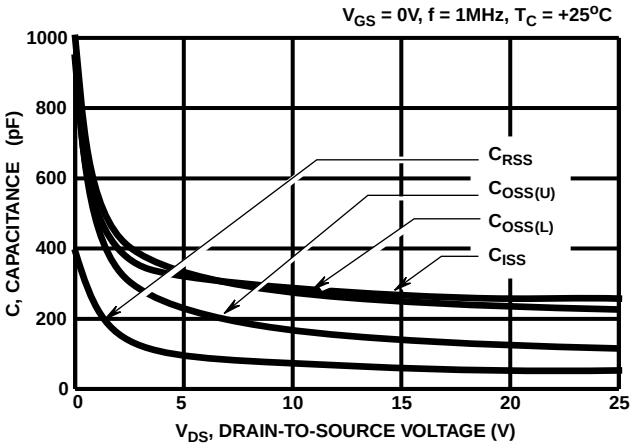


FIGURE 9. TYPICAL CAPACITANCE vs VOLTAGE

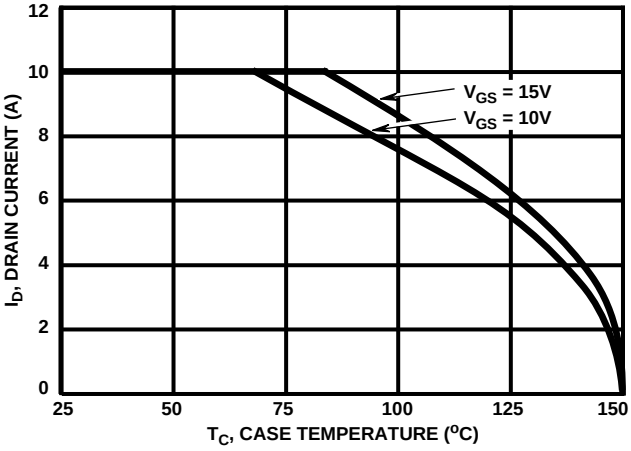


FIGURE 10. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

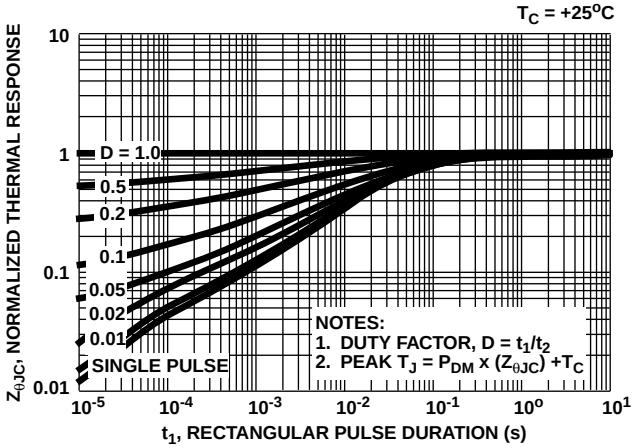


FIGURE 11. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

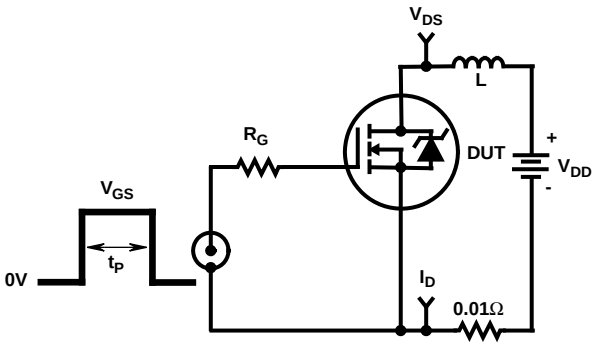


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

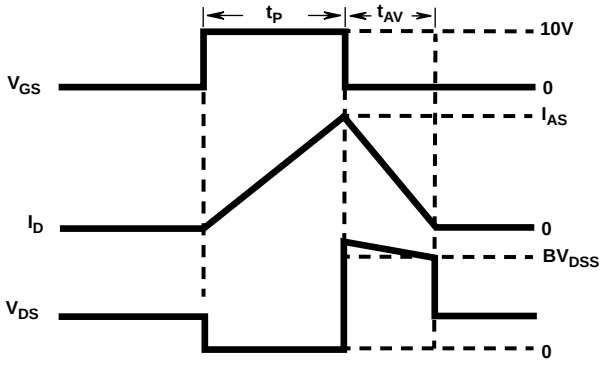


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

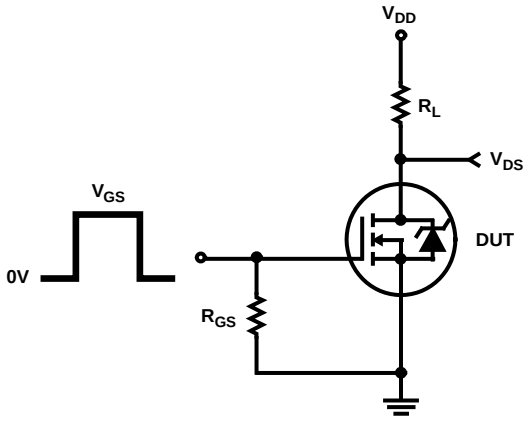


FIGURE 14. RESISTIVE SWITCHING TEST CIRCUIT

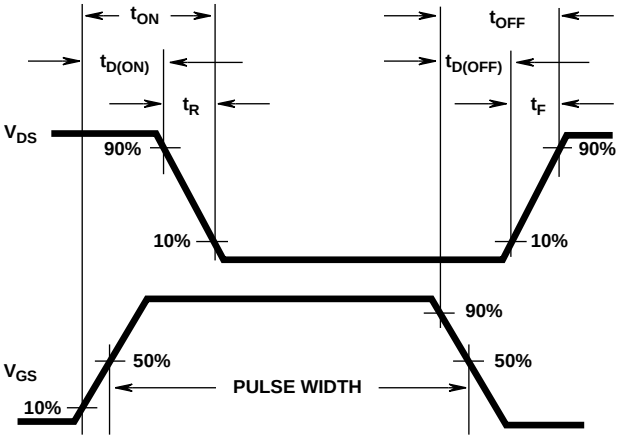


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

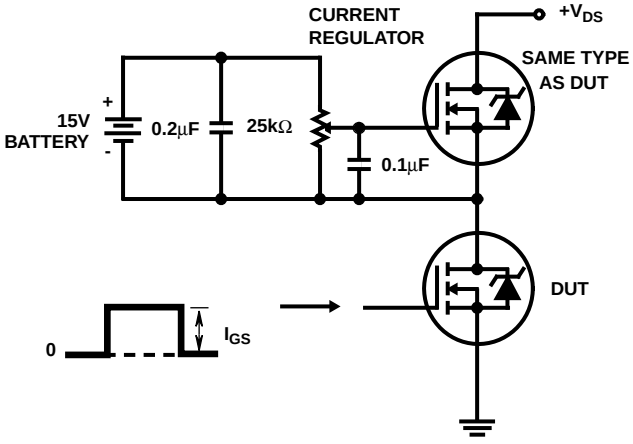


FIGURE 16. GATE CHARGE TEST CIRCUIT

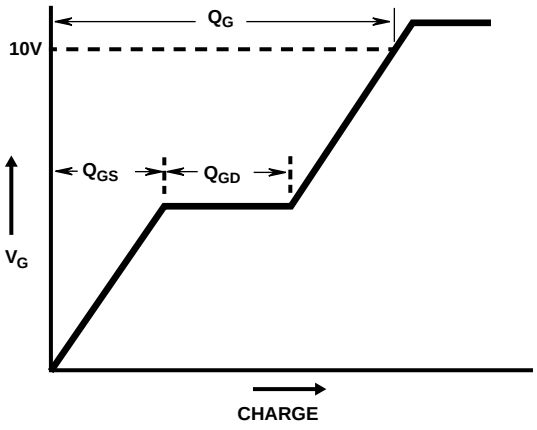


FIGURE 17. BASIC GATE CHARGE WAVEFORM

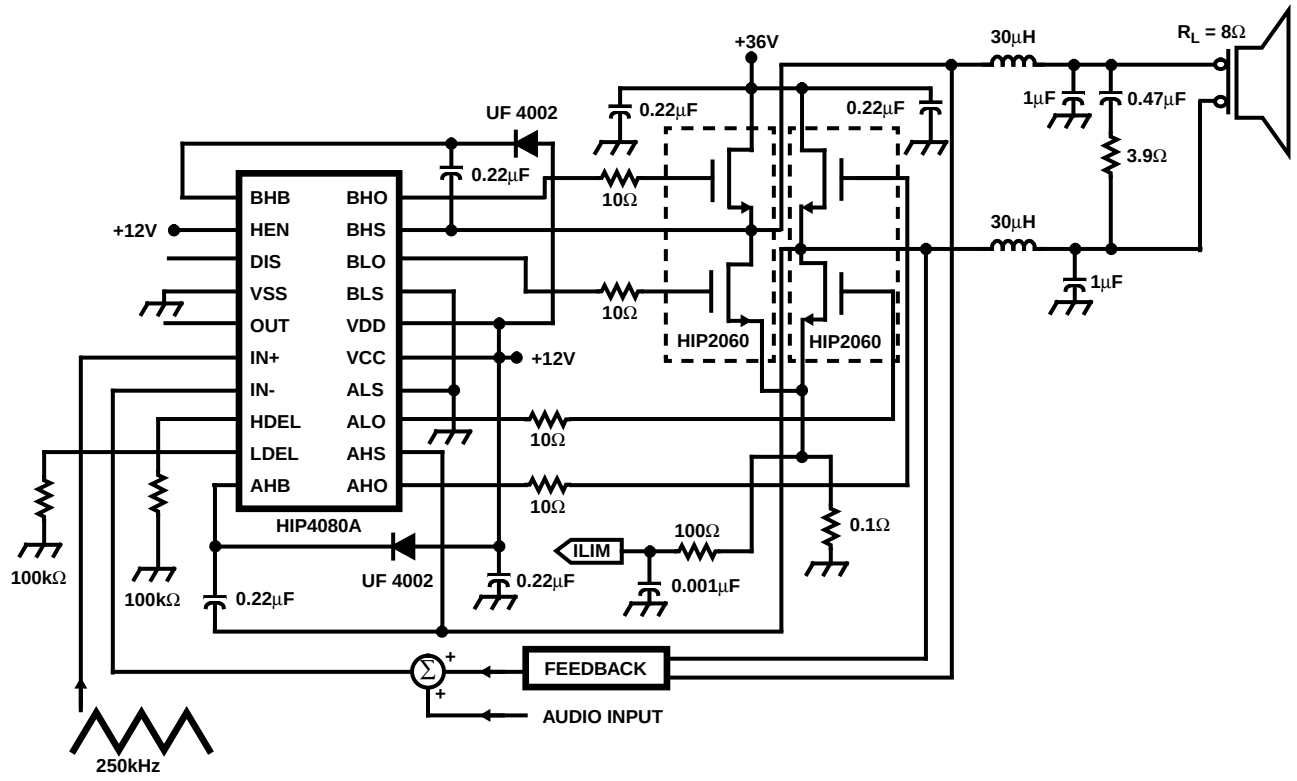


FIGURE 18. 70W SWITCHING AUDIO AMPLIFIER APPLICATION CIRCUIT

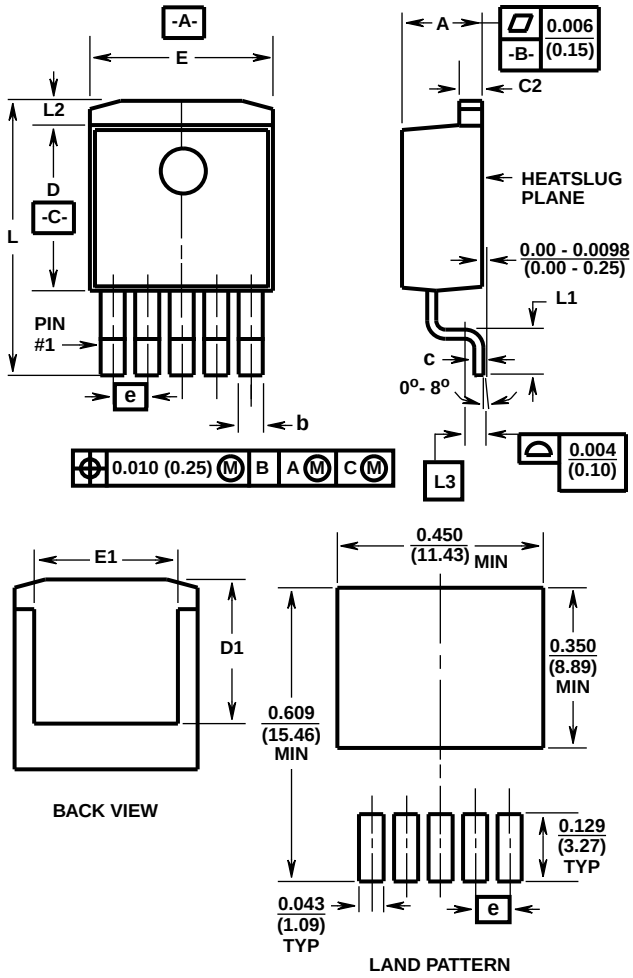
Device Model Netlist for HIP2060 Half Bridge Power MOSFET Array

```
.SUBCKT HIP2060   1   2   3   4   5
X1      6   1   7   3   HIP2060_1
LS1    5   6   7.5n
X2     7   2   8   3   HIP2060_1
LS2   7   4   7.5n
LS3   8   3   7.5n
.ENDS

.SUBCKT HIP2060_1   3   2   11   9
MOS1         4    2    1   1   NMOS1
JFET          10   1    4   J1
D1              5    6     D1
DBODY      1    10     D2
DBREAK    10   7     D3
DSUB         9    3     D4
VBREAK    7    1      DC 90
C21            2    1       850P
C23            2    10     50P
C24           2    4      1350P
RDRAIN    3    10     1.5e-03
RSOURCE    1    11   17.5e-03
FDSCHRG   4    2    VMEAS 1.0
E41            5    11   4   1   1.0
VPINCH    6    8     DC 10.0
VMEAS     8    11     DC 0.0
.MODEL NMOS1 NMOS LEVEL=3 (VTO=2.75 TOX=5e-08 KP=3.150e-03 PHI=0.65 GAMMA=2.55
+ VMAX=6.42e+07 NSUB=4.33e+16 THETA=0.60973 ETA=0.0015 KAPPA=1.275 L=1u W=5950u)
.MODEL J1 NJF (VTO=-15.0 BETA=10.736 LAMBDA=1.15e-02 PB=0.5848 IS=+1.0e-13
+ RD=3.53e-02 ALPHA=0.2)
.MODEL D1 D (IS=1.0e-15 N=0.03 RS=1.0)
.MODEL D2 D (IS=3.0e-13 RS=2.5e-03 TT=20N CJO=350e-12)
.MODEL D3 D (IS=1.0e-13 N=1.0 RS=2.0)
.MODEL D4 D (IS=1.0e-13 RS=2.0e-03 CJO=197e-12)
.ENDS
```

NOTE: For further discussion of the PSPICE PowerFET Macromodel consult Spicing-up SPICE II Software for Power MOSFET Modeling, Harris Application Note AN8610

Single-In-Line Plastic Packages (SIP)



Z5.067A

5 LEAD PLASTIC SINGLE-IN-LINE PACKAGE SURFACE MOUNT "GULLWING" LEAD FORM

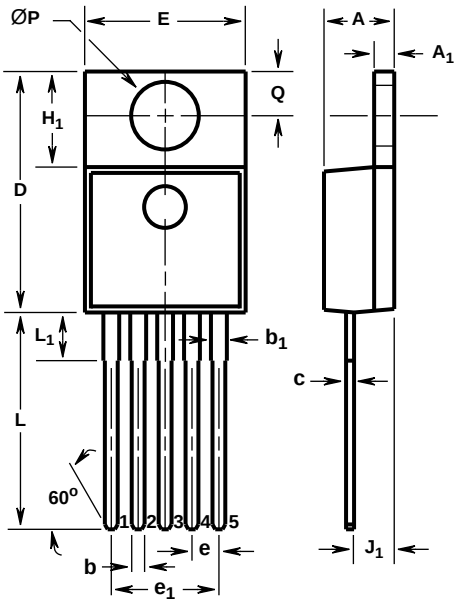
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
C2	0.048	0.055	1.22	1.39	5
D	0.350	0.370	8.89	9.39	-
E	0.395	0.405	10.04	10.28	-
D1	0.310	-	7.88	-	-
E1	0.310	-	7.88	-	-
L	0.549	0.569	13.95	14.45	-
L1	0.068	0.088	1.72	2.24	-
L2	0.045	0.055	1.15	1.40	-
L3	0.030 BSC		0.76 BSC		4
b	0.030	0.037	0.77	0.94	5, 6, 7
c	0.018	0.024	0.46	0.60	5
e	0.067 BSC		1.70 BSC		-

Rev.1 12/95

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-169AB, Issue A.
2. Controlling dimension: Inch.
3. Dimensioning and tolerance per ANSI Y14.5M-1982.
4. Gauge plane L3 is parallel to heatslug plane.
5. Dimensions include lead finish.
6. Leads are not allowed above the datum -B-.
7. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" by more than 0.003'' (0.08mm).

Single-In-Line Plastic Packages (SIP)



Z5.067C (ALTERNATE VERSION)
5 LEAD PLASTIC SINGLE-IN-LINE PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.031	0.041	0.79	1.04	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.590	0.610	14.99	15.49	-
E	0.395	0.405	10.04	10.28	-
e	0.067 TYP		1.70 TYP		5
e_1	0.268 BSC		6.80 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.105	0.115	2.66	2.92	-

Rev. 1 4/96

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TS-001AA outline dated 8-89.
2. Solder finish uncontrolled in this area.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.

Sales Office Headquarters

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