HARRIS Semiconductor

HI2304

August 1997

NOT RECOMMENDED FOR NEW DESIGNS
See HI1178

Triple 8-Bit, 20 MSPS, RGB, 3-Channel D/A Converter

Features

- **Resolution . . . . . .Triple 8-Bit**
- **Maximum Conversion Speed 20MHz**
- **RGB 3-Channel Input/Output**
- **Differential Linearity Error . . . . . ±0.5 LSB**
- **Low Power Consumption . . . . . .50mW (330Ω Load for 1.2V_{P-P} Output)**
- **Single Power Supply . . . . . +3.3V**
- **Low Glitch Noise**
- **Direct Replacement for Sony CXD2304**

Applications

- **Digital TV**
- **Graphics Display**
- **High Resolution Color Graphics**
- **Video Reconstruction**
- **Instrumentation**
- **Image Processing**
- **I/Q Modulation**

Description

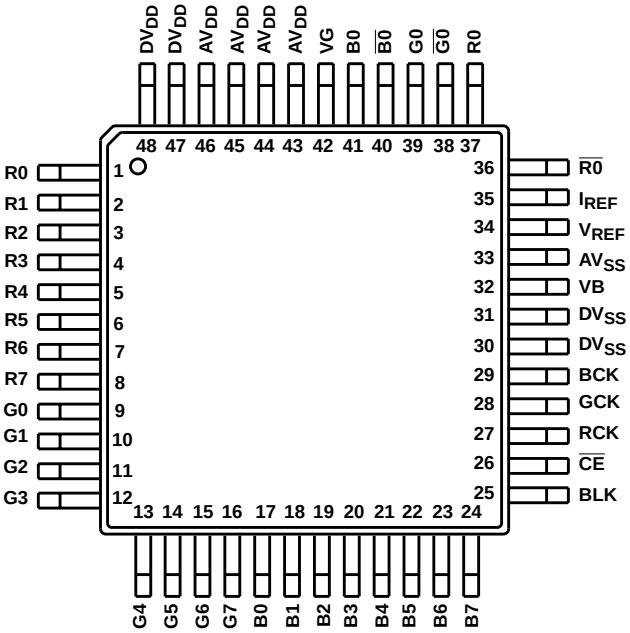
The HI2304 is a triple 8-bit, high-speed, CMOS D/A converter designed for video band use. It has three separate, 8-bit, pixel inputs, one each for red, green, and blue video data. A single 3.3V power supply and pixel clock input can be controlled individually, or connected together as one. The HI2304 also has BLANK video control signal. For faster speed and 5.0V operation, refer to the HI1178.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI2304JCQ	-20 to 75	48 Ld MQFP	Q48.7x7-S

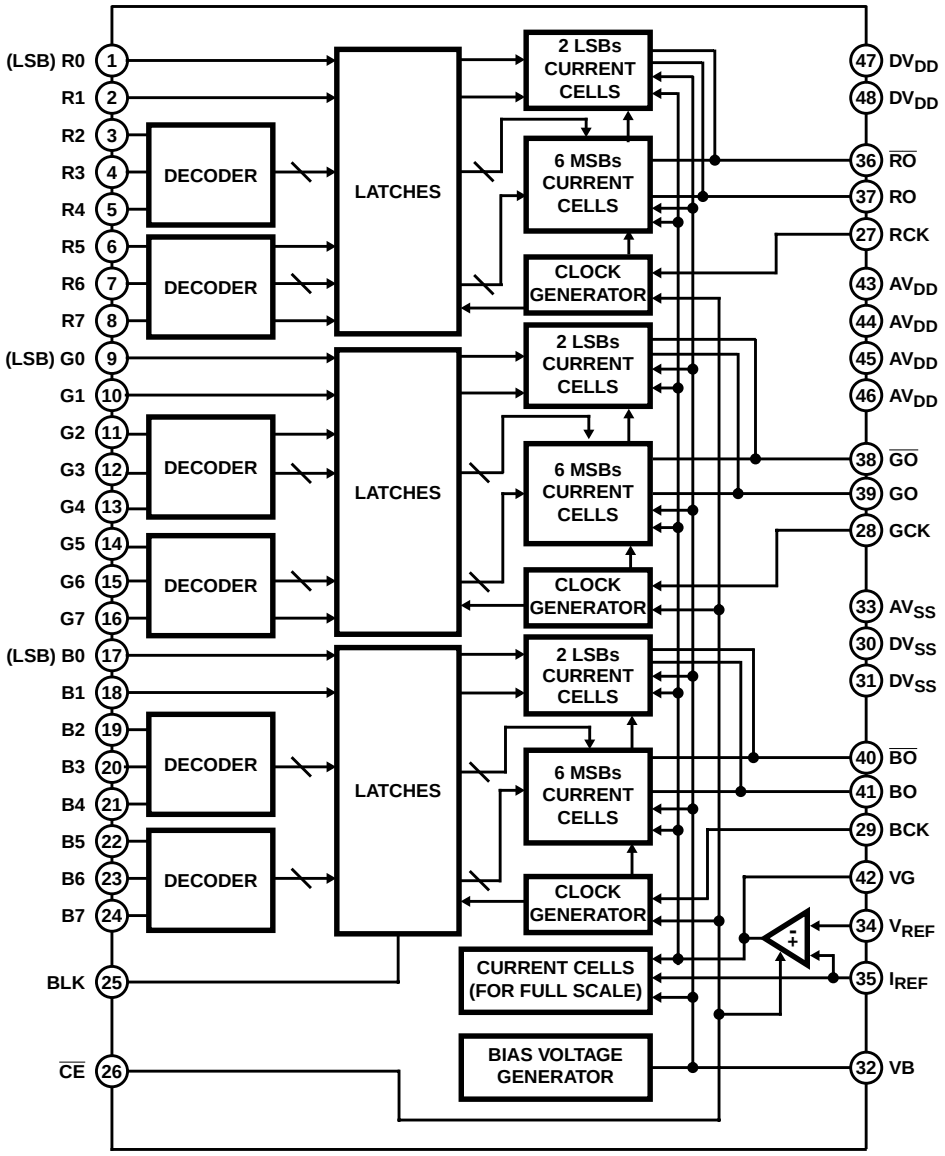
Pinout

HI2304
(MQFP)
TOP VIEW

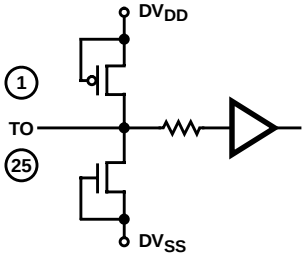


File Number **4116.1**

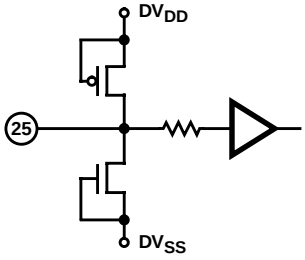
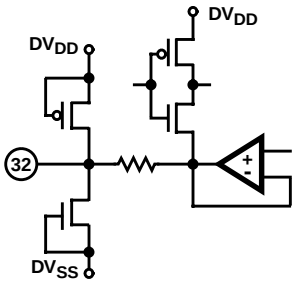
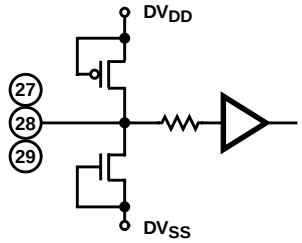
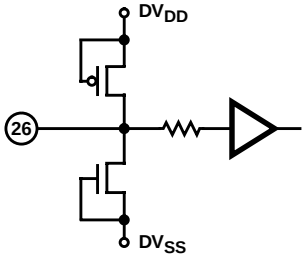
Functional Block Diagram



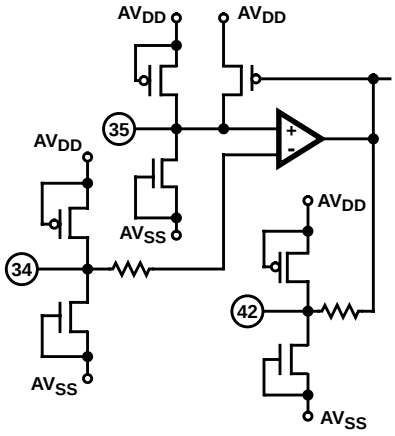
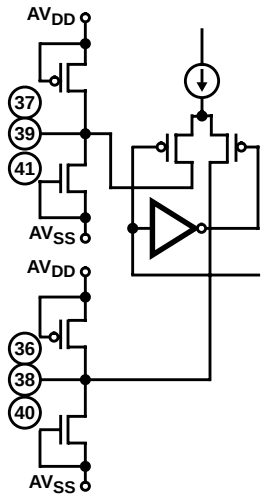
Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 8	R0 to R7		Digital Input.
9 to 16	G0 to G7		
17 to 24	B0 to B7		

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
25	BLK		Blanking pin. No signal at “H” (Output 0V) Output condition at “L”.
32	VB		Connect a capacitor of about 0.1µF.
27	RCK		Clock Pin.
28	GCK		
29	BCK		
30, 31	DV_{SS}		Digital GND.
33	AV_{SS}		Analog GND.
26	$\overline{CE}$		Chip Enable Pin. No signal (Output 0V) at “H” and minimizes power consumption.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
35	I_{REF}		Connect a resistance 16 times “16R” that of output resistance value “R”.
34	V_{REF}		Set full scale output value.
42	VG		Connect a capacitor of about 0.1µF.
43 to 46	AV_{DD}		Analog V_{DD}.
37	RO		Current output pin. Voltage output can be obtained by connecting a resistance.
39	GO		
41	BO		
36	$\overline{RO}$		Inverted current output pin. Normally dropped to analog GND.
38	$\overline{GO}$		
40	$\overline{BO}$		
47, 48	DV_{DD}		Digital V_{DD}.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Input Voltage (V_{IN}) . . . . . V_{DD} to V_{SS}
Output Current (I_{OUT}) . . . . . 0mA to 15mA
(Every Each Channel)

Operating Conditions

Temperature Range (T_{OPR}) . . . . . -20^oC to 75^oC
Supply Voltage
AV_{DD}, AV_{SS} . . . . . 3.0V to 3.6V
DV_{DD}, DV_{SS} . . . . . 3.0V to 3.6V
Reference Input Voltage (V_{REF}) 1.2V
Clock Pulse Width
t_{PW1} . . . . . 25ns (Min)
t_{PW0} . . . . . 25ns (Min)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	104

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature (T_{STG}) . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications f_{CLK} = 20MHz, V_{DD} = 3.3V, R_{OUT} = 330Ω, V_{REF} = 1.2V, R_{IRF} = 5.1kΩ, $T_A = 25^oC$

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		n		-	8	-	Bit
Maximum Conversion Speed		f_{MAX}		20	-	-	MHz
Linearity Error		INL		-2.5	-	2.5	LSB
Differential Linearity Error		DNL		-0.5	-	0.5	LSB
Full Scale Output Voltage		V_{FS}		1.12	1.24	1.36	V
Full Scale Output Ratio (Note 1)		F_{SR}		0	1.5	3	%
Full Scale Output Current		I_{FS}		-	3.8	-	mA
Offset Output Voltage		V_{OS}		-	-	1	mV
Power supply Current		I_{DD}	14.3MHz, at Color Bar Data input	-	15	-	mA
Digital Input Current	H Level	I_{IH}		-	-	5	µA
	L Level	I_{IL}		-5	-	-	µA
Set Up Time		t_S		7	-	-	ns
Hold Time		t_H		3	-	-	ns
Propagation Delay Time		t_{PD}		-	20	-	ns
Glitch Energy		GE		-	150	-	pV/s
Crosstalk		CT	1MHz Sine Wave Output	-	53	-	dB

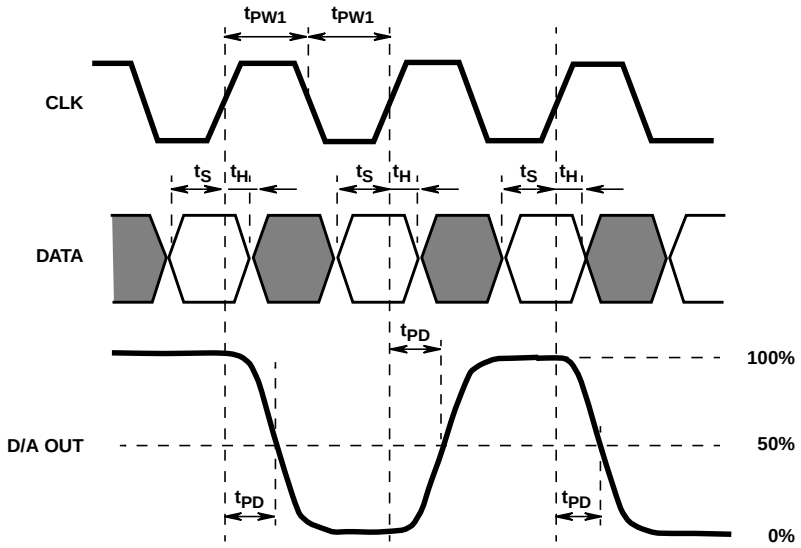
NOTE:

2. Full Scale Output Ratio = $\left| \frac{\text{Full scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}} - 1 \right|$ x 100(%).

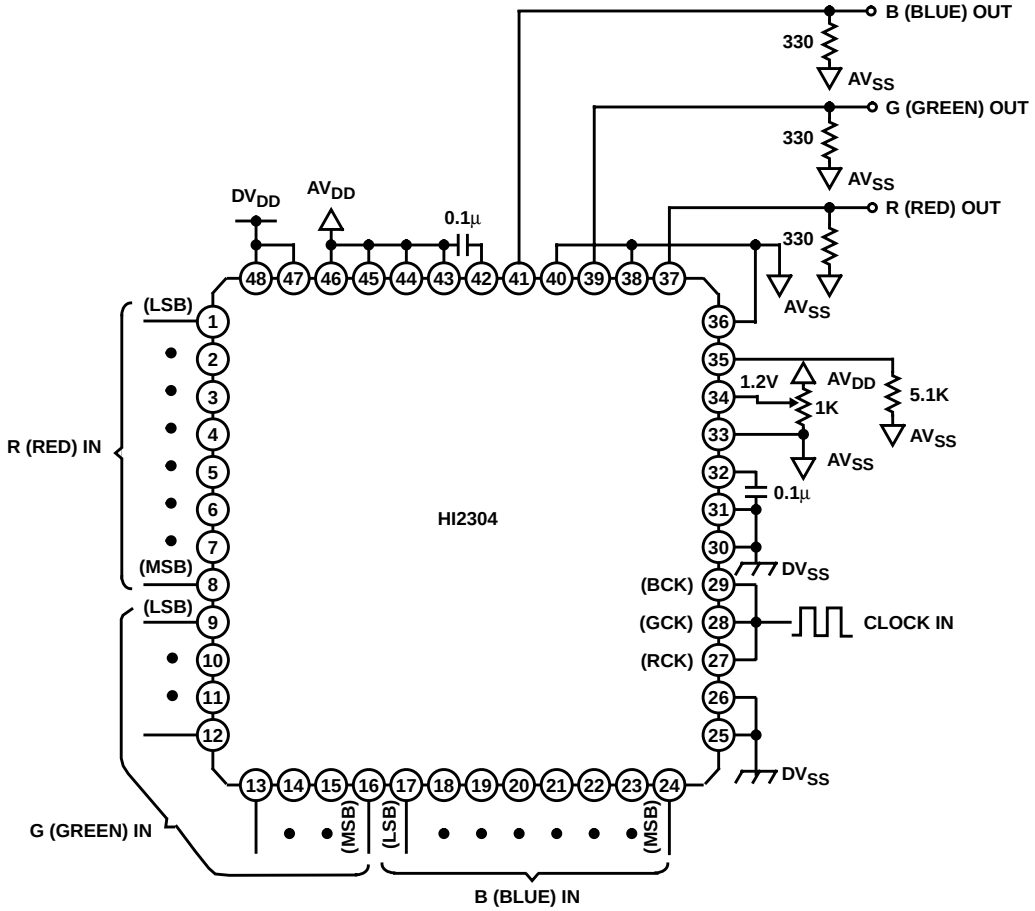
I/O Chart (When Full Scale Output Voltage at 2.00V)

INPUT CODE								OUTPUT VOLTAGE
MSB							LSB	
1	1	1	1	1	1	1	1	1.2V
				•				
				•				
				•				
1	0	0	0	0	0	0	0	0.6V
				•				
				•				
				•				
0	0	0	0	0	0	0	0	0V

Timing Diagram



Typical Application Circuit



Notes On Operation

- How to Select the Output Resistance

  The HI2304 is a current output D/A converter. To obtain the output voltage, connect the resistance to IO pin (RO, GO, BO). For specifications we have:

  Output Full Scale Voltage V_{FS} = 1.2 [V].

  Output Full Scale Current I_{FS} = 3.8 [mA].

  Calculate the output resistance value from the relation of $V_{FS} = I_{FS} \times R$. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here, please note that V_{FS} becomes $V_{FS} = V_{REF} \times 16R/R$. R is the resistance connected to IO while R is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand, glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase Relation Between Data and Clock

  To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock, applied from the exterior. Be sure to satisfy the provisions of the set up time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.

- V_{DD}, V_{SS}

To reduce noise effects, separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about 0.1µF, as close as possible to the pin.

Test Circuits

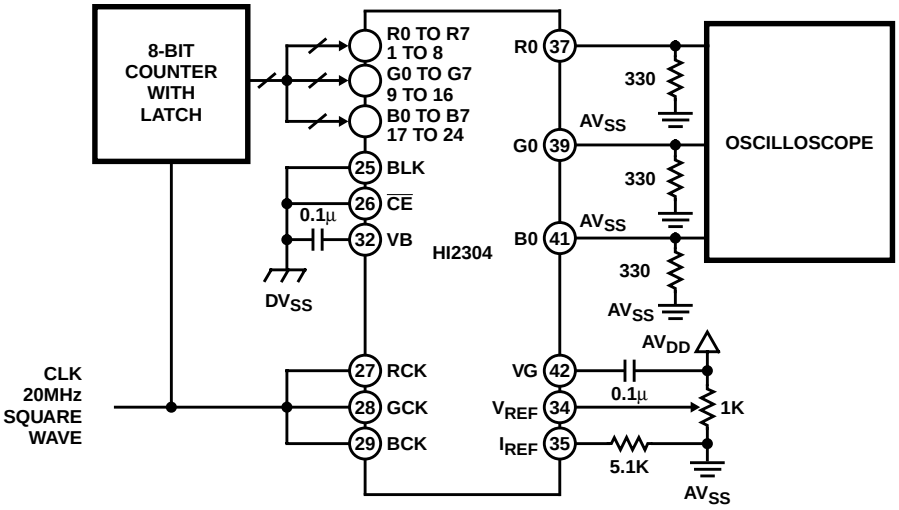


FIGURE 1. MAXIMUM CONVERSION RATE TEST CIRCUIT

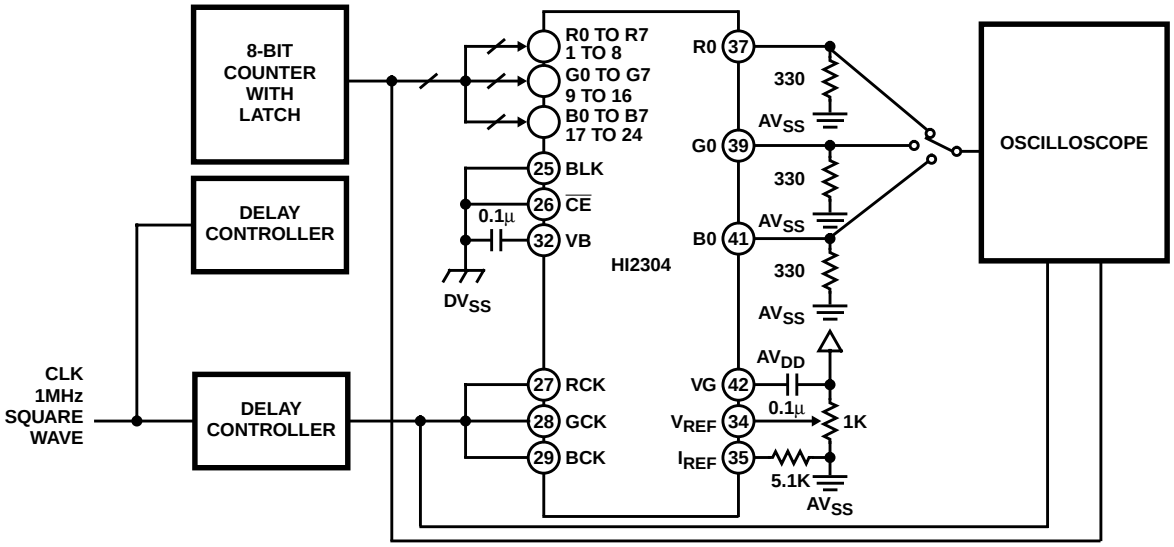


FIGURE 2. SET-UP HOLD TIME GLITCH ENERGY TEST CIRCUIT

Test Circuits (Continued)

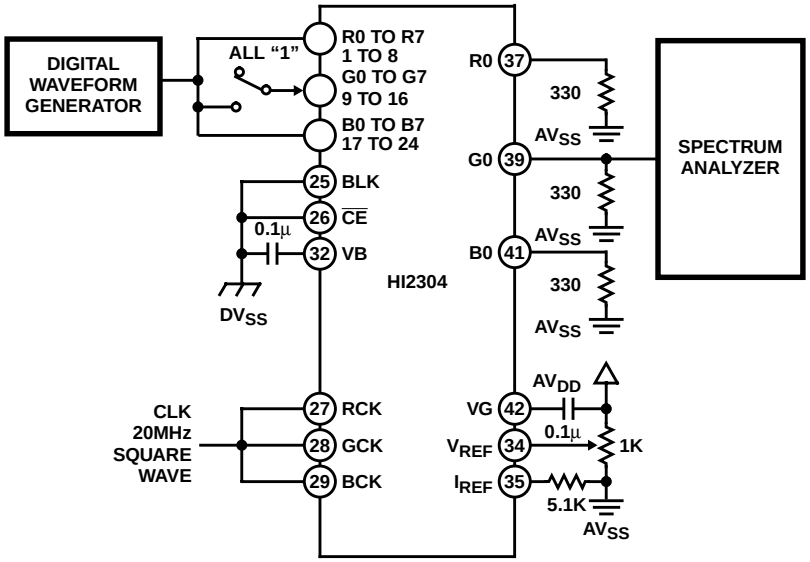


FIGURE 3. CROSSTALK TEST CIRCUIT (See Figure 7)

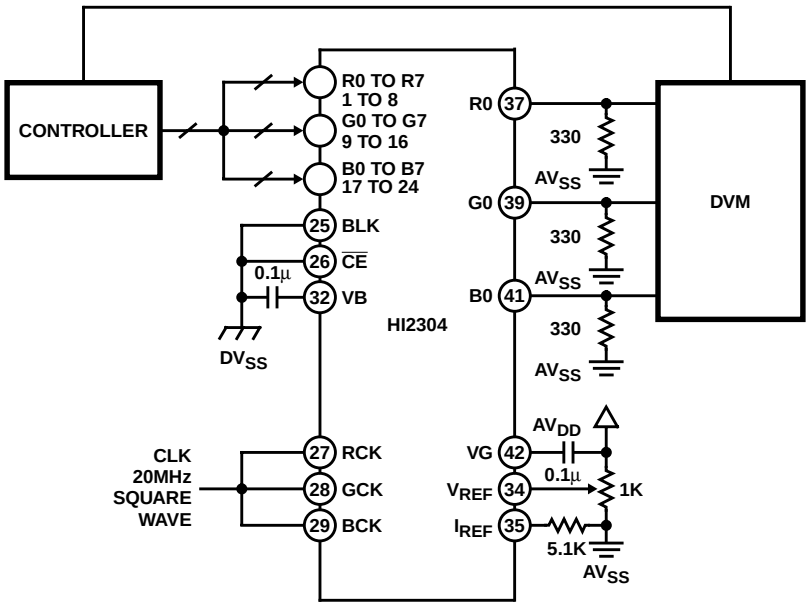


FIGURE 4. DC CHARACTERISTICS TEST CIRCUIT

Test Circuits (Continued)

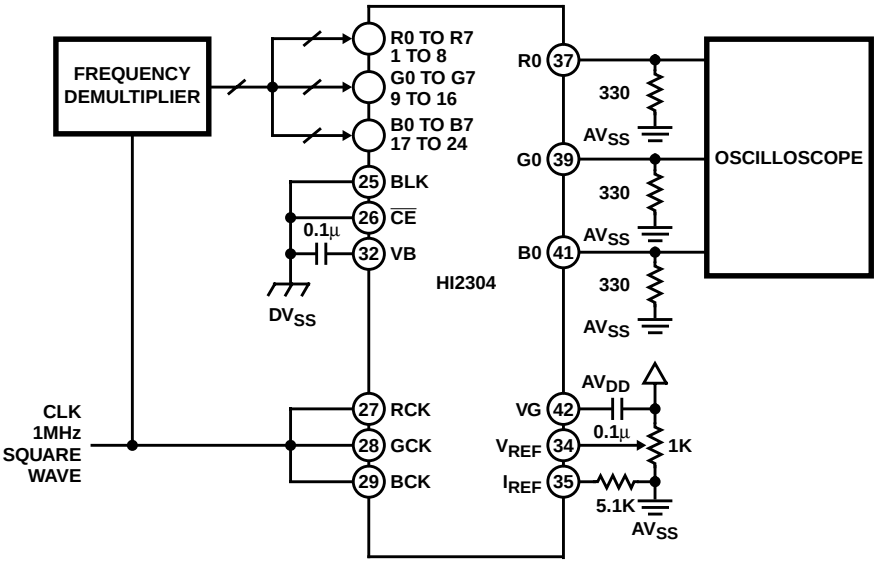
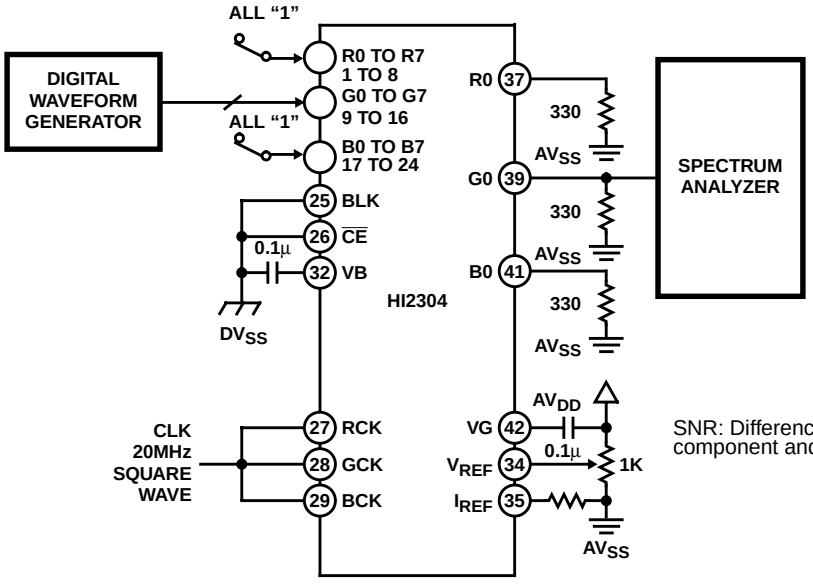


FIGURE 5. PROPAGATION DELAY TIME TEST CIRCUIT



SNR: Difference between primary component and secondary distortion.

FIGURE 6. SNR TEST CIRCUIT (See Figure 8)

Typical Performance Curves

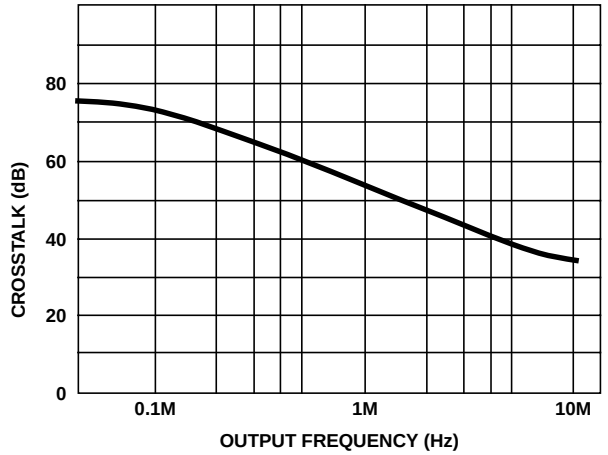


FIGURE 7. CROSSTALK

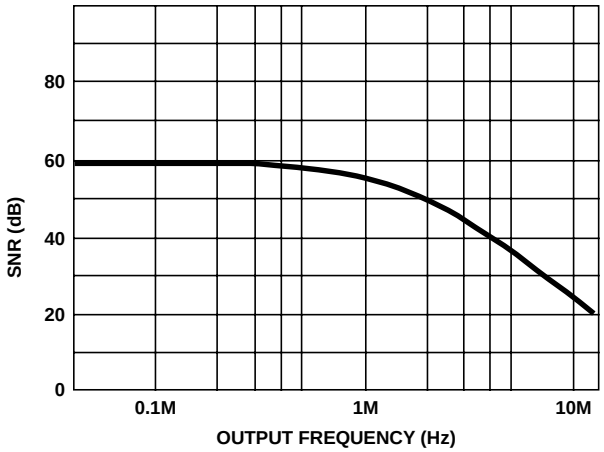


FIGURE 8. SNR (DIFFERENCE BETWEEN PRIMARY COMPONENT AND SECONDARY DISTORTION)

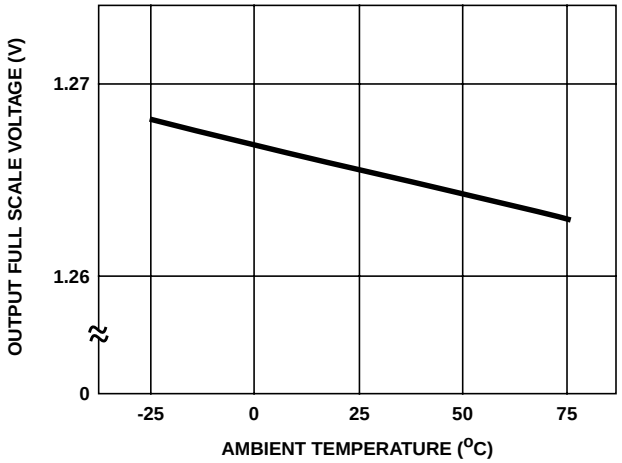


FIGURE 9. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

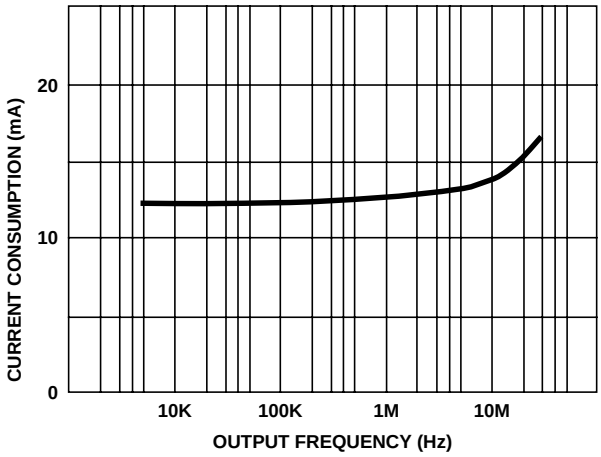


FIGURE 10. OUTPUT FREQUENCY vs CURRENT CONSUMPTION

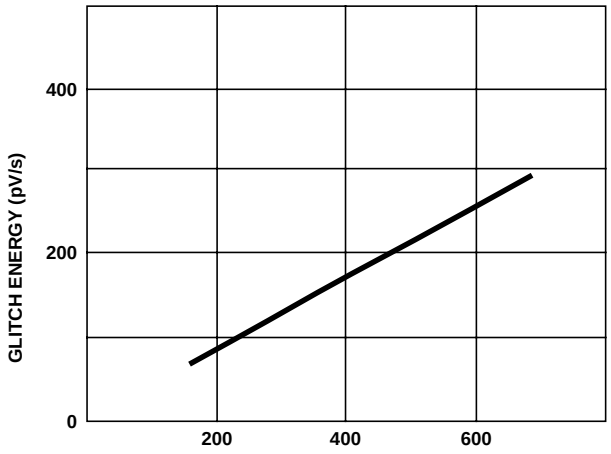


FIGURE 11. OUTPUT RESISTANCE vs GLITCH ENERGY

Reference Measurement Condition and Description

AV_{DD} = 3.3V.

DV_{DD} = 3.3V.

V_{REF} = 1.2V.

R_{IRF} = 5.1kΩ.

T_A = 25^{o}C.

Figure 7 and Figure 8 refer to the measurement circuit.

Figure 9 is input data = all 1.

Figure 10 is input data = output of incremental counter, current consumption is total of 3ch.