Data Sheet | September 2000 | File Number 4102.2

6-Bit, 20MSPS, Video A/D Converter (CMOS)

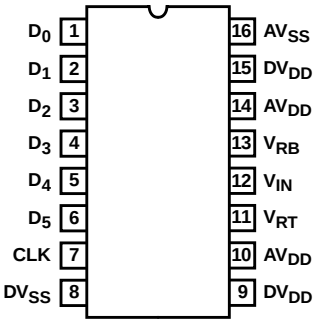
HI1172 is a 6-bit, CMOS A/D converter for video use. The adoption of a 2-step parallel conversion achieves speeds of 20MSPS minimum, 35MSPS typical.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HI1172JCB	-20 to 75	16 Ld SOIC	M16.2-S

Pinout

HI1172 (SOIC)
TOP VIEW



Features

- Resolution 6-Bit
- Maximum Sampling Frequency 20MSPS
- Low Power Consumption at 20MSPS (Typ) (Reference Current Excluded) 40mW
- Built-In Sample and Hold Circuit
- Three-State TTL Compatible Output
- Power Supply . . . . . 5V Single
- Low Input Capacitance. 4pF
- Reference Impedance . . . . . 250Ω (Typ)

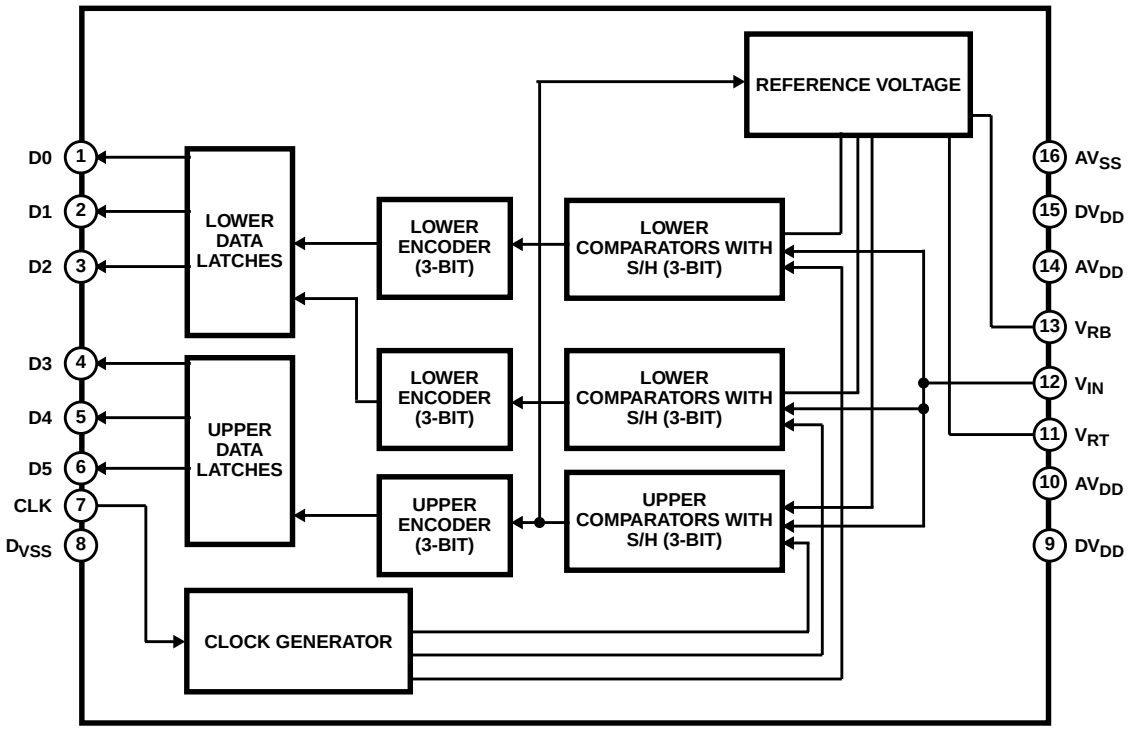
Applications

- Video Digitizing
- Wireless Communications

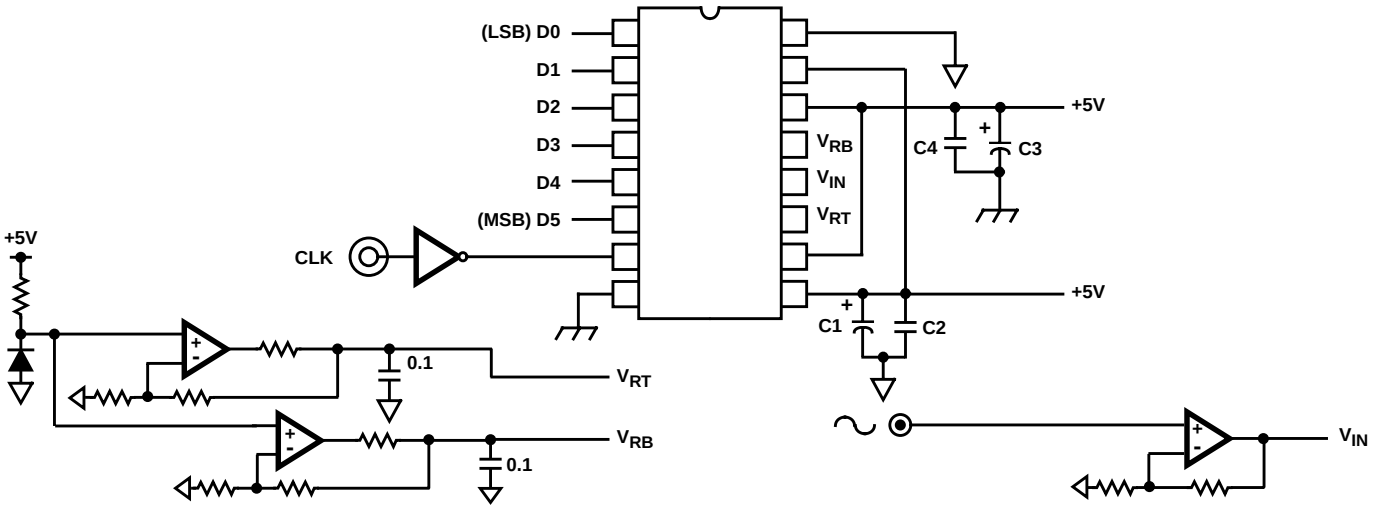
Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

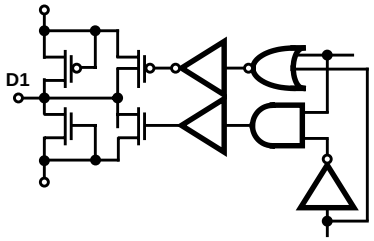
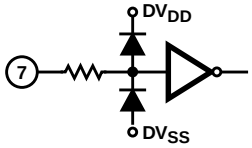
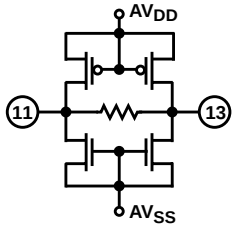
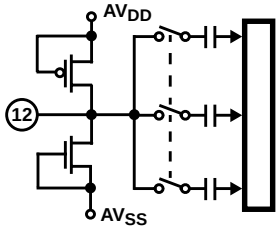
Functional Block Diagram



Typical Application Circuit



Pin Descriptions

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 6	D0 to D5		D0 (LSB) to D5 (MSB) Output.
7	CLK		Clock Input.
8	DV_{SS}		Digital GND.
9, 15	DV_{DD}		Digital +5V.
10, 14	AV_{DD}		Analog +5V.
11	V_{RT}		Reference Voltage (Top).
13	V_{RB}		Reference Voltage (Bottom).
12	V_{IN}		Analog Input.
16	AV_{SS}		Analog GND.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Reference Voltage (V_{RT}, V_{RB}) . . . . . V_{DD} to V_{SS}
Analog Input Voltage (V_{IN}) . . . . . V_{DD} to V_{SS}
Digital Input Voltage (CLK) . . . . . V_{DD} to V_{SS}
Digital Output Voltage (V_{OH}, V_{OL}) . . . . . V_{DD} to V_{SS}

Operating Conditions

Supply Voltage Range, AV_{DD}, AV_{SS} . . . . . 4.75V to 5.25V
Reference Voltage, DV_{DD}, DV_{SS}
- V_{RT} . . . . . 0.9V to 5V
- V_{RB} . . . . . 0V to 4.1V
- V_{RT} - V_{RB} . . . . . 0.9V to AV_{DD}

Analog Input Voltage (V_{IN}) . . . . . V_{RB} to V_{RT}
Clock Pulse Width
- t_{PW1} . . . . . 25ns (Min)
- t_{PW0} . . . . . 25ns (Min)

Temperature Range . . . . . -20^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	120

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{DD} = +5V$, $V_{RB} = 1V$, $V_{RT} = 2V$, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Speed, f_C	f_C	V_{IN} = 1V to 2V f_{IN} = 1kHz Ramp		0.5	-	20	MSPS
Integral Non-Linearity	E_L	f_C = 20MSPS V_{IN} = 1V to 2V		-	±0.3	±0.5	LSB
Differential Non-Linearity	E_D	f_C = 20MSPS V_{IN} = 1V to 2V		-	±0.3	±0.5	LSB
Supply Current	I_{DD}	f_C = 20MSPS NTSC Ramp Wave Input		-	7	12	mA
Reference Pin Current	I_{REF}			3	4	5.7	mA
Analog Input (-1dB)	BW			-	18	-	MHz
Analog Input Capacitance	C_{IN}	$V_{IN} = 1.5V + 0.07V_{RMS}$		-	4	-	pF
Reference Resistance (V_{RT} to V_{RB})	R_{REF}			175	250	325	Ω
Offset Voltage	E_{OT}			0	-20	-40	mV
	E_{OB}			15	35	55	mV
Digital Input Voltage	V_{IH}			4.0	-	-	V
	V_{IL}			-	-	1.0	V
Digital Input Current	I_{IH}	V_{DD} = Max	$V_{IH} = V_{DD}$	-	-	5	µA
	I_{IL}		V_{IL} = 0V	-	-	5	µA
Digital Output Current	I_{OH}	V_{DD} = Min	$V_{OH} = V_{DD} - 0.5V$	-1.1	-	-	mA
	I_{OL}		V_{OL} = 0.4V	3.7	-	-	mA
Output Data Delay	T_{DL}	With TTL 1 Gate and 10pF Load		-	18	30	ns
Differential Gain Error	DG	NTSC 40 IRE Mod		-	1.0	-	%
Differential Phase Error	DP	Ramp, f_C = 14.3MSPS		-	1.0	-	deg
Aperture Jitter	t_{AJ}			-	40	-	ps
Sampling Delay	t_{SD}			-	4	-	ns

Test Circuits

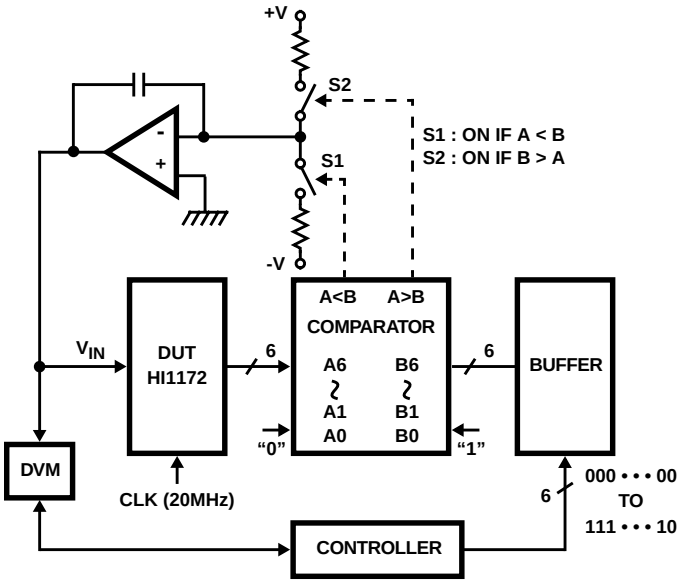


FIGURE 1. INTEGRAL NON-LINEARITY ERROR, DIFFERENTIAL NON-LINEARITY, OFFSET VOLTAGE

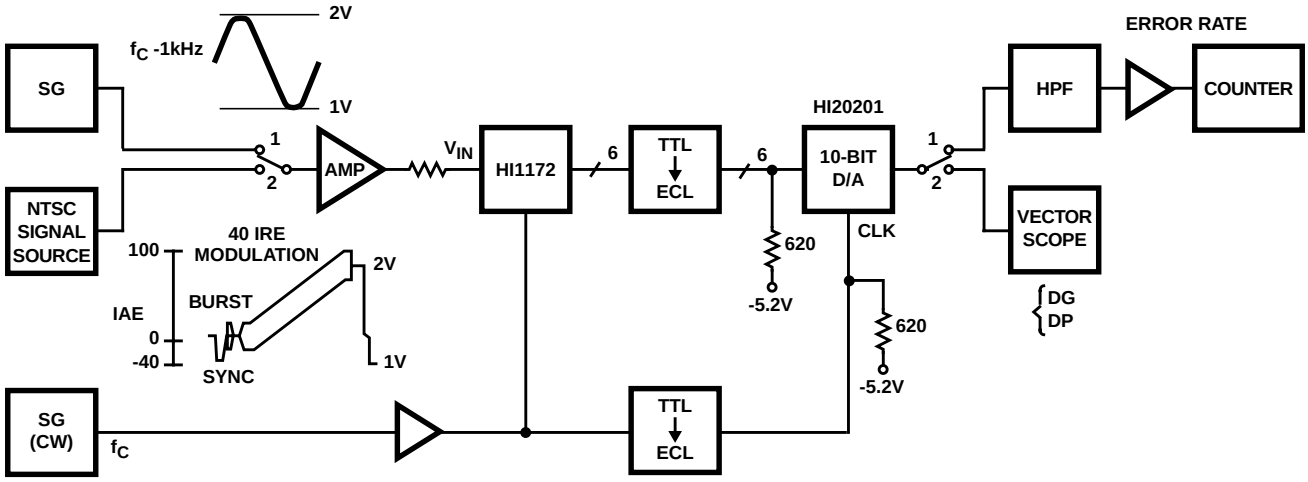


FIGURE 2. MAXIMUM OPERATIONAL SPEED, DIFFERENTIAL GAIN ERROR, DIFFERENTIAL PHASE ERROR

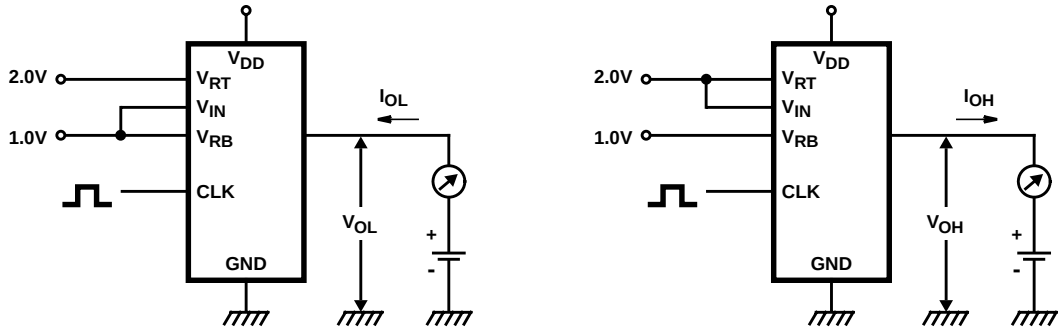


FIGURE 3. DIGITAL OUTPUT CURRENT TEST CIRCUIT

Timing Diagrams

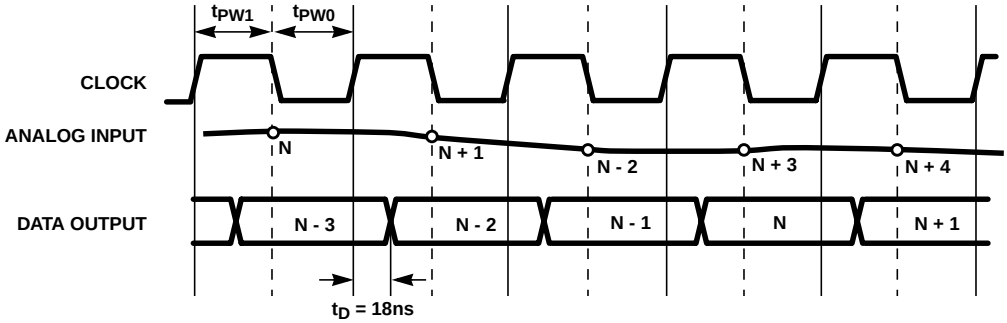


FIGURE 4. TIMING CHART 1

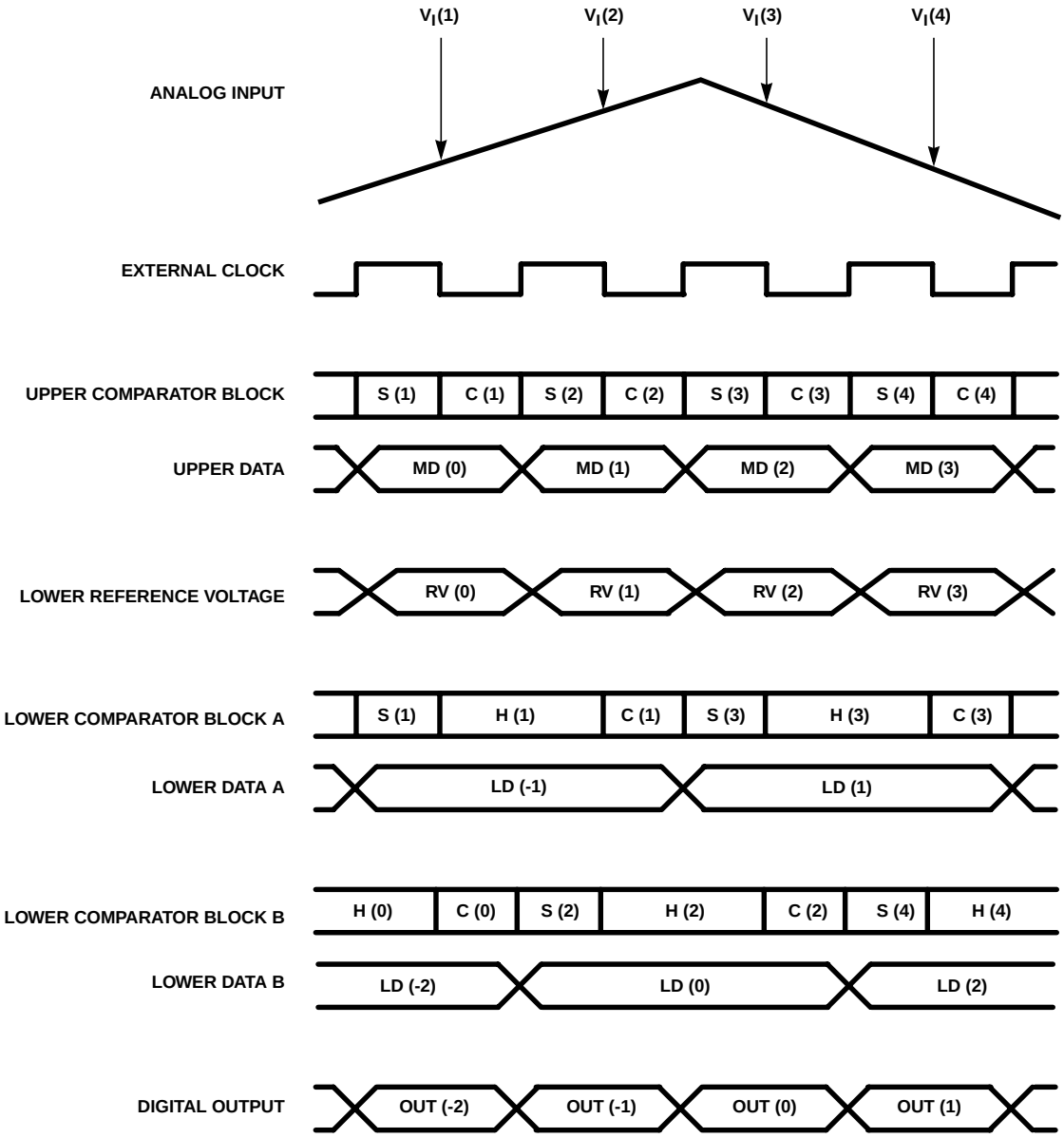


FIGURE 5. TIMING CHART 2

Digital Output

Compatibility between analog input voltage and the digital output code is indicated in the chart below.

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE					
		MSB					LSB
V_{RT}	0	1	1	1	1	1	1
•	•			•			
•	•			•			
•	•			•			
•	31	1	0	0	0	0	1
•	32	0	1	1	1	1	1
•	•			•			
•	•			•			
•	•			•			
V_{RB}	63	0	0	0	0	0	0

Operation (See Block Diagram and Waveform)

The HI1172 is a 2-step parallel system A/D converter featuring a 3-bit upper comparators group and 2 lower comparators groups of 3-bit each. The reference voltage that is equal to the voltage between V_{RT}-V_{RB}/8 is constantly applied to the upper 3-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.

This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols, i.e., input sampling (auto zero) mode, input hold mode and comparison mode.

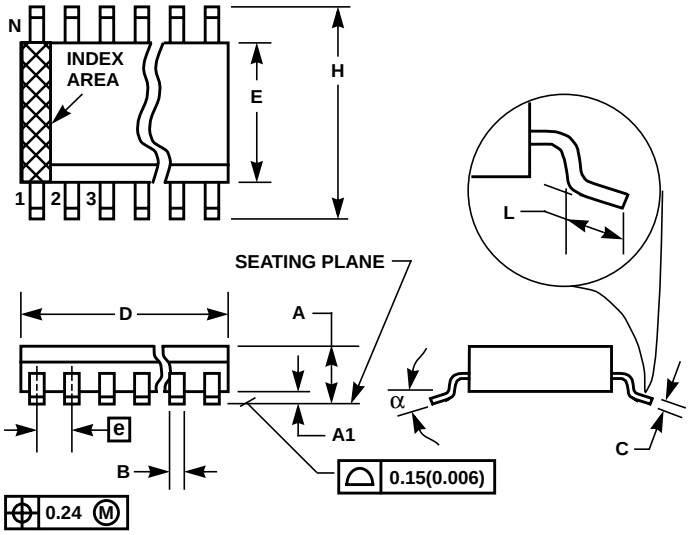
The operation of respective parts is as indicated in the chart. Input voltage Vi (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.

The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Notes On Operation

- V_{DD}, V_{SS} - To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1µF set as close as possible to the pin to bypass to the respective GNDs.
- Analog Input - Compared with a flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to drive with an amplifier featuring sufficient bandwidth and drive capability. When driving with an amplifier of low output impedance, parasitic oscillation may occur. That may be prevented by inserting a resistance of about 100Ω in series between the amplifier output and A/D input.
- Clock Input - The clock line wiring should be as short as possible. Also, to avoid any interference with other signals, separate it from the other circuits.
- Reference Input - Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. By bypassing V_{RT} and V_{RB} pins to GND with a capacitor of about 0.1µF, stable characteristics are obtained.
- Timing - Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.
- About Latch Up - It is necessary that AV_{DD} and DV_{DD} pins to be the common source of power supply. This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON.

Small Outline Plastic Packages (SOIC)



M16.2-S

16 LEAD SMALL OUTLINE PLASTIC PACKAGE (200 MIL)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.067	0.078	1.70	2.00	-
A1	0.002	0.011	0.05	0.30	-
B	0.014	0.021	0.35	0.55	-
C	0.006	0.011	0.15	0.30	-
D	0.386	0.405	9.80	10.30	1
E	0.205	0.220	5.20	5.60	2
e	0.050 BSC		1.27 BSC		-
H	0.296	0.326	7.50	8.3	-
L	0.012	0.027	0.30	0.70	3
N	16		16		4
α	0^o	10^o	0^o	10^o	-

Rev. 0 2/96

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs.
2. Dimension “E” does not include interlead flash or protrusions.
3. “L” is the length of terminal for soldering to a substrate.
4. “N” is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil Ltd.
8F-2, 96, Sec. 1, Chien-kuo North,
Taipei, Taiwan 104
Republic of China
TEL: 886-2-2515-8508
FAX: 886-2-2515-8369