HA5352

Fast Acquisition Dual Sample and Hold Amplifier

May 1997

NOT RECOMMENDED FOR NEW DESIGNS
See HA5351
contact our Technical Support Center at
i-888-INTERSIL or www.intersil.com/tsc

Features

- **Fast Acquisition to 0.01% . . . . . .70ns (Max)**
- **Low Offset Error . . . . . ±2mV (Max)**
- **Low Pedestal Error . . . . . ±10mV (Max)**
- **Low Droop Rate . . . . . 2μV/μs (Max)**
- **Wide Unity Gain Bandwidth 40MHz**
- **Low Power Dissipation per Amp . . . . . .220mW (Max)**
- **Total Harmonic Distortion (Hold Mode) . . . . . -72dBc (V_{IN} = 5V_{P-P} at 1MHz)**
- **Fully Differential Inputs**
- **On Chip Hold Capacitor**

Applications

- **Synchronous Sampling**
- **Wide Bandwidth A/D Conversion**
- **Deglitching**
- **Peak Detection**
- **High Speed DC Restore**

Description

The HA5352 is a fast acquisition, wide bandwidth Dual Sample and Hold amplifier built with the Intersil HBC-10 BiCMOS process. This Sample and Hold amplifier offers the combination of features; fast acquisition time (70ns to 0.01%), excellent DC precision and extremely low power dissipation, making it ideal for use in multi-channel systems that require low power.

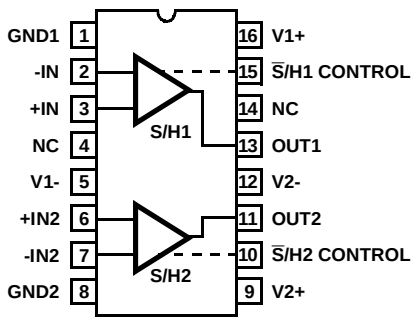
The HA5352 comes in an open loop configuration with fully differential inputs providing flexibility for user defined feedback. In unity gain the HA5352 is completely self-contained and requires no external components. The on-chip 15pF hold capacitors are completely isolated to minimize droop rate and reduce the sensitivity of pedestal error. The HA5352 Dual Sample and Hold is available in a 14 lead PDIP and 16 lead SOIC packages saving board space while its pinout is designed to simplify layout.

Ordering Information

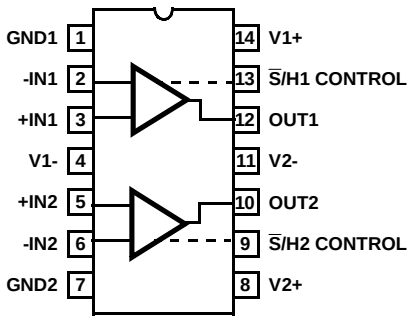
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5352IP	-40°C to +85°C	14 Lead Plastic DIP
HA5352IB	-40°C to +85°C	16 Lead Plastic SOIC (W)

Pinouts

HA5352 (300 mil SOIC)
TOP VIEW



HA5352 (PDIP)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals . . . . . +11V
Differential Input Voltage . . . . . +6V
Voltage between S/H control and ground. . . . . +5.5V
Output Current, Continuous . . . . . ±37mA
Junction Temperature (Plastic Packages) . . . . . +150^{o}C
Lead Temperature (Soldering, 10s) . . . . . +300^{o}C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA5352I. . . . . -40^{o}C ≤ T_A ≤ +85^{o}C
Storage Temperature Range . . . . . -65^{o}C ≤ T_A ≤ +150^{o}C
Thermal Package Characteristics θ_{JA}
Plastic DIP. . . . . 90^{o}C/W
SOIC . . . . . 95^{o}C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified

PARAMETERS	TEMP	HA5352I			UNITS
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Input Voltage Range	Full	-2.5	-	+2.5	V
Input Resistance (Note 2)	+25^{o}C	100	500	-	kΩ
Input Capacitance	+25^{o}C	-	-	5	pF
Input Offset Voltage	+25^{o}C	-2	-	2	mV
	Full	-3.0	-	3.0	mV
Offset Voltage Temperature Coefficient	Full	-	15	-	µV/^{o}C
Bias Current	Full	-	2.5	5	µA
Offset Current	Full	-1.5	-	+1.5	µA
Common Mode Range	Full	-2.5	-	+2.5	V
Common Mode Rejection (±2.5V_{DC}, Note 3)	Full	60	80	-	dB
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (±2.5V_{OUT})	+25^{o}C	95	108	-	dB
	Full	85	-	-	dB
Unity Gain -3dB Bandwidth	+25^{o}C	-	40	-	MHz
TRANSIENT RESPONSE					
Rise Time (200mV Step)	+25^{o}C	-	8.5	-	ns
Overshoot (200mV Step)	+25^{o}C	0	-	30	%
Slew Rate (5V Step)	Full	88	105	-	V/µs
DIGITAL INPUT CHARACTERISTICS					
Input Voltage (High) V_{IH}	+25^{o}C, +85^{o}C	2.1	-	5.0	V
	-40^{o}C	2.4	-	5.0	V
Input Voltage (Low) V_{IL}	Full	0	-	0.8	V

Electrical Specifications Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified **(Continued)**

PARAMETERS		TEMP	HA5352I			UNITS
			MIN	TYP	MAX	
Input Current (V_{IL} = 0V)	I_{IL}	Full	-1	-	+1	µA
Input Current (V_{IH} = 5V)	I_{IH}	Full	-1	-	+1	µA
OUTPUT CHARACTERISTICS						
Output Voltage (R_L = 510Ω)		Full	-3	-	+3	V
Output Current (R_L = 100Ω)		+25°C, +85°C	20	25	-	mA
		-40°C	15	-	-	mA
Full Power Bandwidth ($5V_{P-P}$, A_V = +1, -3dB)		Full	-	13	-	MHz
Output Resistance - Hold Mode		+25°C	-	0.02	-	Ω
TOTAL OUTPUT NOISE, D.C. TO 10MHz						
Sample Mode		+25°C	-	325	-	µVrms
Hold Mode		+25°C	-	325	-	µVrms
SAMPLE MODE DISTORTION CHARACTERISTICS						
Total Harmonic Distortion	V_{IN} = $4.5V_{P-P}$, F_{IN} = 100kHz	+25°C	-	-80	-76	dBc
	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz	+25°C	-	-74	-69	dBc
	V_{IN} = $1V_{P-P}$, F_{IN} = 10MHz	+25°C	-	-57	-52	dBc
Signal to Noise Ratio (RMS Signal to RMS Noise)	V_{IN} = $4.5V_{P-P}$, F_{IN} = 100kHz	+25°C	-	73	-	dB
Crosstalk	V_{IN} = $5V_{P-P}$, F_{IN} = 10MHz	+25°C	-	75	-	dB
HOLD MODE DISTORTION CHARACTERISTICS (50% Duty Cycle S/H)						
Total Harmonic Distortion	V_{IN} = $4.5V_{P-P}$, F_{IN} = 100kHz, $F_S \cong$ 100kHz	+25°C	-	-78	-74	dBc
	V_{IN} = $5V_{P-P}$, F_{IN} = 1MHz, $F_S \cong$ 1MHz	+25°C	-	-72	-67	dBc
	V_{IN} = $1V_{P-P}$, F_{IN} = 10MHz, $F_S \cong$ 1MHz	+25°C	-	-51	-47	dBc
Signal to Noise Ratio (RMS Signal to RMS Noise)	V_{IN} = $4.5V_{P-P}$, F_{IN} =100kHz, $F_S \cong$ 100kHz	+25°C	-	70	-	dB
SAMPLE AND HOLD CHARACTERISTICS						
Acquisition Time	0V to 2.0V Step to ±1mV	+25°C	-	53	-	ns
	0V to 2.0V Step to 0.01% (±200µV)	+25°C	-	64	70	ns
	-2.5V to +2.5V Step to 0.01% (±500µV)	+25°C	-	90	100	ns

Electrical Specifications Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMP	HA5352I			UNITS
		MIN	TYP	MAX	
Droop Rate	+25°C	-	0.3	-	µV/µs
	Full	-2	-	2	µV/µs
Hold Step Error (V_{IL} = 0V, V_{IH} = 4.0V, t_R = 5ns)	Full	-10	-	+10	mV
Hold Mode Settling Time (to ±1mV)	25°C	-	50	-	ns
Hold Mode Feedthrough ($5V_{P-P}$, 500kHz, Sine)	25°C	-	72	-	dB
EADT (Effective Aperture Delay Time)	+25°C	-	+1	-	ns
Aperture Time (Note 2)	+25°C	-	10	-	ns
Aperture Uncertainty	+25°C	-	10	20	ps
Aperture Match	+25°C	-	30	-	ps
POWER SUPPLY CHARACTERISTICS					
Supply Current (per Amp)	Full	-	20	22	mA
Total Supply Current	Full	-	40	44	mA
PSRR (+V or -V, 10% Delta)	Full	60	74	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derived from Computer Simulation only, not tested.
3. +CMRR is measured from 0V to +2.5V, -CMRR is measured from 0V to -2.5V.

Die Characteristics

DIE DIMENSIONS:
2530 x 3110 x 525 ±25.4µm
100 x 122 x 19 ±1mil

METALLIZATION:
Type: Metal 1: AlSiCu/TiW
Thickness: Metal 1: 6kÅ ± 750Å

Type: Metal 2: AlSiCu
Thickness: Metal 2: 16kÅ ± 1.1kÅ

GLASSIVATION:
Type: Sandwich Passivation
Nitride - 4kÅ, Undoped Si Glass(USG) - 8kÅ, Total - 12kÅ ±2kÅ

SUBSTRATE POTENTIAL: V-

TRANSISTOR COUNT: 312

Metallization Mask Layout

HA5352