HA13558AFH

CD-ROM Combo Driver

HITACHI

ADE-207-235C (Z)
4th Edition
November 1, 1997

Description

The HA13558AFH is combination of Spindle, Forcus, Tracking, Slider, Tray designed for CD-ROM and have following function and features.

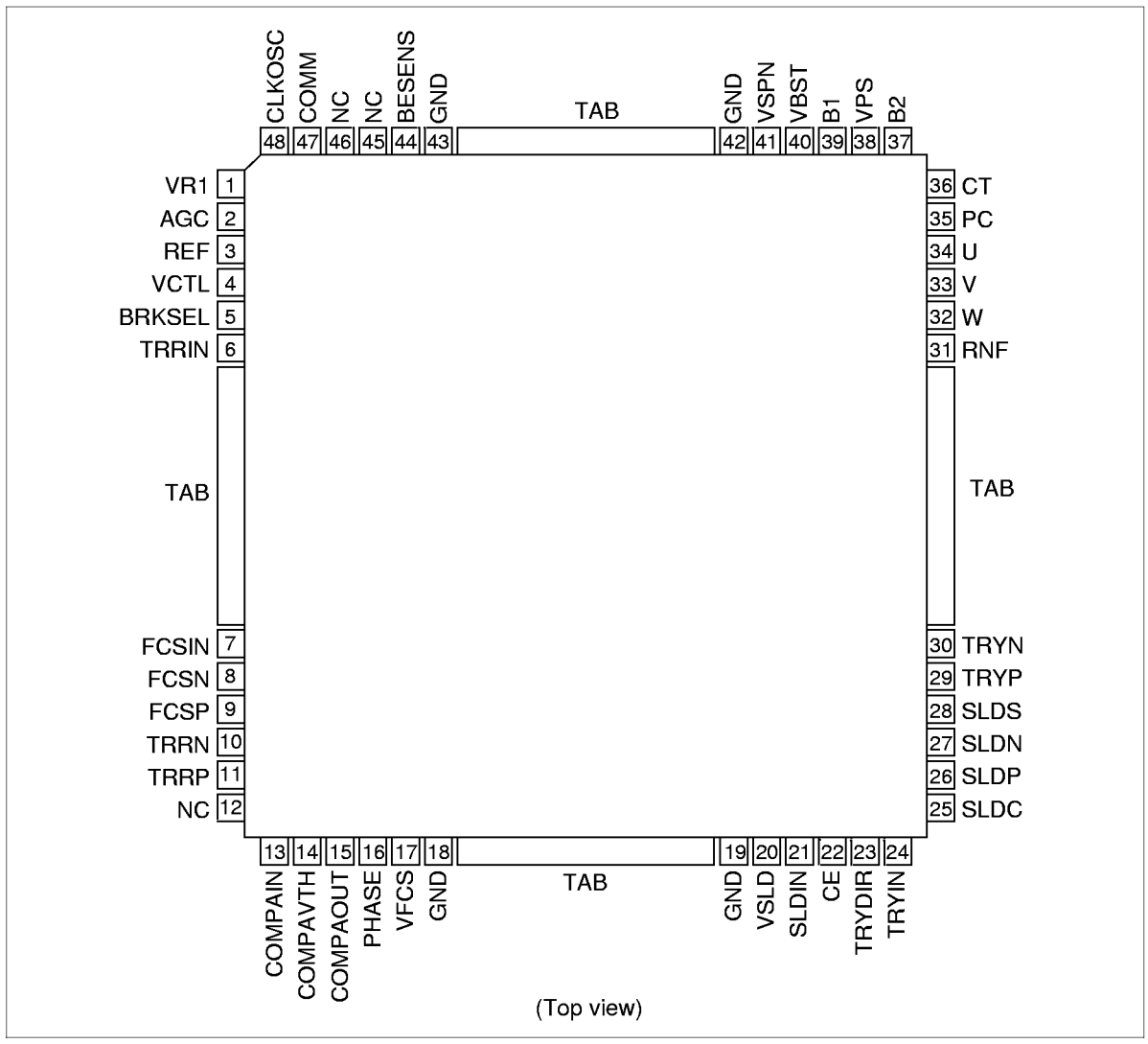
Functions

- 1.5 A sensorless spindle driver
- 0.5 A BTL forcus driver
- 0.5 A BTL tracking driver
- 1.5 A H bridge slider motor driver
- 1.0 A H bridge tray motor driver
- Amplitude detector circuit
- Over temperature shut down (OTSD)

Features

- Sensorless spindle driver
- Soft switching Drive
- Low output saturation voltage (spindle)

Pin Arrangement



(Top view)

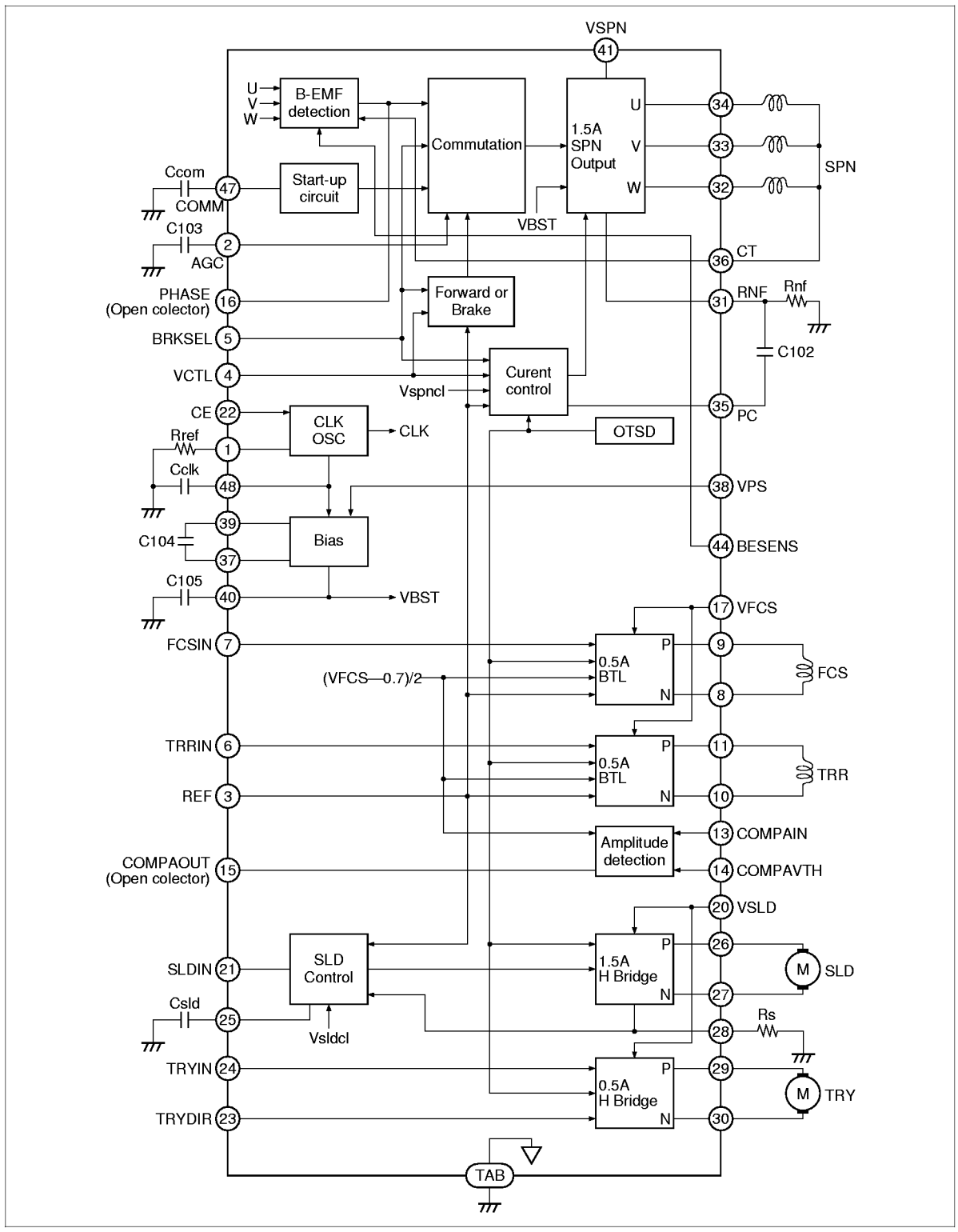
Pin Description

Pin No.	Pin Name	Function
1	VR1	Reference voltage. The IC's internal reference current is determined by this voltage and the external resistor Rref.
2	AGC	AGC for the soft switching function. Holds the level used for IC internal processing fixed even if the B-EMF level fluctuates due to the rotation speed.
3	REF	Reference voltage for the spindle control input, the FCS driver control input, the TRR driver control input, and the SLD driver control input.
4	VCTL	Spindle control input. Generates forward torque when a voltage higher than REF is applied, and brake when a voltage lower than REF is applied.
5	BRKSEL	To select the brake (L: Short brake, H: Reverse brake)
6	TRRIN	TRR driver control input. Takes the REF pin voltage as the reference.
7	FCSIN	FCS driver control input. Takes the REF pin voltage as the reference.
8, 9	FCSN & P	FCS driver output
10, 11	TRRN & P	TRR driver output
12	NC	No connection
13	COMPAIN	Amplitude detection comparator input. Connect either the FCS or TRR driver output to this pin.
14	COMPAVTH	Amplitude detection comparator threshold setting input. (Vin = 0.3 to 1.8 V)
15	COMPAOUT	Amplitude detection comparator output
16	PHASE	Outputs the B-EMF zero cross phase.
17	VFCS	Power supply for the FCS driver, TRR driver, and control block
20	VSLD	Power supply for the slide motor driver and tray motor driver
21	SLDIN	Slide control input. Takes the REF pin voltage as the reference.
22	CE	Chip enable
23	TRYDIR	Tray motor direction control
24	TRYIN	Tray motor drive PWM control input
25	SLDC	Slide off timer time constant. The PWM off time is determined by the external capacitor and resistor Csld and Rref.
26, 27	SLDP & N	Slide motor driver output
28	SLDS	Slide driver current detection
29, 30	TRYP & N	Tray motor driver output
31	RNF	Spindle driver current detection
32, 33, 34	W, V, U	Spindle driver output
35	PC	Spindle driver output
36	CT	Spindle center tap
37, 39	BC2 & 1	Booster pumping capacitor connection

Pin Description (cont)

Pin No.	Pin Name	Function
38	VPS	DC-DC converter control block power supply
40	VBST	Booster output. This circuit generates a voltage about 1.5 V above that of the VPS pin.
41	VSPN	Spindle power supply
44	BESENS	Spindle B-EMF input sensitivity switching pin. 12V: GND short, 5V: open
45	NC	No connection
46	NC	No connection
47	COMM	Sensorless motor startup oscillation time constant. The startup oscillation frequency is determined by the external capacitor and resistor Ccom and Rref.
48	CLKOSC	Clock oscillator circuit. The clock oscillator frequency is determined by the external capacitor and resistor Cclk and Rref.

Block Diagram



Truth Table

Table 1 Overall

CE	OTSD	SPN Driver	FCS Driver	TRR Driver	SLD Driver	TRY Driver
L	X	Z	Z	Z	Z	Z
H	ON	Z	Z	Z	Z	Z
	OFF	ON	ON	ON	ON	ON

Table 2 SPN Driver

BRKSEL	VCTL	SPN Driver
L	> REF + Vdzspn	Forward torque
	REF ± Vdzspn	Z
	< REF – Vdzspn	Short brake
H	> REF + Vdzspn	Forward torque
	REF ± Vdzspn	Z
	< 0.8V	Reverse brake (Full)

Table 3 FCS & TRR Drivers

FCS & TRRIN	P Output	N Output
≤ REF	SINK	SOURCE
≥ REF	SOURCE	SINK

Table 4 SLD Driver

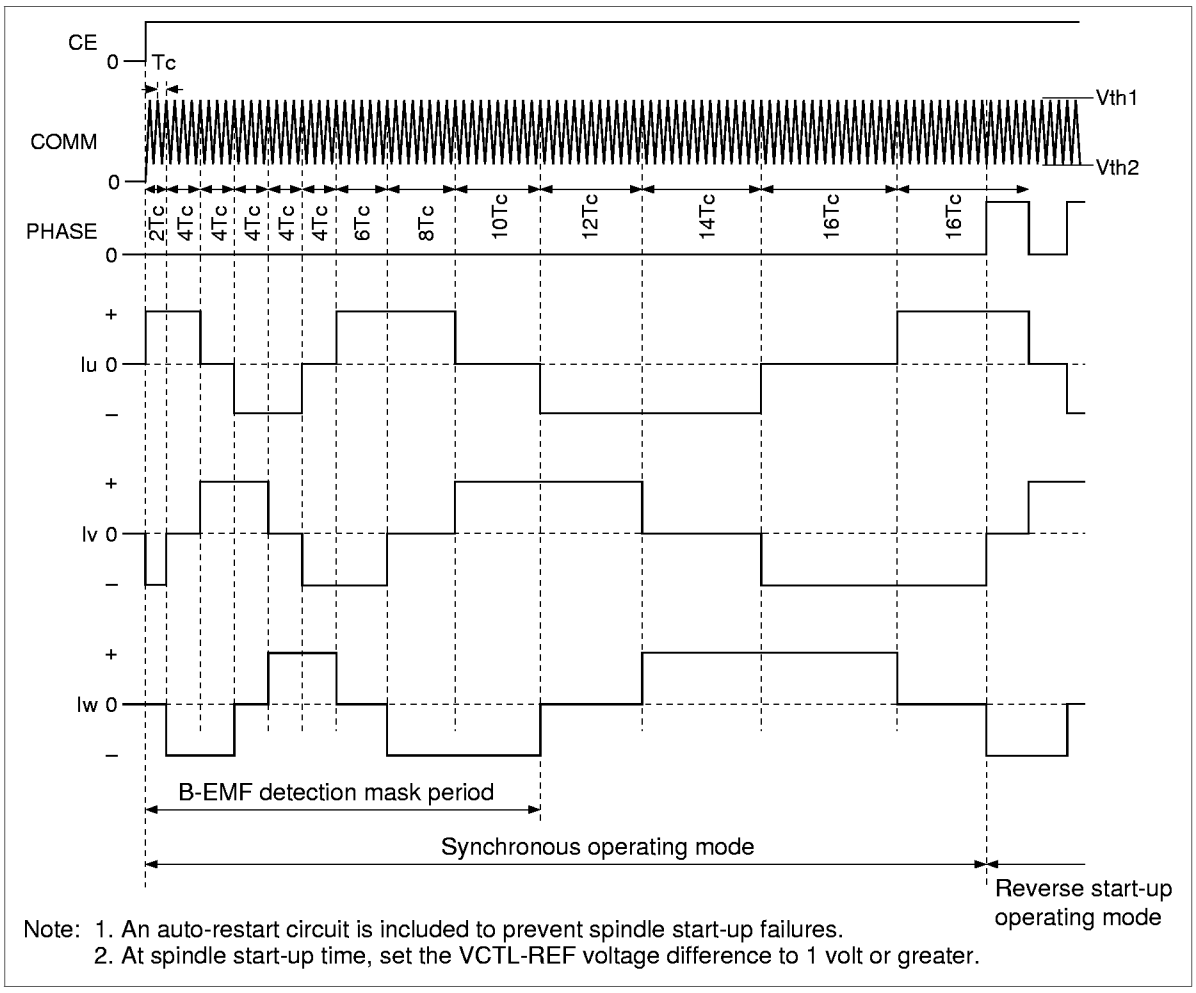
SLDIN	P Output	N Output
> REF + Vdzsld	H	PWM
REF ± Vdzsld	H	Z
< REF – Vdzsld	PWM	H

Table 5 TRY Driver

TRYDIR	TRYIN	P Output	N Output
L	L	Z	H
L	H	L	H
H	L	H	Z
H	H	H	L

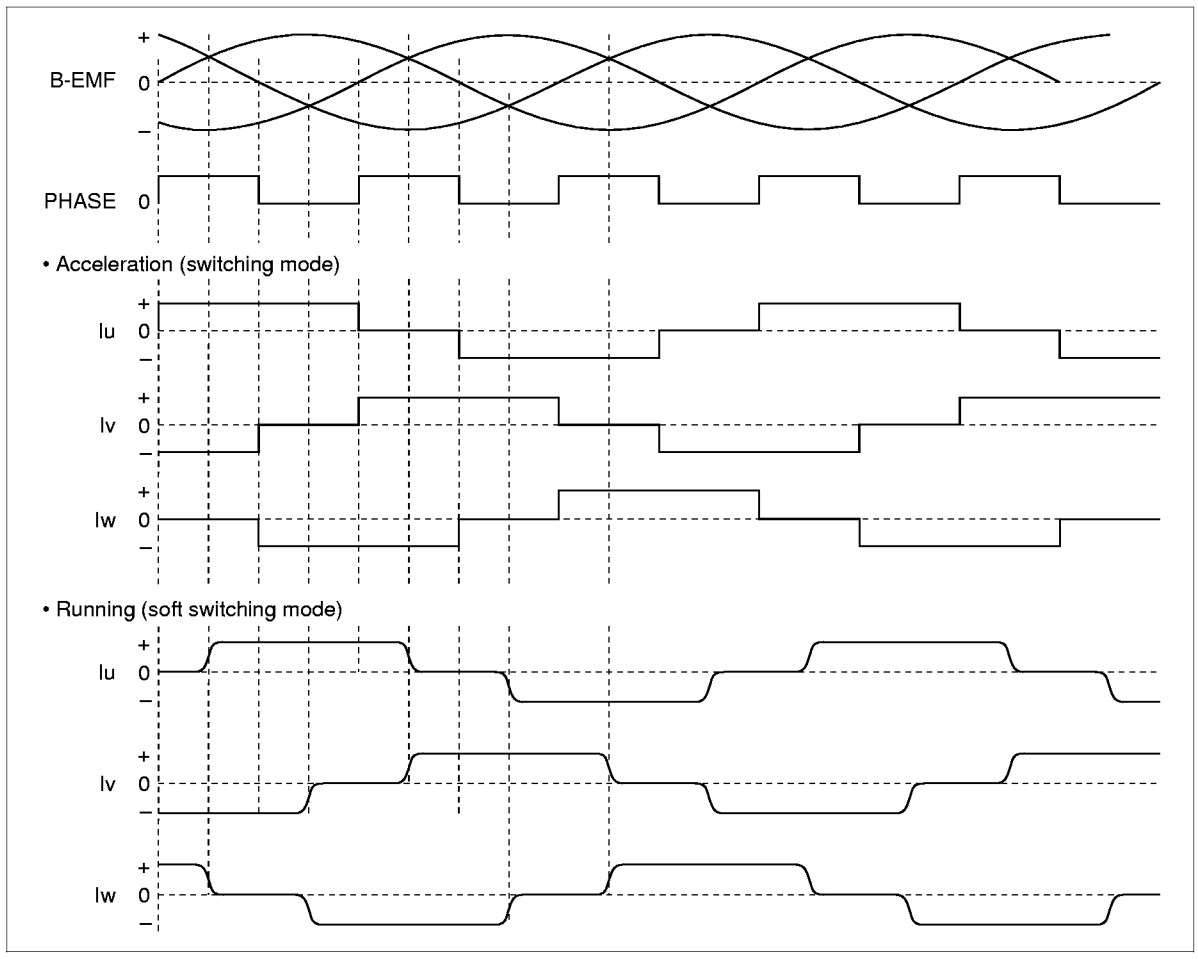
Timing Chart

1. Start-up of Spindle

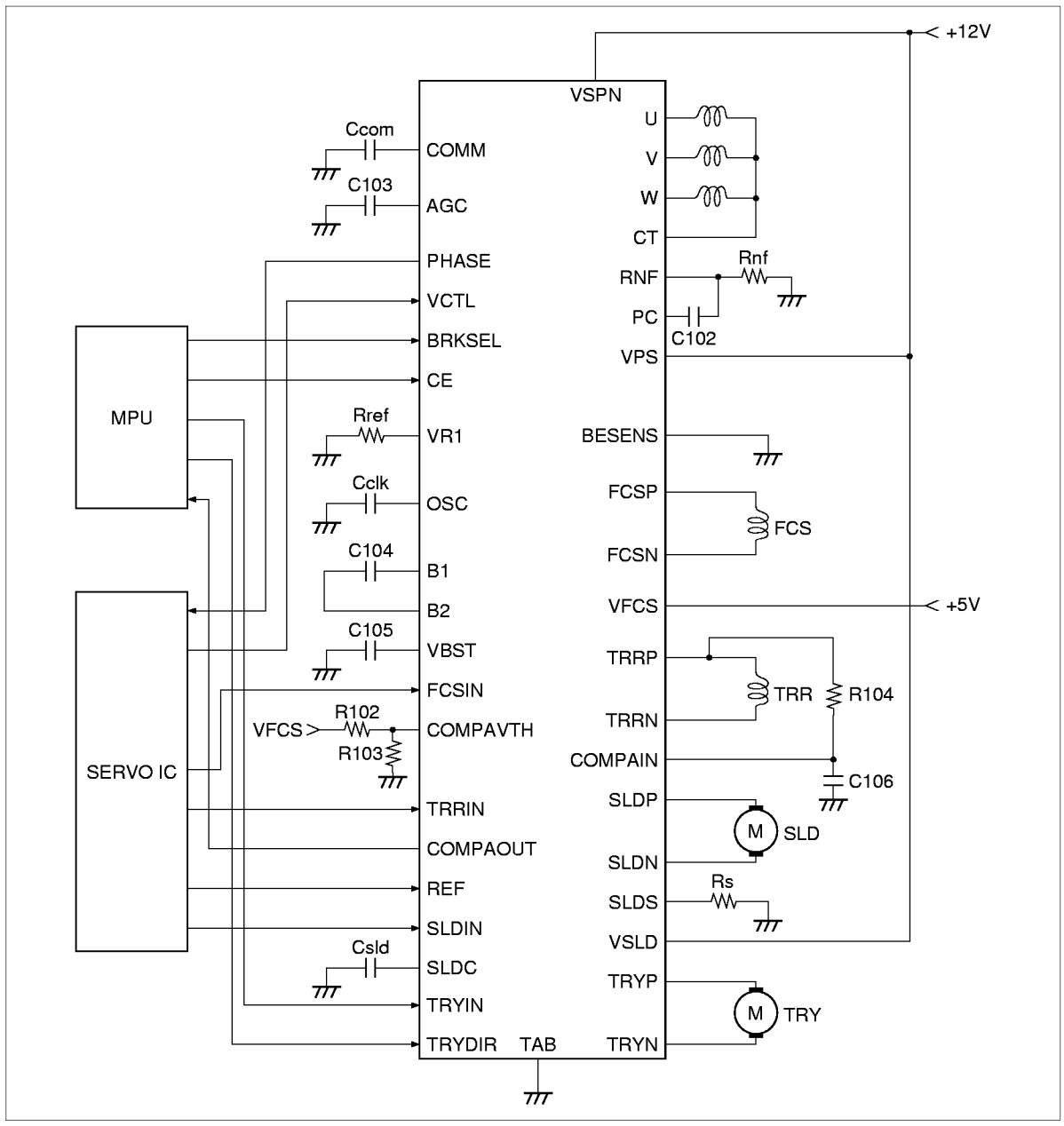


Note: 1. An auto-restart circuit is included to prevent spindle start-up failures.
2. At spindle start-up time, set the VCTL-REF voltage difference to 1 volt or greater.

2. Commutation of Spindle



Application



External Components

Parts No.	Recommended Value	Recommended range	Purpose	Note
R102, R103	—	—	for Amplitude detection voltage setting	
R104	—	—	for Amplitude detection filter	
Rnf	0.47Ω	≥ 0.27Ω	SPN driver current detection resistor	1
Rref	3.3kΩ	≥ 3.3kΩ	for Reference current setting	2 to 4
Rs	0.47Ω	≥ 0.27Ω	SLD driver current detection resistor	5
C102	0.1μF		for Phase compensation for SPN driver current control	
C103	0.1μF		for B-EMF amplitude AGC	
C104	0.1μF		for Booster pomping	
C105	0.47μF		for Booster output smoothing	
C106	—		for Amplitude detection filter	
Ccom	—		for Start-up oscillation	2
Cclk	47pF		for CLK oscillation	3
Csld	680pF		for Slide control offtime determining time constant	4

Notes: 1. The SPN driver maximum output current is determined by the following formula. Here, Vspncl is the current limiter reference voltage. (See the electrical characteristics table.)

$$Iospnmax = \frac{Vspncl}{Rnf}$$

2. Determine this value using the following formula as a guideline.

$$Tcom = \frac{1}{8}\sqrt{\frac{J}{P \cdot Kt \cdot Ispnmax}} \sim \frac{1}{4}\sqrt{\frac{J}{P \cdot Kt \cdot Ispnmax}}$$

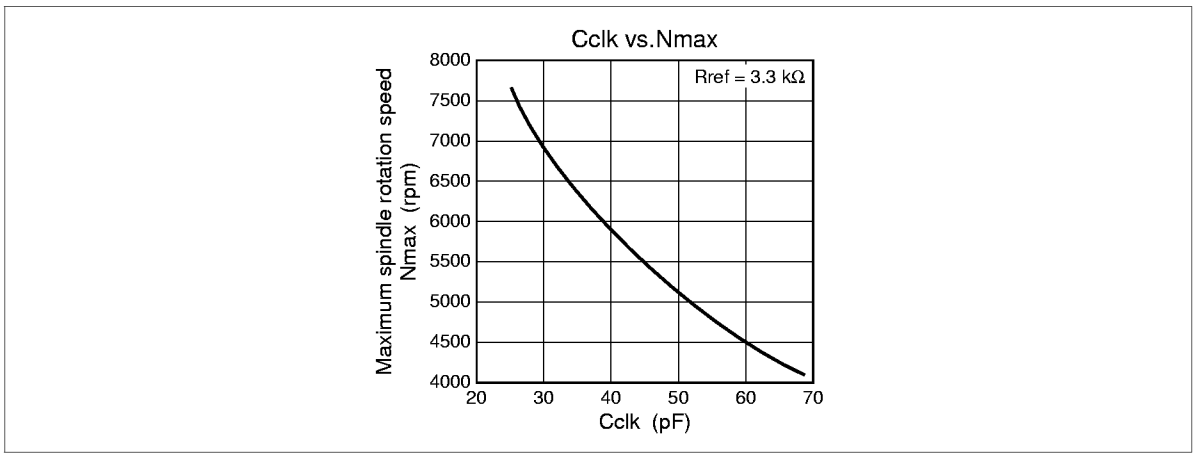
$$Ccom = \frac{Tcom \cdot Vr1}{16 \cdot Rref \cdot \Delta Vthcom}$$

where, J : Spindle inertia [kg · cm · s^2]
P : Number of spindle motor poles [poles]
Kt : Spindle motor torque constant [kg · cm / A]
ΔVthcom : Potential difference between the upper and lower Vth in the startup circuit (ΔVthcom ≈ 1.5V)

3. Determine this value using the following formula as a guideline. Vr1 is the VR1 (pin 7) voltage (See the electrical characteristics table.) and ΔVthclk is the potential difference between the upper and lower Vth. (ΔVthclk is about 1.0 V)

$$Cclk = \frac{Vr1}{16 \cdot fclk \cdot Rref \cdot \Delta Vthclk}$$

Also, the maximum spindle rotation speed depend on the Cclk as following figure.



4. Determine this value using the following formula as a guideline. Here, Vthsld is the SLD control circuit internal threshold voltage. (See the electrical characteristics table.)

$$Csld = \frac{toffsld \cdot Vr1}{8 \cdot Rref \cdot Vthsld}$$

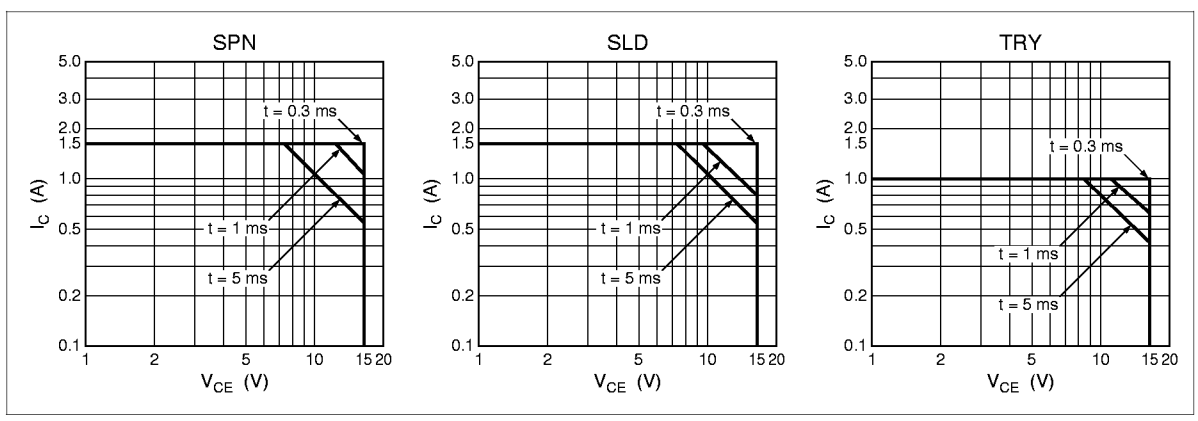
5. The SLD driver maximum output current Iosldmax is determined by the following formula. Here, Vsldcl is the current limiter reference voltage. (See the electrical characteristics table.)

$$Iosldmax = \frac{Vsldcl}{Rs}$$

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Notes
Power supply voltage	Vps	15	V	1
SPN supply voltage	Vspn	15	V	
FCS & TRR supply voltage	Vfcs	7	V	
FCS & TRY supply voltage	Vsld	15	V	
Input voltage	Vin	0 to Vfcs	V	2
SPN output current	Iospn	1.5	A	3
FCS & TRR output current	Iofcs	0.5	A	
TRY output current	Iotry	1.0	A	
SLD output current	Iosld	1.5	A	
Power dissipation	P_T	5	W	4
Junction temperature	Tj	150	°C	1
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. Operating voltage range is shown below.
Vps = 4.25 to 13.8V
Vspn = 2.50 to 15.0V
Vfcs = 4.25 to 5.75V
Vsld = 4.25 to 13.8V
Tjopr = 0 to +135°C
2. Applied to CE, VCTL, FCSIN, TRRIN, SLDIN, TRYIN, TRYDIR and BRKSEL.
3. ASO of each output transistor is shown below.
4. Thermal resistance is shown below.
θj-tab ≤ 12°C/W (preliminary)
θj-a1 ≤ 30°C/W (when mounted on 4 layer multi glass-epoxy board)



Electrical Characteristics (Ta = 25°C, Vps = 12V, Vspn = 12V, Vfcs = 5V, Vsld = 12V)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Quiescent current		Ips0	0	0.01	0.10	mA	Vps=15.0V, CE=L	38	
		Ifcs0	0.25	0.38	0.56	mA	Vfcs=7.0V, CE=L	17	
		Ispn0	0	0.135	0.17	mA	Vspn=14V, CE=L	41	
		Isld0	0	0.01	0.10	mA	Vsld=15V, CE=L	20	
		Ips	7.0	12.0	18.0	mA	Vps=15.0V, CE=H	38	
		Ifcs	26.0	40.0	54.0	mA	Vfcs=7.0V, CE=H	17	1
		Ispn	0	0.11	0.3	mA	Vspn=14V, CE=H	41	
		Isld	2.2	3.0	4.5	mA	Vsld=15V, CE=H	20	
Logic input	Input current	Iince	0	70	100	µA	Vin=0 to Vfcs	22	
		Iin	–10	0	+10	µA		5, 23, 24	
	Low level voltage	Vil	—	—	0.8	V			
	High level voltage	Vih	2.0	—	—	V			
Logic output	Low level voltage	Vol	0.08	0.15	0.4	V	Io=1mA	15, 16	
	Leak current	Icer1	–10	—	+10	µA	Vce=15V		
SPN driver	Output saturation voltage	Vsatspn	0.5	1.0	1.4	V	Iospn=1.0A	32, 33, 34	7
	Leak current	Icer2	0	2.2	3.0	mA	Vce=15V		
	Current limiter voltage	Vspncl	0.30	0.33	0.36	V		31	2
Logic input	Input current	Iinctl	–10	0	+10	µA	Vctl=0 to Vfcs	4	
		Iinref	–20	0	+20	µA	VREF=2 to 3	3	
	REF voltage range	Vref	2.0	—	3.0	V			
	Dead zone voltage	Vdzspn	±50	±75	±100	mV	Vref reference	3, 4	2
	Soft switch	Vsoft1	0.4	—	0.6	V	Vref reference	4	3
	voltage range	Vsoft2	—	2.0	—	Vp-p	VBEMF		
	Current control gain	Gctl	–14	–12.5	–11	dB		3, 4, 31	2

Electrical Characteristics (Ta = 25°C, Vps = 12V, Vspn = 12V, Vfcs = 5V, Vsld = 12V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
FCS & TRR driver	Input current	Iinfcs	–2	0	+2	µA	Vfcsin=0 to Vfcs	3, 6, 7	
	Output saturation voltage	Vsatfcs	0.8	1.45	1.8	V	Io=0.33A	8, 9,10,11	
	Output quiescent voltage	Vqfcs	2.04	2.15	2.22	V	FCSIN=REF TRRIN=REF		
	Input conversion offset voltage	Vosfcs	–20	0	+20	mV			
	Voltage gain	Gvfcs	5	6	7	dB			
	Gain band width	Bfcs	100	200	—	kHz	ΔGv=–3dB		
SLD & TRY driver	Output saturation voltage	Vsatsld	1.3	2.0	2.4	V	Iosld=0.75A	26, 27	
		Vsattry	1.7	2.2	2.6	V	Iotry=0.7A	29, 30	
	Leak current	Icer3	–100	–10	0	µA	Vce=15V	26 to 30	
	Penetration current	Iovlap	0	0	100	mA		20	6
	Transient response time	tplh1	0	0.2	5	µs		26 to 30	
		tphl1	0	0.2	5	µs			
	Current limiter voltage	Vsldcl	0.297	0.33	0.363	V		28	4
SLD control	Input current	Iinsld	–10	0	+10	µA	Vsldin=0 to Vfcs	21	
	Current control gain	Gsld	–14	–12.5	–11	dB		3, 21, 28	4
	Dead zone voltage	Vdzsld	±50	±75	±100	mV	Vref reference		
	Threshold voltage	Vthsld	1.7	2.0	2.3	V		25	
	Charge current	Ichsld	44	50	56	µA	Rref=3.3kΩ		
Amplitude detection	VTH input voltage range	Vinth	0.3	—	1.8	V		14	
	Input current	Iinco	–10	0	+10	µA	Vcompain=0 to V_{FCS} –0.3V	13, 14	5
	Hysteresis	Vhysco	70	100	130	mV			
	Offset voltage	Vofco	–200	0	+200	mV			

Electrical Characteristics (Ta = 25°C, Vps = 12V, Vspn = 12V, Vfcs = 5V, Vsld = 12V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
CLK OSC	Reference voltage	Vr1	1.3	1.4	1.5	V	Rref=3.3kΩ	1	
	Oscillation frequency	f_{CLK}	212	250	288	kHz	Rref=3.3kΩ, Cclk=100pF	48	
Start-up circuit	Oscillation frequency	fcom	140	165	190	Hz	Rref=3.3kΩ, Ccom=0.1μF	47	
	B-EMF Comp input	Viemf	80	100	130	mV	BESENS=0V	32, 33,	
	sensitivity		40	52	70	mV	BESENS OPEN	34, 36	
OTSD	Operating temperature	Tsd	135	160	—	°C			6
	Hysteresis	Thys		50	—	°C			

Note: 1. Ifcs shows a spec with the following conditions.
Vcompavth = 0V, Vctl = Vsldin = Vfcsin = Vtrrin = REF = 2.5V, Vtryin = 0V, Rref = 3.3kΩ, pin DDBST open.

2. See figure 1.

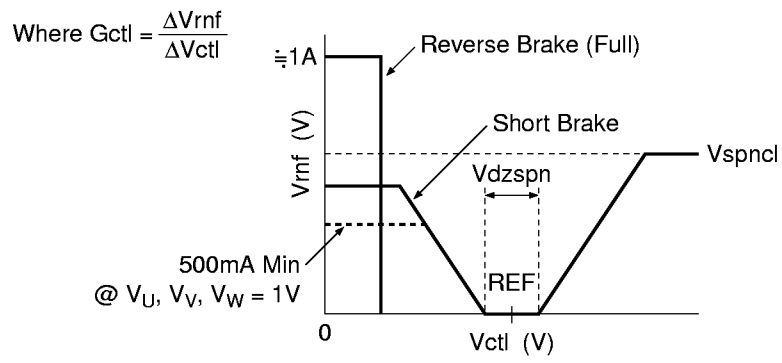


Figure 1

3. Figure 2 show how switching occurs in SW mode and in SOFT SW mode.

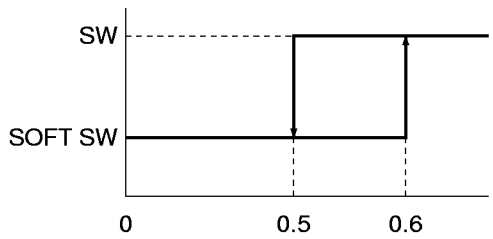


Figure 2

4. See figure 3.

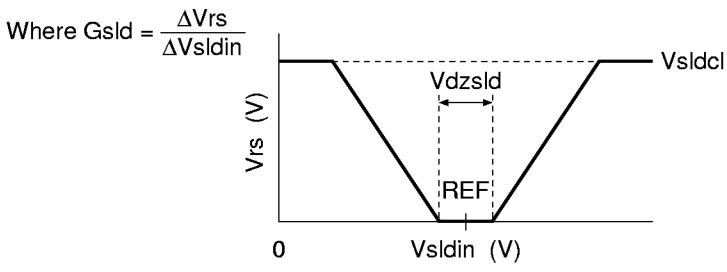


Figure 3

5. See figure 4.

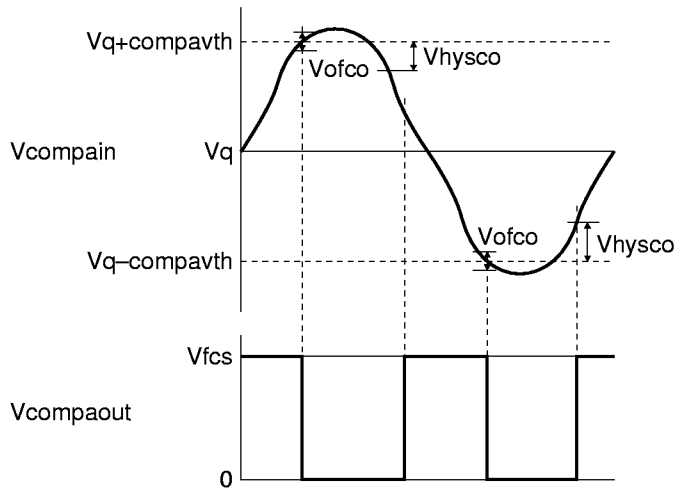
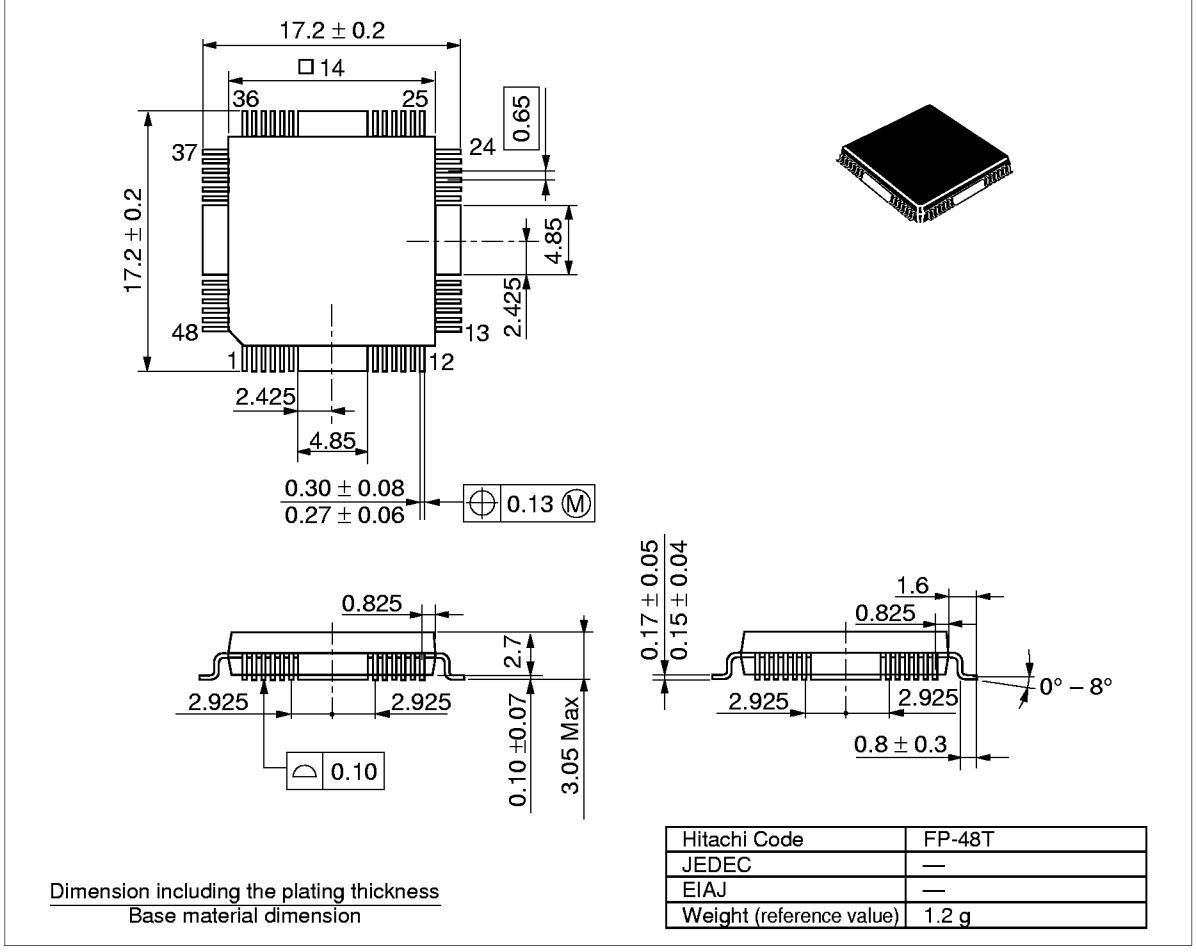


Figure 4

6. Design guide only.
7. When the W → U phase is powered: Vsatspn = 1.3V Typ, Δ1.6V Max.

Package Dimensions

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-48T
JEDEC	—
EIAJ	—
Weight (reference value)	1.2 g