# HA13536F

Three-Phase Brushless DC Motor Driver IC

HITACHI

ADE-207-111B (Z)
3rd Edition
July 1996

## Description

The HA13536F is a 3-phase brushless DC motor driver IC with digital speed control. It is being developed for direct drive of the spindle motor of 5 V floppy disk drives with a height of 3/4" or less. It has the following functions and features.

## Functions

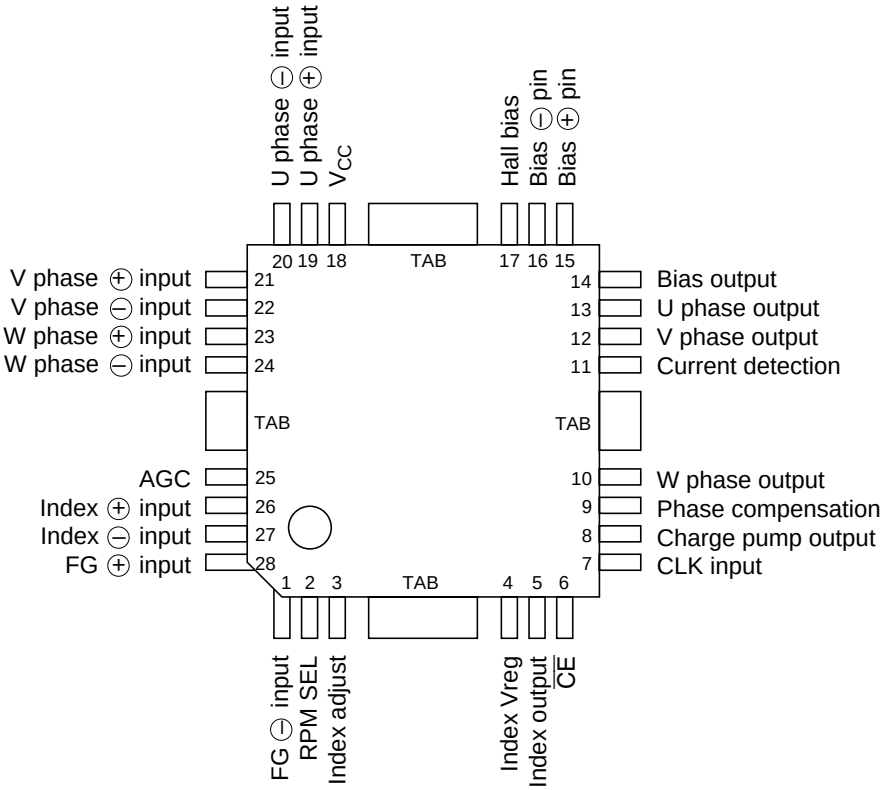
- 1.0 A per phase, 3-phase drive circuit (current driver)
- Digital speed control circuit
- FG Amp
- Index circuit
- Current limiter circuit
- Over-temperature shutdown circuit (OTSD)

## Features

- Low saturation voltage, typically 1.15 V (at 0.7 A)
- Soft switching drive circuit
- No need for an output snubber circuit

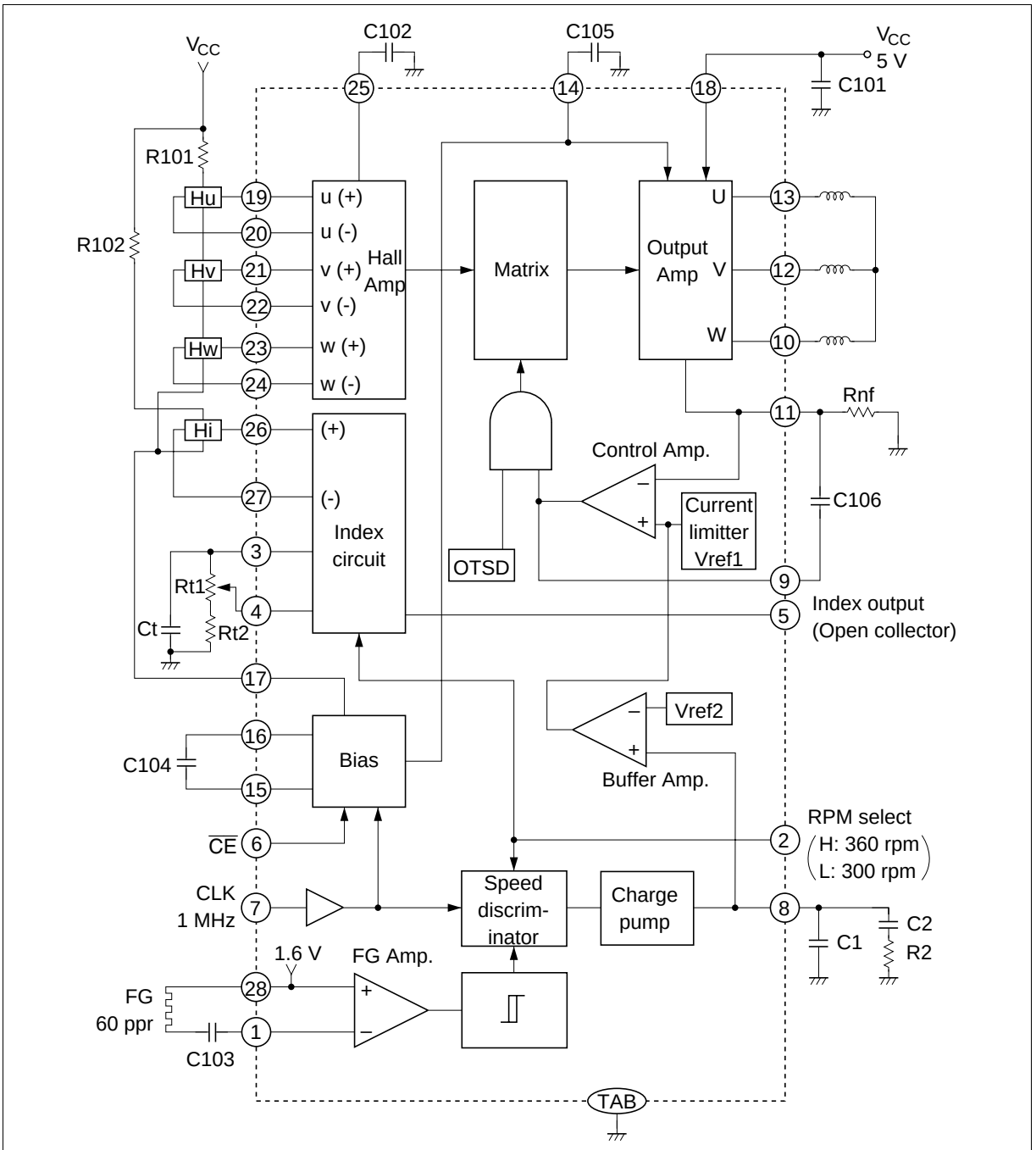
Hitachi semiconductor

## Pin Arrangement




(Top view)

## Block Diagram




Note : Pin arrangement is preliminary specification.

## Pin Function

| Pin Number | Pin Name | Function | Pin Voltage |
|---|---|---|---|
| 1 | FG (–) input | FG Amp. (–) input terminal | |
| 2 | RPMSEL | Change terminal for motor rotation speed<br>"L" → 300 rpm, "H" → 360 rpm | $V_{TH}$ = 1.4 V Typ |
| 3 | Index adjustment | Terminal to set up burst time of index circuit | 0 V Min, 1.2 V Max |
| 4 | Index Vreg | Output terminal for fixed voltage of index circuit | 1.5 V Typ |
| 5 | Index output | Index output terminal (Open collector) | $V_{OL}$ = 0.14 V Typ<br>(@$I_O$ = 2 mA) |
| 6 | $\overline{CE}$ | Chip enable terminal<br>"L": enable, "H": disable | $V_{TH}$ = 1.4 V Typ |
| 7 | CLK input | CLK input terminal | $V_{TH}$ = 1.4 V Typ |
| 8 | C-PUMP output | Speed error Integration and Phase compensation of speed control | |
| 9 | Phase compensation | To prevent the parastic oscillation of output, insert the capacitor between pin 9 and pin 11. | |
| 10 | W phase output | W phase output | |
| 11 | Current detection | Output current detection and terminal which is connected with phase compensation capacitor for carrent control. | |
| 12 | V phase output | V phase output | |
| 13 | U phase output | U phase output | |
| 14 | Bias output | Bias output terminal | |
| 15 | Bias (+) pin | Bias (+) pin terminal | |
| 16 | Bias (–) pin | Bias (–) pin terminal | |
| 17 | Hall bias | Hall bias terminal<br>$\overline{CE}$ = "L" → Bias,<br>$\overline{CE}$ = "H" → High impedance | 2.2 V Typ<br>(@I = 10 mA) |
| 18 | $V_{CC}$ | Power supply | 4.25 V Min, 6.5 V Max |
| 19 | U phase (+) input | U phase (+) input terminal | 2.0 V Min,<br>$V_{CC}$ – 0.5 V Max |
| 20 | U phase (–) input | U phase (–) input terminal | 2.0 V Min,<br>$V_{CC}$ – 0.5 V Max |
| 21 | V phase (+) input | V phase (+) input terminal | 2.0 V Min,<br>$V_{CC}$ – 0.5 V Max |
| 22 | V phase (–) input | V phase (–) input terminal | 2.0 V Min,<br>$V_{CC}$ – 0.5 V Max |
| 23 | W phase (+) input | W phase (+) input terminal | 2.0 V Min,<br>$V_{CC}$ – 0.5 V Max |
| 24 | W phase (–) input | W phase (–) input terminal | 2.0 V Min,<br>$V_{CC}$ – 0.5 V Max |
| 25 | AGC | Hall amp output wave form adjustment terminal<br>(Insert capacitor C102 between GND) | |

## Pin Function (cont)

| Pin Number | Pin Name | Function | Pin Voltage |
|---|---|---|---|
| 26 | Index (+) input | Index amp (+) input terminal | 1.4 V Min,<br>$V_{CC}$ – 0.5 V Max |
| 27 | Index (–) input | Index amp (–) input terminal | 1.4 V Min,<br>$V_{CC}$ – 0.5 V Max |
| 28 | FG (+) input | FG amp (+) input terminal | DC bias 1.6 V Typ |

## External Parts

| Part Number | Recommended Value | Purpose | Notes |
|---|---|---|---|
| R2 | — | Integration constant | 1 |
| R101 | — | Hall bias | |
| R102 | — | Index hall bias | |
| Rnf | — | Current detection and limitation | 2 |
| Rt1 | 0 to 50 kΩ | Index burst adjustment | 3 |
| Rt2 | 100 kΩ | Index pulse width setting | |
| C1, C2 | — | Integration constants | 1 |
| C101 | ≥ 0.1 µF | Power supply bypass | 4 |
| C102 | 0.1 µF | AGC filter | 5 |
| C103 | 0.47 µF | FG amp. coupling | 5 |
| C104 | 0.1 µF | Bias | |
| C105 | ≥ 0.1 µF | Bias | 7 |
| C106 | 0.1 µF | Phase compensation | 4 |
| Ct | 0.1 µF | Index setting | 3, 6 |

Notes: 1. Determine the integration constants from the following formulas:

$$\omega_O \leq \frac{2\pi f_{FG}}{20} \quad \text{(rad/s)}$$

$$R2 = \frac{1}{9.55} \cdot \frac{J\omega_O N_O \cdot Rnf}{K_T Gctl\ Icp} \quad (\Omega)$$

$$C1 = \frac{1}{\sqrt{10}} \cdot \frac{1}{\omega_O R2} \quad \text{(F)}$$

$$C2 = 10C1 \quad \text{(F)}$$

In the above formulas:

$\omega_O$ = Time constant of servo loop

$f_{FG}$ = FG frequency in Hz

$N_O$ = Motor speed in rpm

J = Motor moment of inertia in kg•cm•$s^2$

$K_T$ = Motor torque constant in kg•cm/A

Rnf = Current detection in Ω

Gctl = Control amp gain (see Electrical Characteristics)

Icp = Charge pump output current (see Electrical Characteristics)

2. The current limiter operates according to the following formula:

$$I_{OMAX} = \frac{Vref1}{Rnf} \quad (A)$$

where Vref1 is the current limiter reference voltage (see Electrical Characteristics)

3. The burst time t1 is defined as follows:

$t1 \approx -Ct \times Rt1' \times \ln (1 - Vth1\ (L) / Vreg)$ (RPM select input low)

$t1 \approx -Ct \times Rt1' \times \ln (1 - Vth1\ (H) / Vreg)$ (RPM select input high)

where Rt1' is resistance value inter 3 to 4 pin.

4. Place as close to the IC as possible.
5. Determine C102 and C103 according to the following formulas:

$$C102 \geq \frac{200}{N_O P} \quad (\mu F)$$

$$C103 \geq \frac{100}{f_{FG}} \quad (\mu F)$$

where

P = Number of motor poles

6. The index pulse width t2 is determined as follows:

$t2 \approx -Ct \times Rt2' \times \ln (Vth1 / Vth2)$

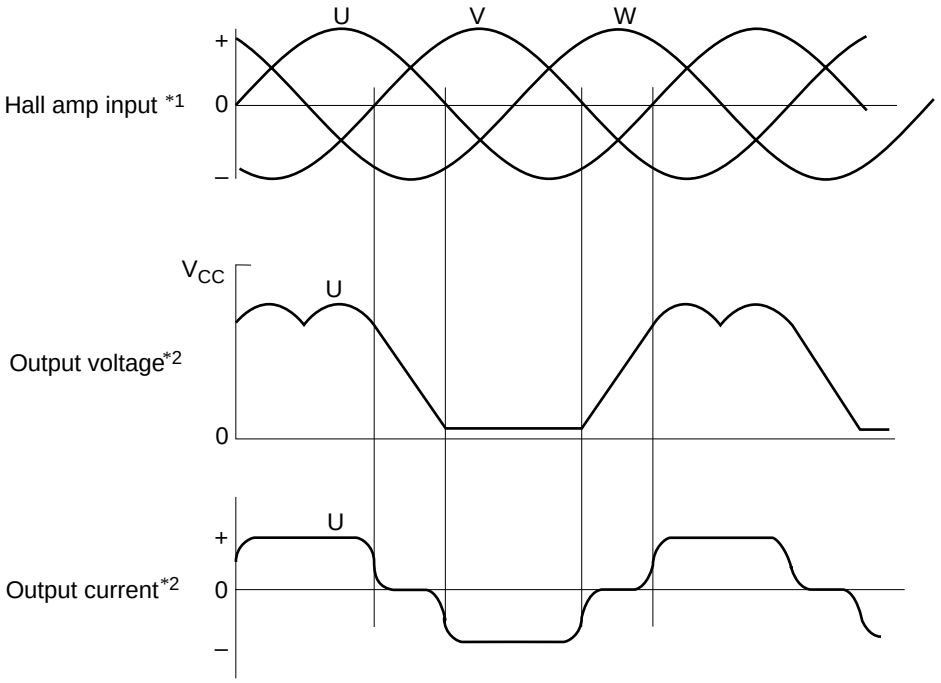
where Vth2 is the threshold voltage (see Electrical Characteristics).

Rt2' : Rt1 (max) + Rt2

7. If the circuit is affected by noise, a large capacitance value should be set.

## Timing Waveforms

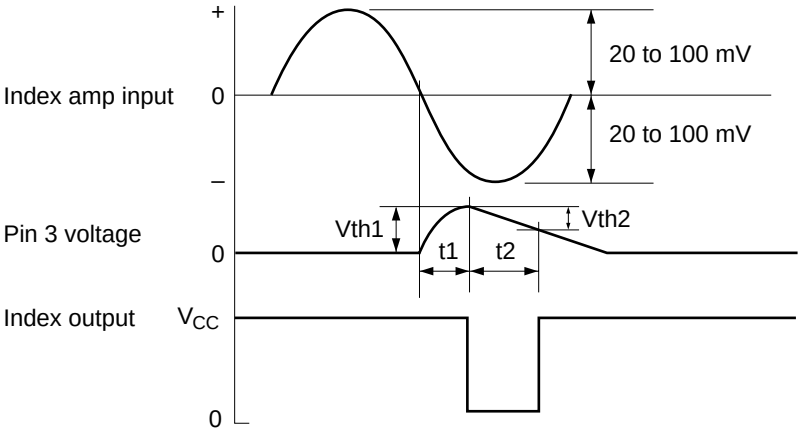
### Hall Amp Input vs. Output Voltage and Current



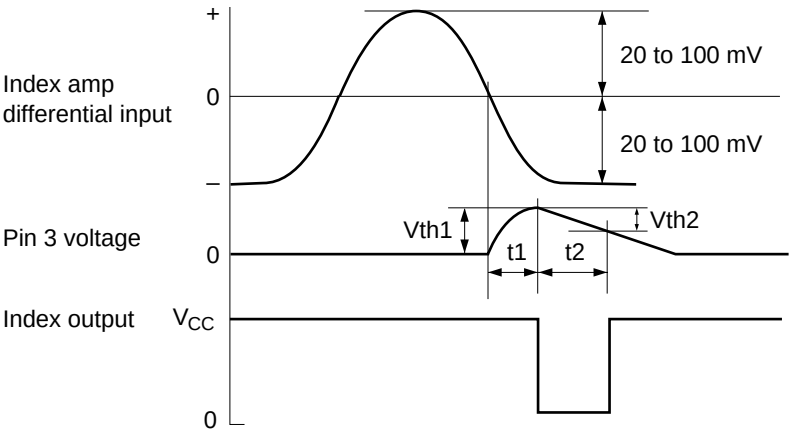

Notes: 1. The input waveforms to the hall amp should be sine waves with a third harmonic content of less than 20%.
2. Only the U phase output is shown.

**Index Amp Input vs. Output**

- Application 1




- Application 2



## Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 7 | V | 1 |
| Input voltage | Vin | 0 to $V_{CC}$ + 0.3 | V | 2 |
| Peak output current | $I_{OP}$ | 1.0 | A | |
| Normal output current | $I_O$ | 0.7 | A | |
| Power dissipation | $P_T$ | 1.5 | W | 3 |
| Junction temperature | Tj | +150 | °C | 1 |
| Storage temperature range | Tstg | –55 to +125 | °C | |

Notes: 1. The operating ranges is:
$V_{CC}$ = 4.25 to 6.5 V
Tjopr = 0 to +125°C
2. Applied to the $\overline{CE}$, CLK, and RPM SEL pins.
3. Permissible value when Tpin = 113°C and thermal resistance is as follows:
$\theta_{j-pin} \leq 25$°C/W
$\theta_{j-a1} \leq 55$°C/W (when mounted on a metal substrade)
$\theta_{j-a2} \leq 80$°C/W (when mounted on a glass epoxy substrade)

## Electrical Characteristics (Ta = 25°C, $V_{CC}$ = 5 V)

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions | Pin Nos. | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Quiscent current | | $I_{CCO}$ | — | — | 0.45 | mA | $\overline{CE}$ = H, $V_{CC}$ = 6.5 V | 18 | |
| | | $I_{CC}$ | — | 9 | 13 | mA | $\overline{CE}$ = L, $V_{CC}$ = 6.5 V | | |
| Logic input | Input current (6 pin) | $I_{I1}$ | –80 | — | 2 | µA | $\overline{VCE}$ = 0 to 6.5 V | 2, 6, 7 | |
| | Input current (2 pin) | $I_{I2}$ | –2 | — | 100 | µA | $V_{RPM}$ = 5.5 V | | |
| | Input current (7 pin) | $I_{I3}$ | –2 | — | 450 | µA | $V_{CLK}$ = 5.5 V | | |
| | Input low voltage | $V_{IL}$ | 0 | — | 0.8 | V | | | |
| | Input high voltage | $V_{IH}$ | 2.0 | — | 5.5 | V | | | |
| Logic output | Output low voltage | $V_{OL}$ | — | — | 0.4 | V | $I_O$ = 2 mA | 5 | |
| | Leakage current | $I_{OH}$ | — | — | ±10 | µA | $V_{CE}$ = 7.0 V | | |
| Hall amp | Input resistance | Rhi | 7 | 10 | 13 | kΩ | | 19 to 24 | |
| | Common-mode input voltage range | $V_H$ | 2.0 | — | $V_{CC}$ – 0.5 | V | | | |
| | Differential input voltage range | Vh | 30 | — | 160 | $mV_{PP}$ | | | |
| Output amp | Leakage current | $I_{CER(H)}$ | 0 | — | 5 | mA | $V_O$ = 7.0 V | 10, 12, 13 | |
| | | $I_{CER(L)}$ | — | — | ±100 | µA | $V_O$ = 0 V | | |
| | Saturation voltage | Vsat1 | — | 1.15 | 1.65 | V | $I_O$ = 0.7 A | | 1 |
| | | Vsat2 | — | 0.6 | 0.85 | V | $I_O$ = 0.35 A | | |
| FG amp and detector | Input voltage range | Vfg | 2 | — | 20 | $mV_{PP}$ | | 1, 28 | |
| | Noise margin | nd | — | — | 0.5 | $mV_{PP}$ | Differential Noise | | |
| | | nc | — | — | 0.5 | V | COMMON Noise | | |

**Electrical Characteristics** (Ta = 25°C, $V_{CC}$ = 5 V) (cont)

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions | Pin Nos. | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Speed discriminator and charge pump | Number of counts | N | — | 1666.5 | — | — | PRMSEL = L | | |
| | | | — | 1388.5 | — | — | PRMSEL = H | | |
| | Operating frequency | $f_{CLK}$ | 0.9 | 1.0 | 1.1 | MHz | | 7 | |
| | Leakage current | Ioff | — | — | ±50 | nA | V8 = 0.8 V | 8 | |
| | Output current | Icp+ | 7 | 10 | 13 | µA | Speed reduction full scale | | |
| | | Icp– | –7 | –10 | –13 | µA | Acceleration full scale | | |
| Current control | Threshold voltage | Vref2 | 0.55 | 0.63 | 0.71 | V | | 8 | 2 |
| | Voltage gain | Gctl | –12 | –10 | –8 | dB | | 11 | |
| | Current limitter voltage | Vref1 | 157 | 175 | 193 | mV | $R_{NF}$ = 0.47 Ω | | |
| Index circuit | Input voltage (common) | Vindex | 1.4 | — | $V_{CC}$ – 0.5 | V | | 26, 27 | 3 |
| | Input voltage (different) | Vindex | 40 | — | 300 | mVpp | | | |
| | Hysteresis | hys | — | 14 | — | mV | | | |
| | Input current | | — | — | ±2 | µA | | 3 | |
| | Threshold voltage | Vth1 | 0.60 × Vreg | 0.64 × Vreg | 0.68 × Vreg | V | RPM select = L | | |
| | | | 0.54 × Vreg | 0.58 × Vreg | 0.62 × Vreg | V | RPM select = H | | |
| | Ct discharge threshold voltage | Vth2 | 0.50 × Vreg | 0.54 × Vreg | 0.58 × Vreg | V | RPMSEL = L | 3 | 3 |
| | | | 0.44 × Vreg | 0.48 × Vreg | 0.52 × Vreg | V | RPMSEL = H | | |
| | Bias | Vreg | 1.3 | 1.5 | 1.7 | V | $I_O$ = –0.2 mA | 4 | |
| Hall bias | Output voltage | Vhb | 1.9 | 2.2 | 2.5 | V | Ih = 10 mA, $\overline{CE}$ = L | 17 | |

## Electrical Characteristics (Ta = 25°C, $V_{CC}$ = 5 V) (cont)

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions | Pin Nos. | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Hall bias | Leakage current | Ihof | — | — | ±10 | µA | $\overline{CE}$ = H, Vhb = 7.0 V | 17 | |
| OTSD | Operating temperature | Tsd | 125 | 150 | — | °C | | | 4 |

Notes: 1. Total of sink and source.
2. See figure 1. Gctl = ΔVrnf/ΔVcp.
3. Refer to the timing chart.
4. Design parameter only (No test).

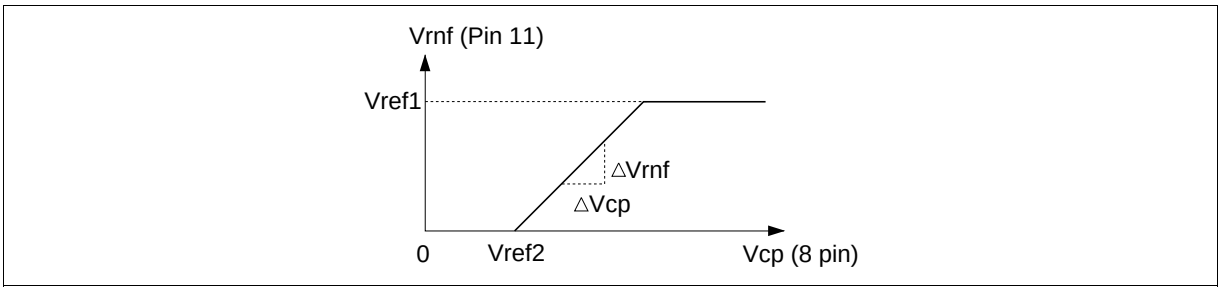
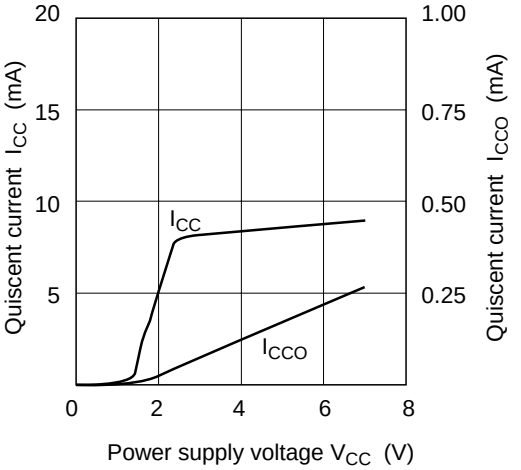
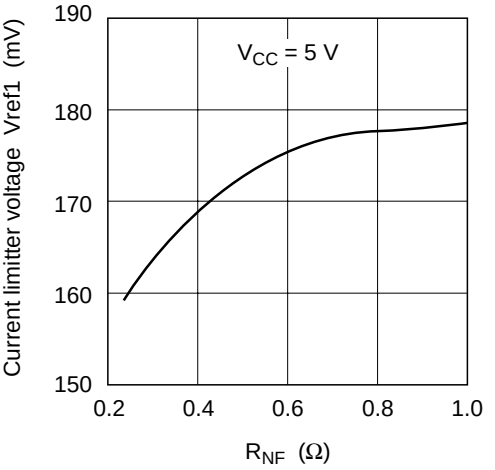
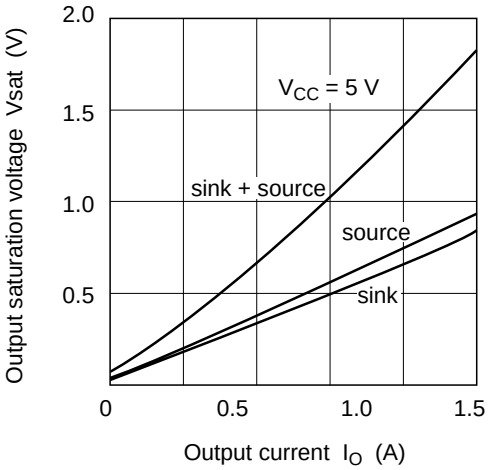


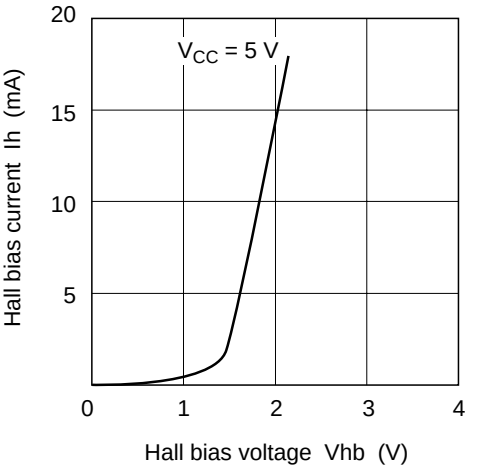

**Figure 1**

## Reference Data

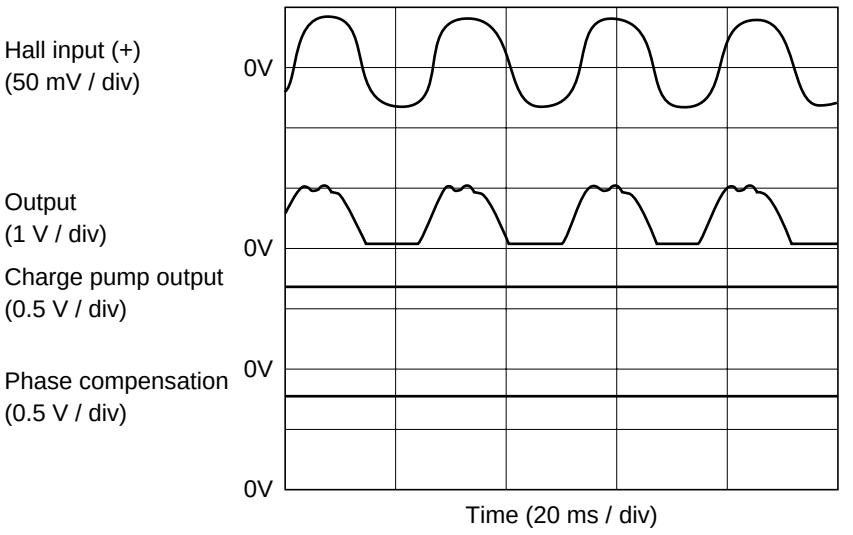


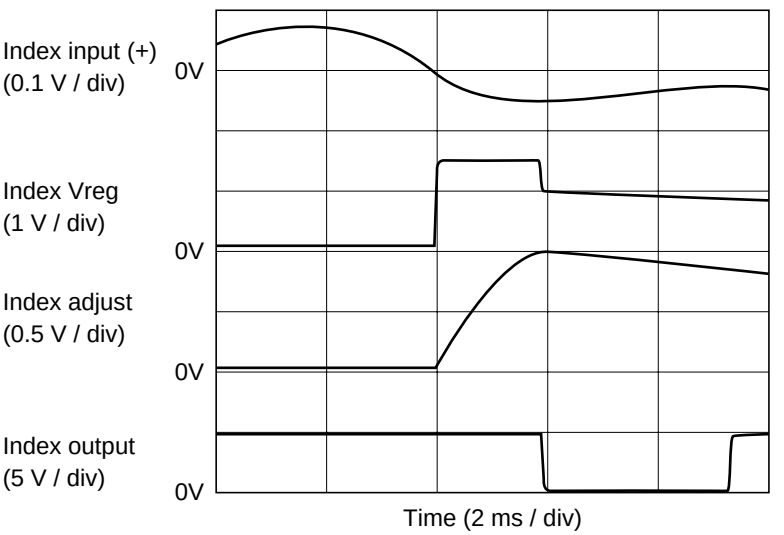



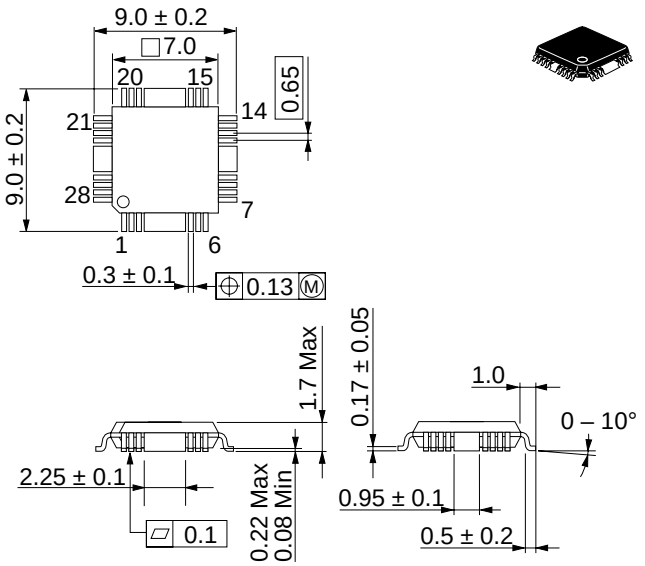
## Mount Waveform Characteristics



## Package Dimensions

Unit: mm

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# HITACHI

**Hitachi, Ltd.**
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
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**For further information write to:**

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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