HYBRID MCU/DSP

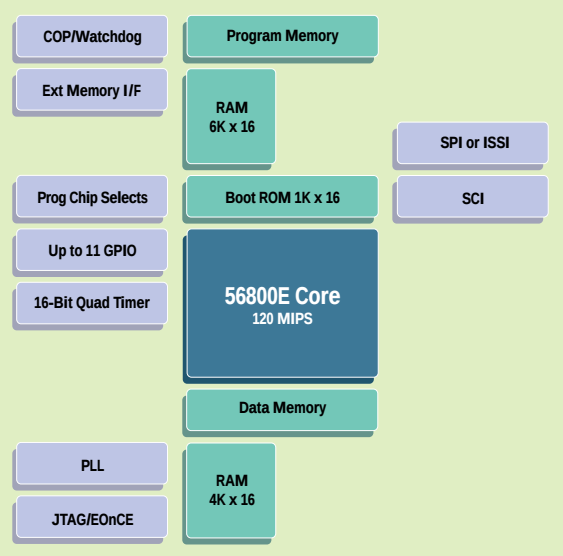
56852

120 MIPS Hybrid Processor

TARGET APPLICATIONS

- Full duplex feature phones
- Voice activated toys
- Voice recognition and command
- Musical effects equipment
- Kareoke systems
- Voice and audio processing
- General purpose applications

The first device in the 56800E family, the 56852 sets a new price per performance standard, offering 120 MIPS below $3.00 at high volume. The 56852 integrates 6K words of program SRAM and 4K words of data SRAM, a quad timer module with two external outputs, a serial peripheral interface (SPI) multiplexed with an improved synchronous serial interface (ISSI), and a serial communication interface (SCI/UART). With 10K words of on-chip SRAM and multiple serial peripherals in an 81-pin MBGA package, the 56852 can easily be integrated into a previously designed system where a DSP co-processor is needed and system board real estate is at a premium. However, with up to 2M words of program or up to 6M words of data addressing space for off-chip memory, the 56852 is also a powerful stand-alone processor ideal for telephony applications, speech processing and recognition, embedded modems, audio processing, such as 3D virtualization and other digital effects, echo cancellation, magnetic and smart card readers, and feature phones.



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BENEFITS

- 120 MIPs at under $3 in high volume
- Hybrid MCU/DSP architecture, removes need for separate MCU in many cases
- Large linear address spaces, up to 4MB program and data, supporting complex communications stacks
- Available in a space saving 81MAPBGA package
- Supported by Metrowerks Codewarrior IDE, allowing rapid application development in C
- Non intrusive debug via JTAG/OnCE port
- Software Development Kit available including algorithms and drivers

56852 16-BIT DIGITAL SIGNAL PROCESSORS

- 120 MIPS at 120MHz
- 6K x 16-bit Program SRAM
- 4K x 16-bit Data SRAM
- 1K x 16-bit Boot ROM
- Access up to 2M words of program memory or up to 6M of data memory
- One Serial Peripheral Interface (SPI) or one Improved Synchronous Serial Interface (ISSI)
- One Serial Communication Interface (SCI)
- Interrupt Controller
- General purpose 16-bit Quad Timer
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- 81-pin MAPBGA package
- Up to 11 GPIO

ENERGY INFORMATION

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

HYBRID MCU/DSP

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PRODUCT DOCUMENTATION

DSP56800E Reference Manual	Detailed description of the 56800E architecture, 16-bit DSP core processor and the instruction set Order Number: DSP56800ERM/D
DSP56852 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56852 Order Number: DSP56852UM/D
DSP56852 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions Order Number: DSP56852/D
DSP56852 Product Brief	Summary description and block diagram of the core, memory, peripherals and interfaces Order Number: DSP56852PB/D

"BEST IN CLASS" DEVELOPMENT ENVIRONMENT

- The Software Development Kit (SDK) provides fully debugged peripheral drivers, libraries and interfaces that allow a programmer to create his own unique C application code independent of component architecture.
- The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, the SDK, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast and efficient development.

56800E CORE FEATURES

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications. Features of the 56800E core include:

- Efficient 16-bit hybrid controller engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Four hardware interrupt levels
- Five software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

56852 MEMORY FEATURES

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip Memory:
  - 6K x 16-bit Program SRAM
  - 4K x 16-bit Data SRAM
  - 1K x 16-bit Boot ROM
- Off-Chip Memory Expansion
- Access up to 2M words of program memory or up to 6M data memory
- Chip Select Logic for glueless interface to ROM and SRAM

56852 PERIPHERAL CIRCUIT FEATURES

- General Purpose 16-bit Quad Timer with two external pins*
- One Serial Communication Interface (SCI)*
- One Serial Port Interface (SPI) or one Improved Synchronous Serial Interface (ISSI) module*
- Interrupt Controller
- Computer Operating Properly (COP)/Watchdog Timer
- JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, real-time debugging
- 81-pin MAPBGA package
- Up to 11 GPIO

* *Each peripheral I/O can be used alternately as a General Purpose I/O*

ORDERING INFORMATION

PART	SUPPLY VOLTAGE	PACKAGE TYPE	PIN COUNT	FREQUENCY (MHz)	ORDER NUMBER
DSP56852	1.8V, 3.3V	Map Ball Grid Array (MBGA)	81	120	DSP56852VF120

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DSP56852PB/D
REV 2