

Symphony™ DSP56721 Multi-Core Audio Processor Product Brief

The Symphony™ DSP56721 Multi-Core Audio Processor is part of the DSP5672x family of programmable CMOS DSPs, designed using multiple DSP56300 24-bit cores.

The DSP56721 is intended for automotive, consumer, and professional audio applications that require high performance for audio processing. Potential applications include A/V receivers, HD-DVD and Blu-Ray players, car audio/amplifiers, and professional audio equipment.

The DSP56721 excels at audio processing for automotive and consumer audio applications requiring high MIPS. Higher MIPS and memory requirements are driven by the new high-definition audio standards (Dolby Digital+, Dolby TrueHD, DTS-HD, for example) and the desire to process multiple audio streams. In addition, the DSP56721 is optimal for the professional audio market requiring audio recording, signal processing, and digital audio synthesis.

The DSP56721 provides a wealth of on-chip audio processing functions, via a plug and play software

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Block Diagram

architecture system which has the ability to support audio decoding algorithms, various equalization algorithms, compression, signal generator, tone control, fade/balance, level meter/spectrum analyzer, among others. The DSP56721 also supports various matrix decoders and sound field processing algorithms.

With two DSP56300 cores, a single DSP56721 device can replace dual-DSP designs, saving costs while meeting high MIPs requirements. Legacy peripherals from the previous DSP5636x/7x families are included, as well as a variety of new modules. Included among the new modules are an Asynchronous Sample Rate Converter (ASRC), Inter-Core Communication (ICC), and a Sony/Phillips Digital Interface (SPDIF).

1 Block Diagram

The following figure shows the block diagram for the DSP56721 device.

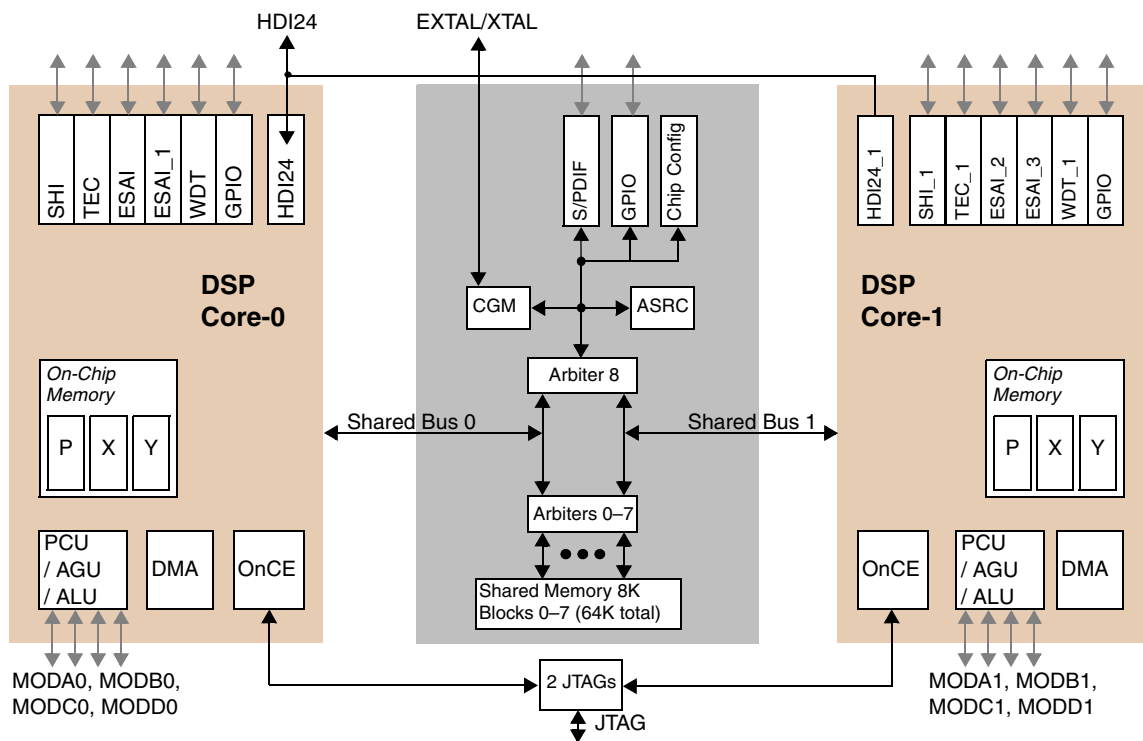


Figure 1. DSP56721 Block Diagram

2 Features

The DSP56721 processor includes the following features:

- Two enhanced DSP56300 cores that are integrated, replacing two DSPs in designs, lowering costs and meeting high MIPs requirements: a minimum 400 million instructions per second in total (200 MIPs/core) using a 200 MHz clock. Each core in the DSP56721 has the following features:
 - Highly parallel instruction set
 - Hardware debugging support (JTAG TAP, OnCE™ module)

- Eight-channel DMA (Direct Memory Access) controller
- Wait and Stop low-power standby modes
- Configurable and flexible arbitration methods for shared peripherals and shared memory blocks.
- Powerful audio data communication abilities:
 - Four Enhanced Serial Audio Interface (ESAI) modules to transmit and receive audio data., with two ESAI modules per core. Each ESAI module includes up to 4 receivers and 6 transmitters, master or slave. I²S, Left-justified, Right-justified, Sony, AC97, network and other programmable protocols are supported.
 - One SPDIF module that is shared by the cores to transmit and receive audio data in IEC958 format.
- Powerful host communication ports:
 - Two Serial Host Interface (SHI) modules, with one SHI per core. The SHI modules support SPI and I²C protocols, multi-master capability in I²C mode, 10-word receive FIFO, and support for 8, 16 and 24-bit words.
 - Two parallel Host Interface (HDI24) modules with DMA support, with one HDI24 per core. The HDI24 modules support 8, 16 and 24-bit host interfaces. Each HDI24 module is a full-duplex, double-buffered parallel port that can connect directly to the data bus of a host processor.
- Two triple-timer modules (TEC), with one TEC per core
- Two watchdog timer modules (WDT) to prevent software runaway conditions, with one WDT per core
- Seamless hardware Asynchronous Sampling Rate Converter (ASRC) module, to support different sample rate audio data transmission and reception. The ASRC can be accessed by both DSP cores.
 - Supports three data sampling rate convert pairs at the same time
 - Different data sampling rate convert pairs can be used by different cores at the same time
- Inter-Core Communication (ICC) module:
 - 64K shared memory between two DSP cores
 - Supports a flexible arbitration system which allows multiple methods of arbitration
 - Non-maskable and maskable interrupts between the two cores
 - Poll data registers for simple data transfer
- As many as 79 GPIO pins, shared with other peripherals function pins. The actual number of pins is different for different packages.

2.1 Dual DSP56300 Cores

The DSP56721 contains two enhanced DSP56300 cores. Together, the two cores provide over twice the performance of Freescale's popular DSP56371 processor, while retaining code compatibility.

The DSP56300 core offers a high level of performance in speed and power, provided by its rich instruction set and low power dissipation. For more about core features, see the *DSP56300 Family Manual* (order number: DSP56300FM).

Features

Each DSP56721 core contains its own set of peripherals: PIC, DMA, HDI24, ESAI, SHI, triple timer, watchdog timer, patch module, and internal memory, which are described in the following sections.

2.2 Core Modules

The following sections describe the various modules that are present with each DSP56721 core. These modules are similar or identical to the modules present in DSP5636x/7x devices.

2.2.1 Internal Core Memory

The memory space of each DSP56721 core is partitioned into three memory spaces: program memory space, X data memory space, and Y data memory space.

Table 1. Memory Map Options for Core-0

Bit Settings			Memory Sizes (24-Bit Words)		
			RAM		
MSW1	MSW0	MS	Program	X Data	Y Data
X	X	0	8K	36K	48K
0	0	1	36K	32K	24K
0	1	1	32K	36K	24K
1	0	1	24K	36K	32K
1	1	1	16K	36K	40K

Table 2. Memory Map Options for Core-1

Bit Settings			Memory Sizes (24-Bit Words)		
			RAM		
MSW1	MSW0	MS	Prog	X Data	Y Data
X	X	0	8K	36K	48K
0	0	1	36K	32K	24K
0	1	1	32K	36K	24K
1	0	1	24K	36K	32K
1	1	1	16K	36K	40K

2.2.2 Direct Memory Access (DMA) Controller

The DMA module permits data transfers without the interaction of a core, and supports any combination of internal memory, internal peripheral I/O and external memory as source and destination during accesses. However, the DSP56721 DMA has been enhanced to support up to 8 DMA channels per core. Additionally, each DMA channel receives its own 32 request lines, allowing more flexibility in the DMA request sources for different channels, and potential support for a greater number of DMA request sources. The DMA module features:

- Eight DMA channels that support internal and external accesses
- One-, two-, and three-dimensional transfers (including circular buffering)
- End-of-block-transfer interrupts
- Triggering from interrupt lines and all peripherals

The DMA module is fully described in the *DSP56300 Family Manual*.

2.2.3 Programmable Interrupt Controller (PIC)

The Program Interrupt Controller arbitrates among all interrupt requests (internal interrupts and the five external requests IRQA, IRQB, IRQC, IRQD, and NMI), and generates the appropriate interrupt vector address. PIC features include:

- Supports both maskable and non-maskable interrupts
- Supports additional DMA and peripheral interrupts. Allows up to 18 DMA and 24 peripheral interrupts
- Supports nine non-maskable interrupts

Refer to the *DSP56300 Family Manual* for more information about the PIC module.

2.2.4 Enhanced Serial Audio Interface (ESAI)

The ESAI module provides a full-duplex serial port for serial communications with a variety of serial devices, including industry-standard codecs, S/PDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, with each section having its own clock generator. There are two ESAI modules per DSP core.

2.2.5 Serial Host Interface (SHI)

The SHI module is a serial I/O interface that provides a path for communication and program/coefficient data transfers between each DSP core and an external host processor. The SHI can also communicate with other serial peripheral devices.

SHI supports two well-known and widely used synchronous serial buses: Serial Peripheral Interface (SPI) bus, and Inter-Integrated-circuit Control (I²C) bus. The SHI supports either SPI or I²C bus protocol as required from a slave or a single-master device.

To minimize DSP core overhead, the SHI supports 8-bit, 16-bit, and 24-bit data transfers. The SHI has a 10-word receive FIFO that permits receiving up to 30 bytes before generating a receive interrupt, thereby reducing the overhead for data reception.

2.2.6 Host Interface (HDI24)

The HDI24 modules are byte-wide or 16-bit wide, full-duplex, double-buffered parallel ports that can connect directly to the data bus of a host processor. When supporting byte-wide parallel ports, the HDI24 module is identical to the HDI08.

Features

The HDI24 supports a variety of buses and provides connection switch a number of industry-standard DSPs, microcomputers, and microprocessors without requiring any additional logic. Each DSP core treats the HDI24 as a memory-mapped peripheral, that occupies eight 24-bit words in data memory space. Each DSP core can also use HDI24 as a memory-mapped peripheral, using either standard polled or interrupt programming techniques. Separate double-buffered transmit and receive data registers allow the DSP core and host processor to transfer data efficiently at high speed. Memory mapping allows you to program DSP core communication using HDI24 registers with standard instructions and addressing modes.

Note: 16-bit bond-out is available on the DSP56721 144LQFP package only. Future DSP5672x family derivatives may support 24-bits (HDI24).

2.2.7 Triple Timer Module (TEC)

The timers within the internal triple timer module act like timed pulse generators or like pulse-width modulators. These timers can also function as event counters, to capture an event or to measure the width or period of a signal.

The Triple Timer module is composed of a common 21-bit prescaler and three independent and identical general purpose 24-bit timer/event counters, with each counter having its own register set. A timer can use internal or external clocking, and can interrupt the DSP core after a specified number of events (clocks). Each of the three timers can signal an external device after counting internal events. A timer can also be used to trigger DMA transfers after a specified number of events (clocks) occurred.

When a timer pin is configured as an input, the timer works as an external event counter or can measure the external pulse width/signal period. When a timer pin is used as an output, the timer works as either a timer, a watchdog, or a pulse width modulator. When a timer pin is not used by a timer, it can be used as a General Purpose Input/Output (GPIO) pin.

2.2.8 Watchdog Timer (WDT)

The Watchdog timer is a 16-bit timer that can help software recover from a runaway code condition. The timer is a free-running down-counter used to generate a reset (by asserting the WDT pin) on underflow. Software must periodically service the watchdog timer in order to restart the countdown and prevent assertion of the WDT pin.

2.2.9 GPIO

The DSP56721 device provides up to 79 bidirectional signals that can be configured as GPIO function signals, or as peripheral function signals. Most of these signals are GPIO by default after resets.

2.2.10 Core Integration Module (CIM)

The CIM includes a chip ID register, a OnCE GDB register, and a DMA stall monitor function. When enabled, the DMA stall monitor can assert a non-maskable interrupt to the DSP core when the DMA has been stalled for longer than a configurable number of cycles due to internal memory contention.

2.2.11 JTAG/OnCE Module

Each DSP core contains its own independent JTAG/OnCE module, which can obtain the working status and data for each DSP core. This is helpful for software or hardware debugging. Note that there is only a single set of JTAG/OnCE output signals on the DSP56721 device.

2.3 Shared Modules

The following sections describes the peripheral modules that are shared between the two DSP56721 cores.

2.3.1 Shared Memory

The DSP56721 shared memory space can be accessed by either DSP Core-0 or DSP Core-1. Shared memory has eight 8K x 24-bit word memory blocks, resulting in a total of 64K shared words (located at \$030000). Shared memory can be accessed as X, Y or P memory. The 8K x 24-bit word blocks are single port SRAMs, with arbiters to perform arbitration when two DSP cores try to simultaneously access the same 8K x 24-bit word SRAM block. However, no shared memory contentions occur when the two DSP cores simultaneously access *different* 8K x 24-bit word SRAM blocks.

2.3.2 Inter-Core Communication (ICC) Module

Using the Inter-Core Communication module (ICC), each DSP core can issue maskable or non-maskable interrupts to the other DSP core. Each DSP core has its own write data register, which passes data to the other DSP core when an interrupt is generated. There are also poll data registers for inter-core data exchanges in the ICC. The ICC module interfaces with the dedicated peripheral buses of both DSP cores.

2.3.3 Shared Bus Arbiter

As shown in Figure 1, the following modules are shared by the two DSP cores: SPDIF, ASRC and Chip Configuration modules and Shared Memory. Each DSP core can access these shared modules without contention as long as neither DMA nor the other core is accessing the same shared blocks. An Arbiter determines the core access delays when contention occurs. The arbitration method can be chosen using the chip configuration registers. The following arbitration methods are supported:

- Always Round-Robin
- Core-0 always has high priority
- Core-1 always has high priority

2.3.4 Sony/Phillips Digital Interface (S/PDIF) Module

The S/PDIF audio module is a stereo transceiver that allows the DSP56721 to receive and transmit digital audio. The DSP56721 provides a single S/PDIF receiver, with 4 multiplexed inputs and one S/PDIF transmitter with two outputs. The S/PDIF module can also transmit and receive S/PDIF channel status (CS) and user (U) data. Note that there is only one S/PDIF module in the DSP56721 device, and it is shared by the two DSP cores.

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An internal Digital Phase-Locked Loop (DPLL) derives the receiving clock from the bi-phase incoming audio-data; the transmitting clock can be derived from an external source or the main oscillator. A frequency measurement circuit is included to allow precise measurement of the receiving clock or the transmitting clock.

2.3.5 Asynchronous Sample Rate Converter (ASRC)

The incoming audio data to the DSP56721 can come from various sources at different sampling rates. Additionally, the outgoing audio data from the DSP56721 may have different sampling rates and it can also be associated with output clocks that are asynchronous to the input clocks.

The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated with an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversions of up to 10 channels, at -120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs. Note that there is only one ASRC module in the DSP56721 device, and the ASRC is shared by the two DSP cores. The three sample rate convert pairs can be used by both DSP cores at same time.

The ASRC is hard-coded and acts like a co-processor, with minimal CPU or DSP core intervention.

2.3.6 Clock Generation Module (CGM)

The CGM is responsible for generating all clocks in the DSP56721. In functional mode, the output is a series of gated clocks. CGM has a low-jitter PLL inside. The PLL has a wide range of frequency multiplications (1 to 256), predivider factors (1 to 32) and output dividers (1 to 8). The CGM also has a power-saving clock divider (2^i : $i=0$ to 7). In functional mode, the PLL control register (PCTL) sits on the bus; both DSP cores can read and write these registers to change the chip's working frequency. Furthermore, each DSP core can independently enter stop or wait states to save power. Note that the shared peripherals enter power-saving mode only when both DSP cores enter stop mode.

3 Document Revision History

Table 3 provides a revision history for this document.

Table 3. DSP56721PB Document Revision History

Revision	Substantive Change(s)
1	Updated HDI24 section.

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