DS2751
Multichemistry Battery Fuel Gauge

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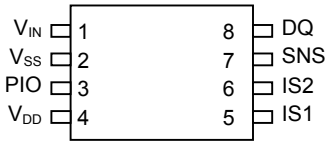
FEATURES

- Available in Two Configurations
  - Internal 25mΩ Sense Resistor
  - External User-Selectable Sense Resistor
- Current Measurement
  - 12-Bit Bidirectional Measurement
  - Internal Sense Resistor Configuration: 0.625mA LSB and ±1.9A Dynamic Range
  - External Sense Resistor Configuration: 15.625µV LSB and ±64mV Dynamic Range
- Current Accumulation
  - Internal Sense Resistor: 0.25mAhr LSB
  - External Sense Resistor: 6.25µVhr LSB
- Voltage Measurement with 4.88mV Resolution
- Temperature Measurement Using Integrated Sensor with 0.125°C Resolution
- 32 Bytes of Lockable EEPROM
- 16 Bytes of General-Purpose SRAM
- Dallas 1-Wire® Interface with Unique 64-Bit Device Address
- Supports 1-Cell Li+/Polymer or 3-Cell Ni Battery Packs
- 3mm Dimension of 8-Pin TSSOP Package Allows Mounting on Side of Thin Li+ and Li+/Polymer Cells
- Low Power Consumption:
  - Active Current: 60µA (typ), 90µA (max)
  - Sleep Current: 1µA (typ), 2µA (max)

PIN CONFIGURATION



DS2751E
8-Pin TSSOP Package

PIN DESCRIPTION

V_{IN}	Voltage-Sense Input
V_{SS}	Device Ground
PIO	Programmable I/O Pin
V_{DD}	Power-Supply Input (2.5V to 5.5V)
IS1	Current-Sense Input
IS2	Current-Sense Input
SNS	Sense Resistor Connection
DQ	Data Input/Output

ORDERING INFORMATION

PART	MARKING	TEMP RANGE	DESCRIPTION
DS2751E	2751E	-20°C to +70°C	8-Pin TSSOP, External Sense Resistor
DS2751E-025	2751R	-20°C to +70°C	8-Pin TSSOP, 25mΩ Sense Resistor
DS2751E/T&R	2751E	-20°C to +70°C	DS2751E on Tape-and-Reel
DS2751E-025/T&R	2751R	-20°C to +70°C	DS2751E-025 on Tape-and-Reel

DESCRIPTION

The DS2751 multichemistry battery fuel gauge is a data-acquisition and information-storage device tailored for cost-sensitive and space-constrained 1-cell Li+/polymer or 3-cell Ni battery-pack applications. The DS2751 provides the key hardware components required to accurately estimate remaining capacity by integrating low-power, precision measurements of temperature, voltage, current, and current accumulation, as well as nonvolatile (NV) data storage, into the small footprint of a 3.0mm x 4.4mm 8-pin TSSOP package.

Through its 1-Wire interface, the DS2751 gives the host system read/write access to status and control registers, instrumentation registers, and general-purpose data storage. Each device has a unique factory-programmed 64-bit net address that allows it to be individually addressed by the host system, supporting multibattery operation.

The DS2751 performs temperature, voltage, and current measurement to a resolution sufficient to support process-monitoring applications such as battery charge control and remaining capacity estimation. Temperature is measured using an on-chip sensor, eliminating the need for a separate thermistor. Bidirectional current measurement and accumulation are accomplished using either an internal 25mΩ sense resistor or an external device. The DS2751 also features a programmable I/O pin that allows the host system to sense and control other electronics in the pack, including switches, vibration motors, speakers, and LEDs.

Three types of memory are provided on the DS2751 for battery information storage: EEPROM, lockable EEPROM, and SRAM. EEPROM memory saves important battery data in true NV memory that is unaffected by severe battery depletion, accidental shorts, or ESD events. Lockable EEPROM becomes ROM when locked to provide additional security for unchanging battery data. SRAM provides inexpensive storage for temporary data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on PIO Pin, Relative to V_{SS}	-0.3V to +12V
Voltage on All Other Pins, Relative to V_{SS}	-0.3V to +6V
Continuous Internal Sense Resistor Current	±2.5A
Pulsed Internal Sense Resistor Current	±50A for <100µs/s, <1000 Pulses
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* *This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 2.5V ≤ V_{DD} ≤ 5.5V, -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	2.5		5.5	V
Data Pin	DQ	(Note 1)	-0.3		+5.5	V
V_{IN} Pin	V_{IN}	V_{DD} ≥ 4.2V (Notes 1, 2)	-0.3		+4.5	V
		2.5V < V_{DD} < 4.2V (Notes 1, 2)			V_{DD} + 0.3	V

DC ELECTRICAL CHARACTERISTICS

(T_A = 2.5V ≤ V_{DD} ≤ 5.5V, -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Current	I_{ACTIVE}	DQ = V_{DD}, normal operation		60	90	µA
Sleep-Mode Current	I_{SLEEP}	DQ = 0V, no activity		1	2	µA
Input Logic High: DQ, PIO	V_{IH}	(Note 1)	1.5			V
Input Logic Low: DQ, PIO	V_{IL}	(Note 1)			0.4	V
Output Logic Low: DQ, PIO	V_{OL}	I_{OL} = 4mA (Note 1)			0.4	V
DQ Pulldown Current	I_{PD}			1		µA
Input Resistance: V_{IN}	R_{IN}		5			MΩ
Internal Current-Sense Resistor	R_{SNS}	+25°C	20	25	30	mΩ
DQ Low-to-Sleep Time	t_{SLEEP}		2.2			s
Undervoltage Detect	V_{UV}	(Note 1)	2.5	2.6	2.7	V
Undervoltage Delay	T_{UVD}		90	100	110	ms

ELECTRICAL CHARACTERISTICS: TEMPERATURE, VOLTAGE, CURRENT

(T_A = 2.5V ≤ V_{DD} ≤ 5.5V, -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Resolution	T_{LSB}			0.125		°C
Temperature Full-Scale Magnitude	T_{FS}		127			°C
Temperature Error	T_{ERR}	(Note 3)			±3	°C
Voltage Resolution	V_{LSB}			4.88		mV
Voltage Full-Scale Magnitude	V_{FS}	(Note 4)	4.5			V
Voltage Offset Error	V_{OERR}	(Note 5)			1	LSB
Voltage Gain Error	V_{GERR}				3	%V reading
Current Resolution	I_{LSB}	(Note 6)		0.625		mA
		(Note 7)		15.625		µV
Current Full-Scale Magnitude	I_{FS}	(Notes 6, 7)	1.9	2.56		A
		(Note 8)		64		mV
Current Offset Error	I_{OERR}	(Note 9)			1	LSB
Current Gain Error	I_{GERR}	(Notes 6, 10)			3	%I reading
		(Note 7)			1	
Accumulated Current Resolution	q_{CA}	(Note 6)		0.25		mAhr
		(Note 7)		6.25		µVhr
Current Sampling Frequency	f_{SAMP}			1456		Hz
Internal Timebase Accuracy	t_{ERR}	0°C to +50°C (Note 11)		±1	±3	%
		-20°C to +70°C			±5	

ELECTRICAL CHARACTERISTICS—1-WIRE INTERFACE

(T_A = 2.5V ≤ V_{DD} ≤ 5.5V, -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Slot	t_{SLOT}		60		120	µs
Recovery Time	t_{REC}		1			µs
Write 0 Low Time	t_{LOW0}		60		119	µs
Write 1 Low Time	t_{LOW1}		1		15	µs
Read Data Valid	t_{RDV}				15	µs
Reset Time High	t_{RSTH}		480			µs
Reset Time Low	t_{RSTL}		480		960	µs
Presence-Detect High	t_{PDH}		15		60	µs
Presence-Detect Low	t_{PDL}		60		240	µs
DQ Capacitance	C_{DQ}				60	pF

EEPROM RELIABILITY SPECIFICATION

(T_A = 2.5V ≤ V_{DD} ≤ 5.5V, -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Copy to EEPROM Time	t_{EEC}			2	10	ms
EEPROM Copy Endurance	N_{EEC}	(Note 12)	25,000			cycles

Note 1: All voltages are referenced to V_{SS}.

Note 2: Operating V_{IN} > 4.5V relative to V_{SS}, or V_{IN} > V_{DD} + 0.3V can induce errors in voltage, temperature, or current measurements.

Note 3: Self heating due to output pin loading and sense resistor power dissipation can alter the reading from ambient conditions.

Note 4: Although the Voltage Register is large enough to report values larger than 4.75V, the internal compensation for circuit variations can reduce the maximum reportable voltage to as low as 4.75V.

Note 5: Voltage offset measurement is with respect to 4.35V at +25°C.

Note 6: Internal current-sense resistor configuration.

Note 7: External current-sense resistor configuration.

Note 8: The Current Register supports measurement magnitudes up to 2.56A using the internal sense-resistor option and 64mV with the external resistor option. Compensation of the internal sense-resistor value for process and temperature variation may reduce the maximum reportable magnitude to 1.9A.

Note 9: Current offset error null to ±1 LSb typically requires a one time 3.5s in-system calibration by user.

Note 10: Current gain-error specification applies to gain error in converting the voltage difference at IS1 and IS2, and excludes any error remaining after the DS2751 compensates for the internal sense-resistor's temperature coefficient of 3700ppm/°C to an accuracy of ±500ppm/°C. The DS2751 does not compensate for external sense resistor characteristics, and any error terms arising from the use of an external sense resistor should be taken into account when calculating total current measurement error.

Note 11: Typical value for t_{ERR} valid at 3.6V and +25°C.

Note 12: Four year data retention at +70°C.

Figure 1. FUNCTIONAL DIAGRAM

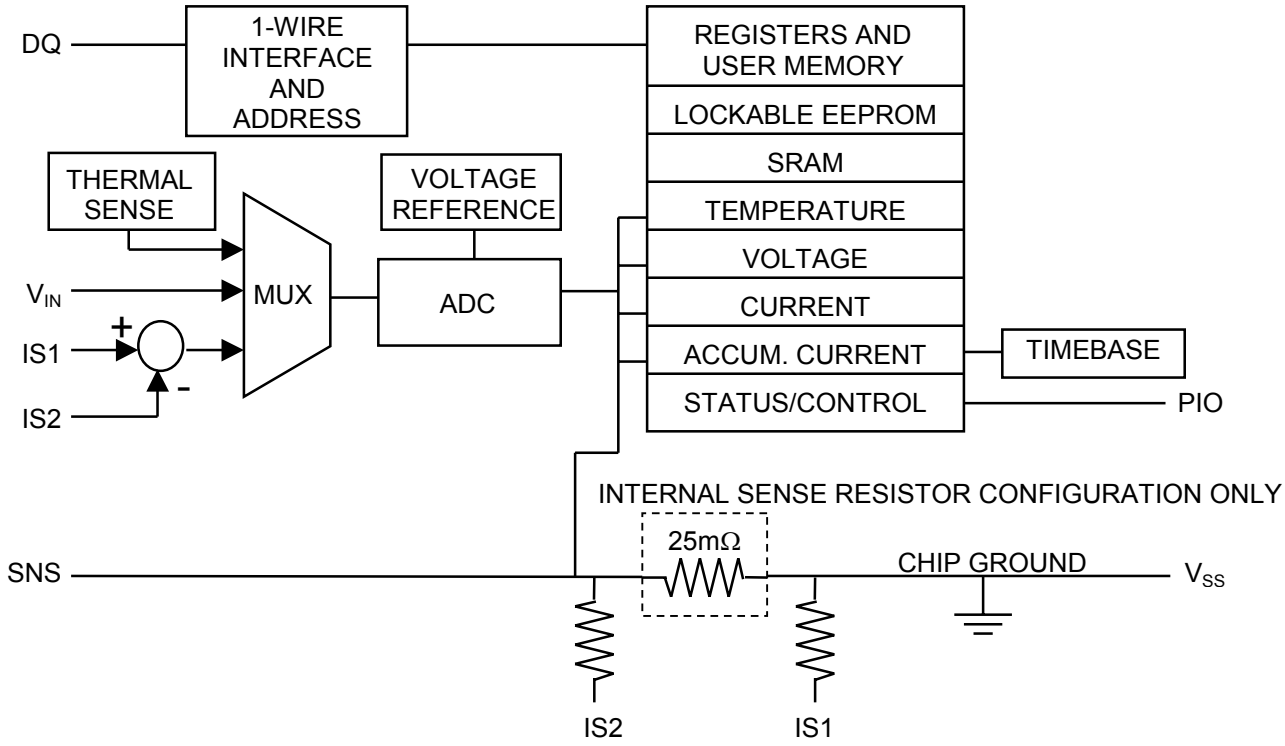
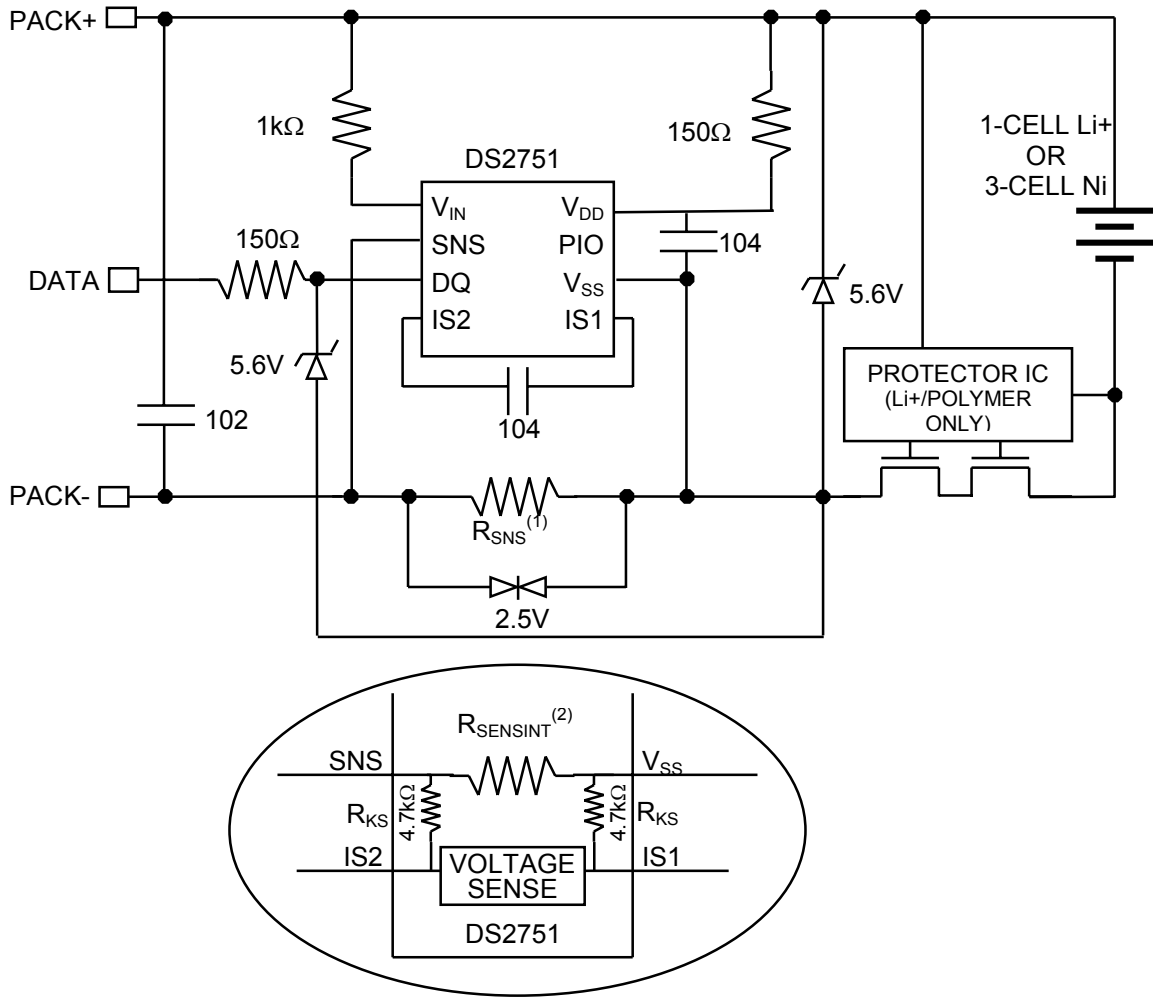


Figure 2. APPLICATION EXAMPLE



1) R_{SENS} is present for external sense resistor configurations only.
2) $R_{SENSINT}$ is present for internal sense resistor configurations only.

POWER MODES

The DS2751 has two power modes: active and sleep. While in active mode, the DS2751 continuously measures current, voltage, and temperature to provide data to the host system to support current accumulation. In sleep mode, the DS2751 ceases these activities. The DS2751 enters sleep mode when PMOD = 1 and either of the following occur:

- the DQ line is low for longer than t_{SLEEP} (2.2s) (pack disconnection).
- the UVEN bit in the Status Register is set to 1 and the voltage on V_{IN} drops below undervoltage threshold V_{UV} for t_{UVD} (cell depletion)

The DS2751 returns to active mode when the DQ line is pulled from a low-to-high state and the voltage on V_{IN} is above V_{UV}. The factory default for the DS2751 is UVEN = PMOD = 0.

The DS2751 defaults to active mode when power is first applied.

CURRENT MEASUREMENT

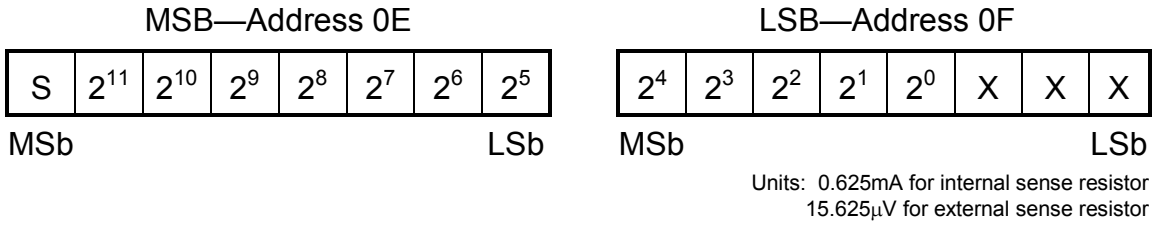
In the active mode of operation, the DS2751 continually measures the current flow into and out of the battery by measuring the voltage drop across a current-sense resistor. The DS2751 is available in two configurations: 1) internal 25mΩ current-sense resistor, and 2) external user-selectable sense resistor. In either configuration, the DS2751 considers the voltage difference between pins IS1 and IS2 ($V_{IS} = V_{IS1} - V_{IS2}$) to be the filtered voltage drop across the sense resistor. A positive V_{IS} value indicates current is flowing into the battery (charging), while a negative V_{IS} value indicates current is flowing out of the battery (discharging).

V_{IS} is measured with a signed resolution of 12 bits. The Current Register is updated in two's-complement format every 88ms with an average of 128 measurements. Currents outside the range of the register are reported at the limit of the range. The format of the Current Register is shown in Figure 3.

For the internal sense resistor configuration, the DS2751 maintains the Current Register in units of amps, with a resolution of 0.625mA and full-scale range of no less than ±1.9A (see Note 7 on I_{FS} spec for more details). The DS2751 automatically compensates for internal sense-resistor process variations and temperature effects when reporting current.

For the external sense resistor configuration, the DS2751 updates the measured V_{IS} voltage to the Current Register in units of volts, with a resolution of 15.625µV and a ±64mV full-scale range.

Figure 3. CURRENT REGISTER FORMAT



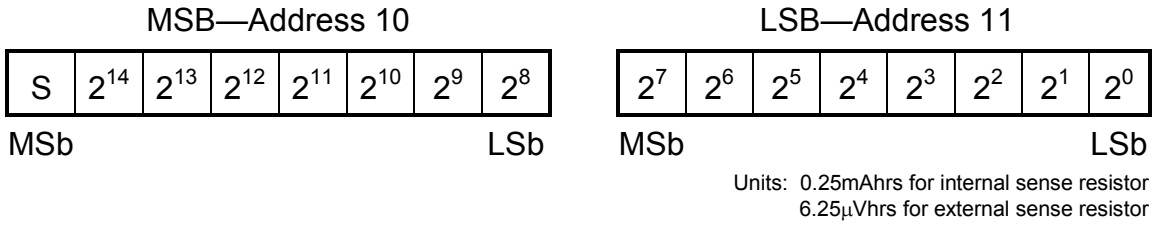
CURRENT ACCUMULATOR

The Current Accumulator facilitates remaining capacity estimation by tracking the net current flow into and out of the battery. Current flow into the battery increments the Current Accumulator, while current flow out of the battery decrements it. Data is maintained in the Current Accumulator in two's-complement format. The format of the Current Accumulator is shown in Figure 4.

When the internal sense resistor is used, the DS2751 maintains the Current Accumulator in units of amp-hours, with a resolution of 0.25mAhrs and a ±8.2Ahrs full-scale range. When using an external sense resistor, the DS2751 maintains the Current Accumulator in units of volt-hours, with a resolution of 6.25µVhrs and a ±205mVhrs full-scale range.

The Current Accumulator is a read/write register that can be altered by the host system as needed.

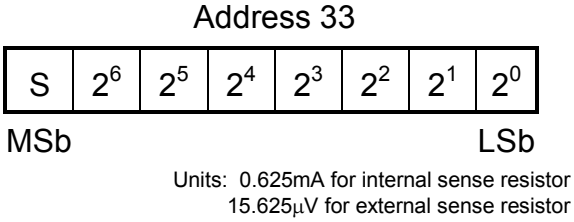
Figure 4. CURRENT ACCUMULATOR FORMAT



CURRENT OFFSET COMPENSATION

Current measurement and the current accumulation are both internally compensated for offset on a continual basis minimizing error resulting from variations in device temperature and voltage. Additionally, a constant bias can be utilized to alter any other sources of offset. This bias resides in EEPROM address 33h in two's-complement format and is subtracted from each current measurement. The current offset bias is applied to both the internal and external sense resistor configurations. The factory default for the current offset bias is a value of 0.

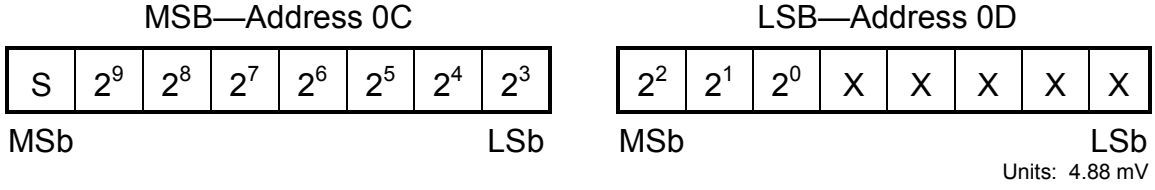
Figure 5. CURRENT OFFSET BIAS



VOLTAGE MEASUREMENT

The DS2751 continually measures the voltage between pins V_{IN} and V_{SS} over a 0 to 4.5V range. The Voltage Register is updated in two's-complement format every 3.4ms with a resolution of 4.88mV. Voltages above the maximum register value are reported as the maximum value. The Voltage Register format is shown in Figure 6.

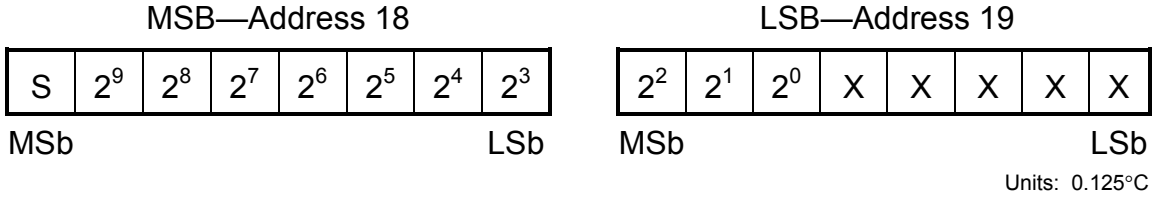
Figure 6. VOLTAGE REGISTER FORMAT



TEMPERATURE MEASUREMENT

The DS2751 uses an integrated temperature sensor to continually measure battery temperature. Temperature measurements are updated in the Temperature Register every 220ms in two's-complement format with a resolution of 0.125°C over a ±127°C range. The Temperature Register format is shown in Figure 7.

Figure 7. TEMPERATURE REGISTER FORMAT



PROGRAMMABLE I/O

To use the PIO pin as an output, write the desired output value to the PIO bit in the Special Feature Register. Writing a 0 to the PIO bit enables the PIO output driver, pulling the PIO pin to V_{SS}. Writing a 1 to the PIO bit disables the output driver, allowing the PIO pin to be pulled high or used as an input. To sense the value on the PIO pin, read the PIO bit. The DS2751 turns off the PIO output driver and sets the PIO bit high when in sleep mode or when DQ is low for more than t_{SLEEP} (2.2s), regardless of the state of the PMOD bit.

MEMORY

The DS2751 has a 256-byte linear address space with registers for instrumentation, status, and control in the lower 32 bytes, with lockable EEPROM and SRAM memory occupying portions of the remaining address space. All EEPROM and SRAM memory is general-purpose except addresses 31h and 33h, which should be written with the default values for the Status Register and Current Offset Register, respectively. When the MSB of any two-byte register is read, both the MSB and LSB are latched and held for the duration of the Read Data command to prevent updates during the read and to ensure synchronization between the two register bytes. For consistent results, always read the MSB and the LSB of a two-byte register during the same Read Data command sequence.

EEPROM memory is shadowed by RAM to eliminate programming delays between writes and to allow the data to be verified by the host system before being copied to EEPROM. All reads and writes to/from EEPROM memory actually access the shadow RAM. In unlocked EEPROM blocks, the Write Data command updates shadow RAM. In locked EEPROM blocks, the Write Data command is ignored. The Copy Data command copies the contents of shadow RAM to EEPROM in an unlocked block of EEPROM but has no effect on locked blocks. The Recall Data command copies the contents of a block of EEPROM to shadow RAM regardless of whether the block is locked or not.

Table 3. MEMORY MAP

ADDRESS (HEX)	DESCRIPTION	READ/WRITE
00	Reserved	
01	Status Register	R
02 to 06	Reserved	
07	EEPROM Register	R/W
08	Special Feature Register	R/W
09 to 0B	Reserved	
0C	Voltage Register MSB	R
0D	Voltage Register LSB	R
0E	Current Register MSB	R
0F	Current Register LSB	R
10	Accumulated Current Register MSB	R/W
11	Accumulated Current Register LSB	R/W
12 to 17	Reserved	
18	Temperature Register MSB	R
19	Temperature Register LSB	R
1A to 1F	Reserved	
20 to 2F	EEPROM, block 0	R/W*
30 to 3F	EEPROM, block 1	R/W*
40 to 7F	Reserved	
80 to 8F	SRAM	R/W
90 to FF	Reserved	

**Each EEPROM block is read/write until locked by the LOCK command, after which it is read-only.*

STATUS REGISTER

The default values for the Status Register bits are stored in lockable EEPROM in the corresponding bits of address 31h. A Recall Data command for EEPROM block 1 recalls the default values into the Status Register bits. The format of the Status Register is shown in Figure 8. The function of each bit is described in detail in the following paragraphs.

Figure 8. STATUS REGISTER FORMAT

Address 01

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	PMOD	RNAOP	UVEN	X	X	X

PMOD—Sleep Mode Enable. A value of 1 in this bit enables the DS2751 to enter sleep mode when the DQ line goes low for greater than t_{SLEEP}. A value of 0 disables the DS2751 from entering the sleep mode. This bit is read-only. The desired default value should be set in bit 5 of address 31h. The factory default is 0.

RNAOP—Read Net Address Opcode. A value of 0 in this bit sets the opcode for the Read Net Address command to 33h, while a 1 sets the opcode to 39h. This bit is read-only. The desired default value should be set in bit 4 of address 31h. The factory default is 0.

UVEN—Undervoltage Sleep Enable. A value of 1 in UVEN along with a value of 1 in PMOD enables the DS2751 to enter sleep mode when the voltage on V_{IN} drops below undervoltage threshold V_{UV} for t_{UVD} (cell depletion). A value of 0 disables the DS2751 from entering the sleep mode due to undervoltage events. This bit is read-only. The desired default value should be set in bit 3 of address 31h. The factory default is 0.

X—Reserved Bits.

EEPROM REGISTER

The format of the EEPROM Register is shown in Figure 9. The function of each bit is described in detail in the following paragraphs.

Figure 9. EEPROM REGISTER FORMAT

Address 07

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EEC	LOCK	X	X	X	X	BL1	BL0

EEC—EEPROM Copy Flag. A 1 in this read-only bit indicates that a Copy Data command is in progress. While this bit is high, writes to EEPROM addresses are ignored. A 0 in this bit indicates that data can be written to unlocked EEPROM blocks.

LOCK—EEPROM Lock Enable. When this bit is 0, the Lock command is ignored. Writing a 1 to this bit enables the Lock command. After the Lock command is executed, the LOCK bit is reset to 0. The factory default is 0.

BL1—EEPROM Block 1 Lock Flag. A 1 in this read-only bit indicates that EEPROM block 1 (addresses 30 to 3F) is locked (read-only), while a 0 indicates block 1 is unlocked (read/write).

BL0—EEPROM Block 0 Lock Flag. A 1 in this read-only bit indicates that EEPROM block 0 (addresses 20 to 2F) is locked (read-only), while a 0 indicates block 0 is unlocked (read/write).

X—Reserved Bits.

SPECIAL FEATURE REGISTER

The format of the Special Feature Register is shown in Figure 10. The function of each bit is described in detail in the following paragraphs.

Figure 10. SPECIAL FEATURE REGISTER FORMAT

Address 08

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
POR	PIO	X	X	X	X	X	X

POR—POR Indicator bit. This bit is set to a 1 when the DS2751 experiences a power-on-reset (POR) event. To use the POR bit to detect a power-on-reset, the POR bit must be set to a 0 by the host system upon power-up and after each subsequent occurrence of a POR.

PIO—PIO Pin Sense and Control. See the *Programmable I/O* section for details on this read/write bit.

X—Reserved Bits.

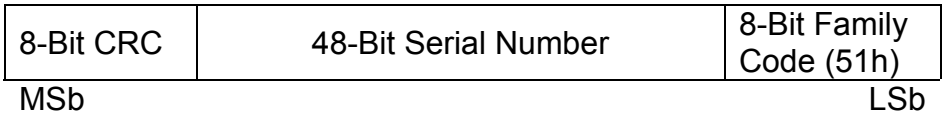
1-WIRE BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. A multidrop bus is a 1-Wire bus with multiple slaves. A single-drop bus has only one slave device. In all instances, the DS2751 is a slave device. The bus master is typically a microprocessor in the host system. The discussion of this bus system consists of four topics: 64-Bit Net Address, Hardware Configuration, Transaction Sequence, and 1-Wire Signaling.

64-BIT NET ADDRESS

Each DS2751 has a unique, factory-programmed 1-Wire net address that is 64 bits in length. The first 8 bits are the 1-Wire family code (51h for DS2751). The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits (see Figure 11). The 64-bit net address and the 1-Wire I/O circuitry built into the device enable the DS2751 to communicate through the 1-Wire protocol detailed in the 1-Wire Bus System section of this data sheet.

Figure 11. 1-WIRE NET ADDRESS FORMAT



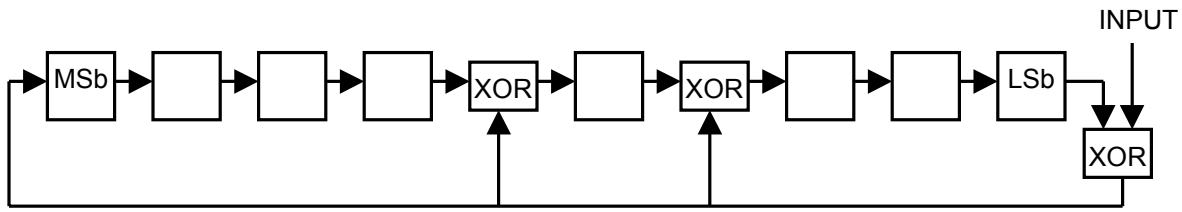
CRC GENERATION

The DS2751 has an 8-bit CRC stored in the most significant byte of its 1-Wire net address. To ensure error-free transmission of the address, the host system can compute a CRC value from the first 56 bits of the address and compare it to the CRC from the DS2751. The host system is responsible for verifying the CRC value and taking action as a result. The DS2751 does not compare CRC values and does not prevent a command sequence from proceeding as a result of a CRC mismatch. Proper use of the CRC can result in a communication channel with a very high level of integrity.

The CRC can be generated by the host using a circuit consisting of a Shift Register and XOR gates as shown in Figure 12, or it can be generated in software. Additional information about the Dallas 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products*.

In the circuit in Figure 12, the shift bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the Shift Register contains the CRC value.

Figure 12. 1-WIRE CRC GENERATION BLOCK DIAGRAM

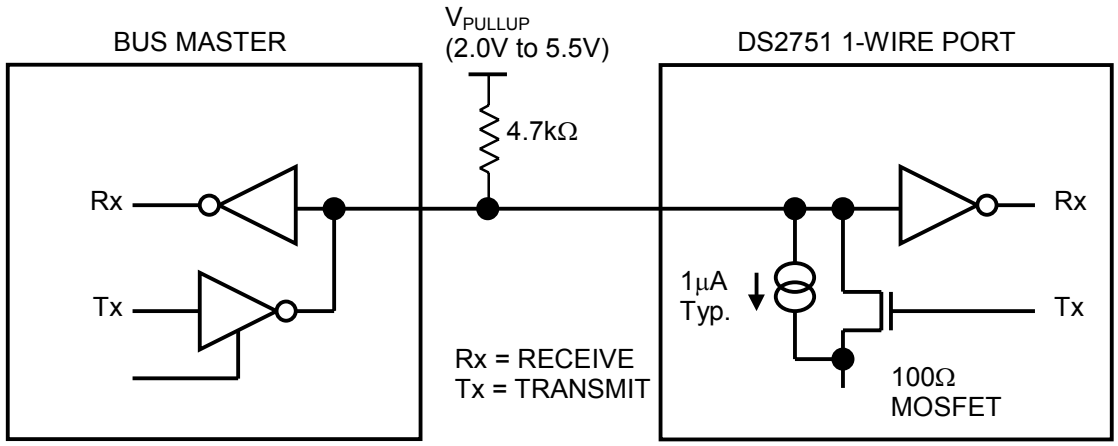


HARDWARE CONFIGURATION

Because the 1-Wire bus has only a single line, it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must connect to the bus with open-drain or tri-state output drivers. The DS2751 uses an open-drain output driver as part of the bidirectional interface circuitry shown in Figure 13. If a bidirectional pin is not available on the bus master, separate output, and input pins can be connected together.

The 1-Wire bus must have a pullup resistor at the bus-master end of the bus. For short line lengths, the value of this resistor should be approximately 5kΩ. The idle state for the 1-Wire bus is high. If, for any reason, a bus transaction must be suspended, the bus must be left in the idle state in order to properly resume the transaction later. If the bus is left low for more than 120μs, slave devices on the bus begin to interpret the low period as a reset pulse, effectively terminating the transaction.

Figure 13. 1-WIRE BUS INTERFACE CIRCUITRY



TRANSACTION SEQUENCE

The protocol for accessing the DS2751 through the 1-Wire port is as follows:

- Initialization
- Net Address Command
- Function Command
- Transaction/Data

The sections that follow describe each of these steps in detail.

All transactions of the 1-Wire bus begin with an initialization sequence consisting of a reset pulse transmitted by the bus master followed by a presence pulse simultaneously transmitted by the DS2751 and any other slaves on the bus. The presence pulse tells the bus master that one or more devices are on the bus and ready to operate. For more details, see the *I/O Signaling* section.

NET ADDRESS COMMANDS

Once the bus master has detected the presence of one or more slaves, it can issue one of the net address commands described in the following paragraphs. The name of each ROM command is followed by the 8-bit opcode for that command in square brackets. Figure 14 presents a transaction flowchart of the net address commands.

Read Net Address [33h or 39h]. This command allows the bus master to read the DS2751's 1-Wire net address. This command can only be used if there is a single slave on the bus. If more than one slave is present, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The RNAOP bit in the Status Register selects the opcode for this command, with RNAOP = 0 indicating 33h and RNAOP = 1 indicating 39h.

Match Net Address [55h]. This command allows the bus master to specifically address one DS2751 on the 1-Wire bus. Only the addressed DS2751 responds to any subsequent function command. All other slave devices ignore the function command and wait for a reset pulse. This command can be used with one or more slave devices on the bus.

Skip Net Address [CCh]. This command saves time when there is only one DS2751 on the bus by allowing the bus master to issue a function command without specifying the address of the slave. If more than one slave device is present on the bus, a subsequent function command can cause a data collision when all slaves transmit data at the same time.

Search Net Address [F0h]. This command allows the bus master to use a process of elimination to identify the 1-Wire net addresses of all slave devices on the bus. The search process involves the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple three-step routine on each bit location of the net address. After one complete pass through all 64 bits, the bus master knows the address of one device. The remaining devices can then be identified on additional iterations of the process. See Chapter 5 of the *Book of DS19xx iButton® Standards* for a comprehensive discussion of a net address search, including an actual example. This publication can be found on the Maxim/Dallas website at www.maxim-ic.com.

FUNCTION COMMANDS

After successfully completing one of the net address commands, the bus master can access the features of the DS2751 with any of the function commands described in the following paragraphs. The name of each function is followed by the 8-bit opcode for that command in square brackets.

Read Data [69h, XX]. This command reads data from the DS2751 starting at memory address XX. The LSb of the data in address XX is available to be read immediately after the MSb of the address has been entered. Because the address is automatically incremented after the MSb of each byte is received, the LSb of the data at address XX + 1 is available to be read immediately after the MSb of the data at address XX. If the bus master continues to read beyond address FFh, the DS2751 outputs logic 1 until a reset pulse occurs. Addresses labeled "reserved" in the memory map contain undefined data. The Read Data command can be terminated by the bus master with a reset pulse at any bit boundary.

Write Data [6Ch, XX]. This command writes data to the DS2751 starting at memory address XX. The LSb of the data to be stored at address XX can be written immediately after the MSb of the address has been entered. Because the address is automatically incremented after the MSb of each byte is written, the LSb to be stored at address XX + 1 can be written immediately after the MSb to be stored at address XX. If the bus master continues to write beyond address FFh, the DS2751 ignores the data. Writes to read-only addresses, reserved addresses and locked EEPROM blocks are ignored. Incomplete bytes are not written. Writes to unlocked EEPROM blocks are to shadow RAM rather than EEPROM. See the *Memory* section for more details.

Copy Data [48h, XX]. This command copies the contents of shadow RAM to EEPROM for the 16-byte EEPROM block containing address XX. Copy Data commands that address locked blocks are ignored. While the Copy Data command is executing, the EEC bit in the EEPROM Register is set to 1 and writes to EEPROM addresses are ignored. Reads and writes to non-EEPROM addresses can still occur while the copy is in progress. The Copy Data command execution time, t_{EEC}, is 2ms typical and starts after the last address bit is transmitted.

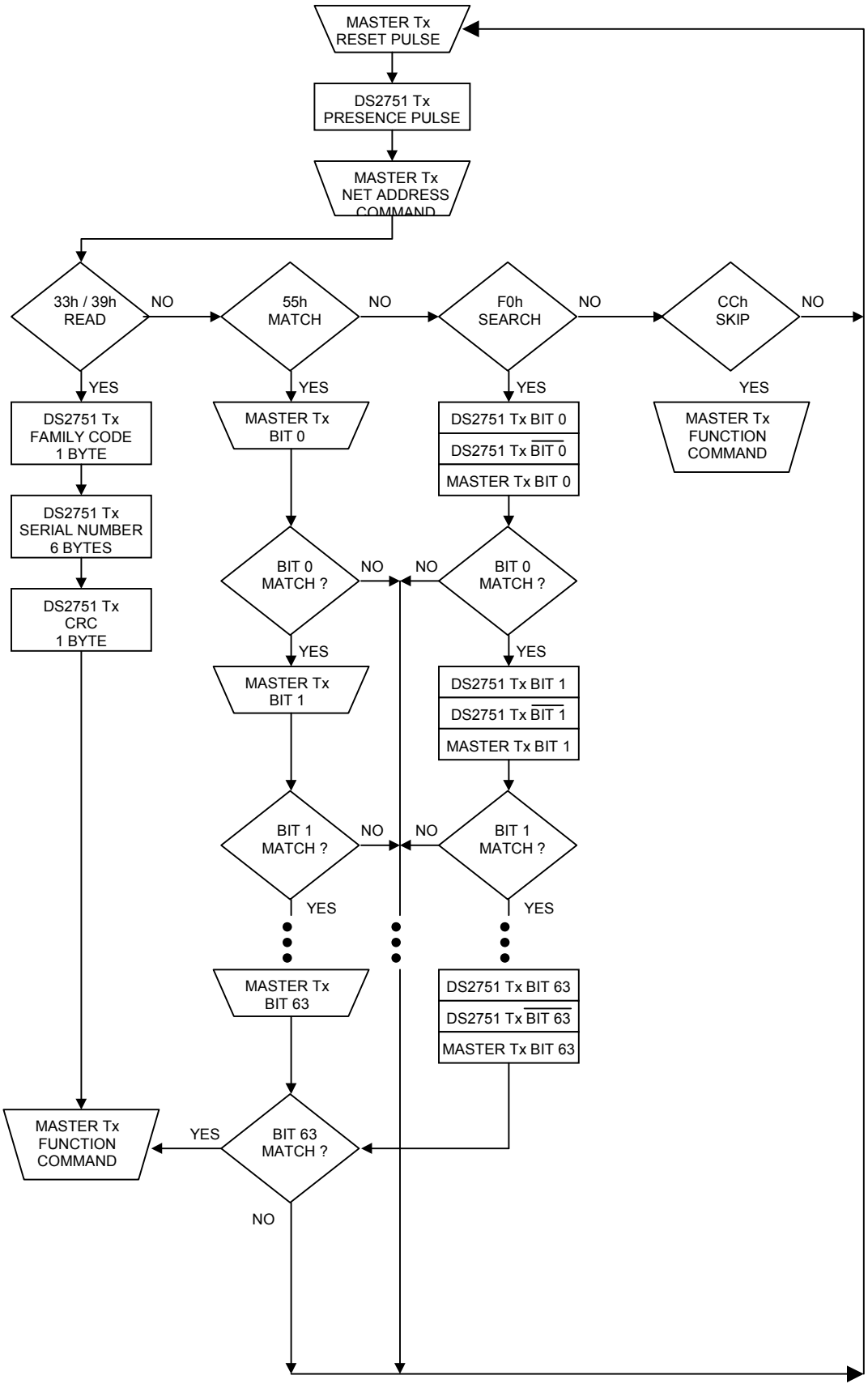
Recall Data [B8h, XX]. This command recalls the contents of the 16-byte EEPROM block containing address XX to shadow RAM.

Lock [6Ah, XX]. This command locks (write-protects) the 16-byte block of EEPROM memory containing memory address XX. The LOCK bit in the EEPROM Register must be set to l before the Lock command is executed. If the LOCK bit is 0, the Lock command has no effect. The Lock command is permanent; a locked block can never be written again.

Table 4. FUNCTION COMMANDS

COMMAND	DESCRIPTION	COMMAND PROTOCOL	BUS STATE AFTER COMMAND PROTOCOL	BUS DATA
Read Data	Reads data from memory starting at address XX	69h, XX	Master Rx	Up to 256 bytes of data
Write Data	Writes data to memory starting at address XX	6Ch, XX	Master Tx	Up to 256 bytes of data
Copy Data	Copies shadow RAM data to EEPROM block containing address XX	48h, XX	Bus idle	None
Recall Data	Recalls EEPROM block containing address XX to shadow RAM	B8h, XX	Bus idle	None
Lock	Permanently locks the block of EEPROM containing address XX	6Ah, XX	Bus idle	None

Figure 14. NET ADDRESS COMMAND FLOW CHART

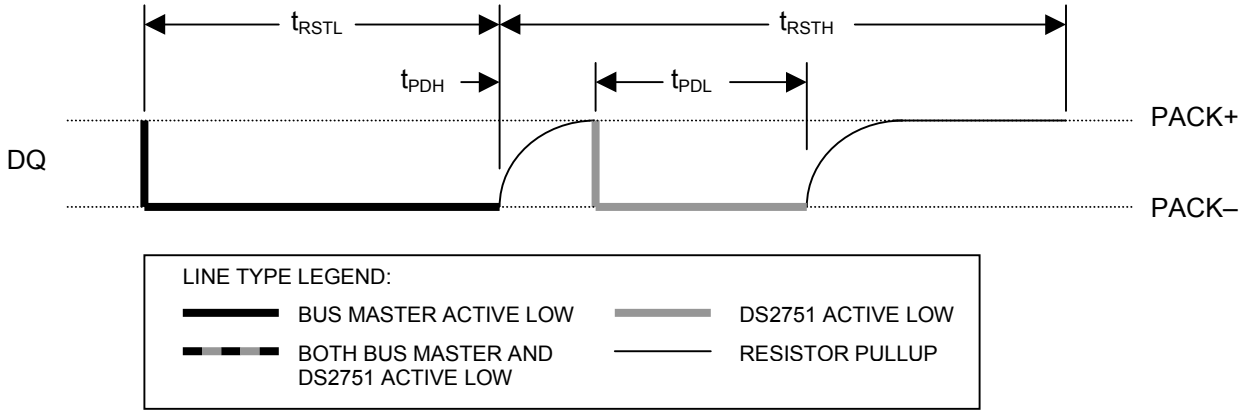


I/O SIGNALING

The 1-Wire bus requires strict signaling protocols to insure data integrity. The four protocols used by the DS2751 are: the initialization sequence (reset pulse followed by presence pulse), Write 0, Write 1, and Read Data. All of these types of signaling except the presence pulse are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2751 is shown in Figure 15. A presence pulse following a reset pulse indicates the DS2751 is ready to accept a net address command. The bus master transmits (Tx) a reset pulse for t_{RSTL}. The bus master then releases the line and goes into receive mode (Rx). The 1-Wire bus line is then pulled high by the pullup resistor. After detecting the rising edge on the DQ pin, the DS2751 waits for t_{PDH} and then transmits the Presence Pulse for t_{PDL}.

Figure 15. 1-WIRE INITIALIZATION SEQUENCE



WRITE TIME SLOTS

A write time slot is initiated when the bus master pulls the 1-Wire bus from a logic high (inactive) level to a logic low level. There are two types of write time slots: Write 1 and Write 0. All write time slots must be t_{SLOT} (60µs to 120µs) in duration with a 1µs minimum recovery time, t_{REC}, between cycles. The DS2751 samples the 1-Wire bus line between 15µs and 60µs after the line falls. If the line is high when sampled, a Write 1 occurs. If the line is low when sampled, a Write 0 occurs (see Figure 16). For the bus master to generate a Write 1 time slot, the bus line must be pulled low and then released, allowing the line to be pulled high within 15µs after the start of the write time slot. For the host to generate a Write 0 time slot, the bus line must be pulled low and held low for the duration of the write time slot.

READ TIME SLOTS

A read time slot is initiated when the bus master pulls the 1-Wire bus line from a logic high level to a logic low level. The bus master must keep the bus line low for at least 1µs and then release it to allow the DS2751 to present valid data. The bus master can then sample the data t_{RDV} (15µs) from the start of the read time slot. By the end of the read time slot, the DS2751 releases the bus line and allows it to be pulled high by the external pullup resistor. All read time slots must be t_{SLOT} (60µs to 120µs) in duration with a 1µs minimum recovery time, t_{REC}, between cycles. See Figure 16 for more information.

Figure 16. 1-WIRE WRITE AND READ TIME SLOTS