National Semiconductor

ADVANCE INFORMATION

DS26LV32A
3V Enhanced CMOS Quad Differential Line Receiver

General Description

The DS26LV32A is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and CCITT V.11. The CMOS DS26LV32A features low I_{CC} of X mA which makes it ideal for battery powered and power conscious applications.

The TRI-STATE® enables, EN and $\overline{EN}$, allow the device to be active High or active Low. The enables are common to all four receivers.

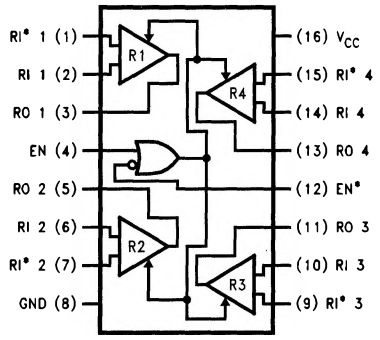
The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as ±200 mV over the common mode range of ±7V. The receiver outputs (RO) are compatible with TTL and CMOS levels.

Features

- Low power CMOS design
- Meets TIA/EIA-422-B (RS-422) and CCITT V.11 recommendation
- Receiver OPEN input failsafe feature
- Guaranteed AC parameter:
  - — Maximum receiver skew TBD
  - — Transition time TBD
- Pin compatible with DS26C32A
- Available in SOIC packaging

Connection Diagram

Dual-In-Line Package
DS26LV32A



TL/F/12643–1

Order Number DS26LV32AM or DS26LV32AN
See NS Package Number M16A or N16E

Truth Table

Enables		Inputs	Outputs
EN	**$\overline{EN}$**	**RI–RI***	**RO**
L	H	X	Z
H	L	$V_{ID} \geq V_{TH\ (Max)}$	H
H	H	$V_{ID} \leq V_{TH\ (Min)}$	L
L	L	Open	H

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)