National Semiconductor

PRELIMINARY

DS26C32C Quad Differential Line Receiver

General Description

The DS26C32 is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

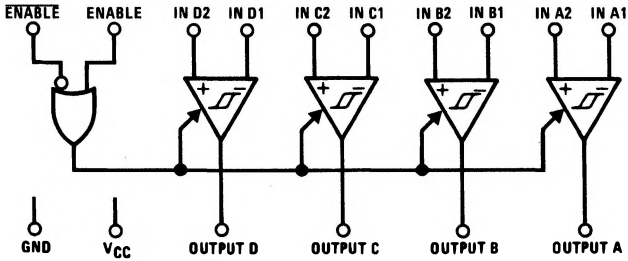
The DS26C32 has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Each receiver is also equipped with input fail-safe circuitry, which causes the output to go to a logic "1" state when the inputs are open.

The DS26C32 provides an enable and disable function common to all four receivers, and features TRI-STATE® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

- Low power CMOS design
- ±0.2V sensitivity over the entire common mode range
- Typical propagation delays: 20 ns
- Typical input hysteresis: 50 mV
- Input fail-safe circuitry
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses

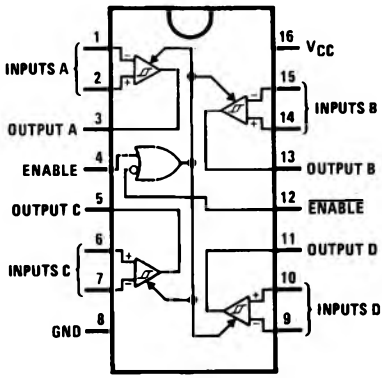
Logic Diagram



TL/F/8764–1

Connection Diagram

Dual-In-Line Package



TL/F/8764–2

Top View

Order Number DS26C32CJ, DS26C32CM, DS26C32CN, DS26C32MJ or DS26C32MN
See NS Package J16A, M16A or N16A

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0
		Open	1

Hi-Z = TRI-STATE

Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

For complete specifications see the Interface Databook.