DS1482

1-Wire Level Shifter and Line Driver with Load Sensor

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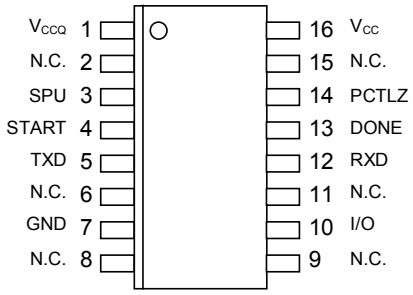
FEATURES

- Works with All iButtons® and 1-Wire® Devices
- Communicates at Regular and Overdrive 1-Wire Speed (Host-Dependent)
- Separate Interface Power Supply to Level Shift to Non-5V Systems
- External Strong-Pullup Control Pin can be Used to Provide Low-On-Resistance-High Current Power Source
- Load Sensor to Detect when Strong-Pullup Power Delivery is no Longer Needed
- Power Delivery DONE Signal can be Connected to Host Interrupt
- Low-Cost 16-Pin SO Surface-Mount Package
- Operating Temperature Range: -40°C to +85°C

PIN ASSIGNMENT



ORDERING INFORMATION

DS1482S	SO-16
DS1482S/T&R	SO-16, Tape-and-Reel

Contact the factory for versions with different signal polarities.

DESCRIPTION

The DS1482 is a simple 1-Wire line driver with load sensor and level shifter, designed to function as an interface between a 3V host system and a 1-Wire system that runs on 5V. Two supplies are provided, a 5V supply for the 1-Wire operations (V_{CC}) and an interface supply (V_{CCQ}). The DS1482 can connect directly to a synchronous serial port if it supports the appropriate bit rates to generate 1-Wire timing.

Figure 1 shows the DS1482 block diagram. TXD is buffered and controls an N-channel transistor, which drives the 1-Wire pin I/O low, e.g., to initiate a time slot. The logic level of the I/O pin is returned through a level-shifting buffer to the RXD pin for the host processor to read. Figure 3 shows the relationship of these signals in case of a 1-Wire read time slot.

The SPU input generates a control signal (PCTLZ) for an external low-impedance PMOS transistor (Figure 2) that bypasses the 1-Wire pullup resistor (R_{PUP}) to provide power for 1-Wire devices with a high-load current. PCTLZ is gated by the inverted TXD signal. This prevents a high through-current in case TXD and SPU are high at the same time.

The DS1482 contains a high-precision comparator because it is important for the host micro to know when the high load on the 1-Wire side is no longer active. As shown in Figure 4, the high current load causes a small drop of the voltage on the I/O pin. The comparator detects when the high current phase ends, and enables DONE after the deglitching time t_{CF} is over. The START signal allows the host micro to selectively enable DONE.

PIN	NAME	FUNCTION
1	V_{CCQ}	Operating voltage for all circuitry that connects to the controlling microprocessor (TXD, RXD, START, SPU, DONE pins).
3	SPU	This line is used to control the external strong pullup function. When SPU is low, the strong pullup (PCTLZ) is high. When SPU is high and TXD is low, PCTLZ is low.
4	START	This line acts as an enable control for the DONE pin. If START is high, then DONE reflects the filtered digital output of the current-sense comparator. If START is low, then DONE is low.
5	TXD	When TXD is low, the I/O pin is pulled resistively to V_{CC}. When TXD is high, the 1-Wire bus is pulled to GND (for write-0, write-1, read, and reset low times).
7	GND	Ground Reference for V_{CCQ}, V_{CC}, 1-Wire
10	I/O	1-Wire Data
12	RXD	This line returns the digital state of the 1-Wire bus, level-shifted to swing between V_{CCQ} and GND.
13	DONE	This line is high only when the buffered, filtered digital output from the current-sense comparator indicates that the downstream 1-Wire slave device is no longer sinking high current. This signal is enabled if START is high.
14	PCTLZ	Active-low control pin for an external low-on-resistance, high-current supply. This signal typically controls the gate of a P-channel MOSFET. This signal is low when SPU is high and TXD is low.
16	V_{CC}	Operating voltage for all circuitry that connects to the 1-Wire environment (I/O and PCTLZ pins).
2, 6, 8, 9, 11, 15	N.C.	Not Connected

Figure 1. Block Diagram

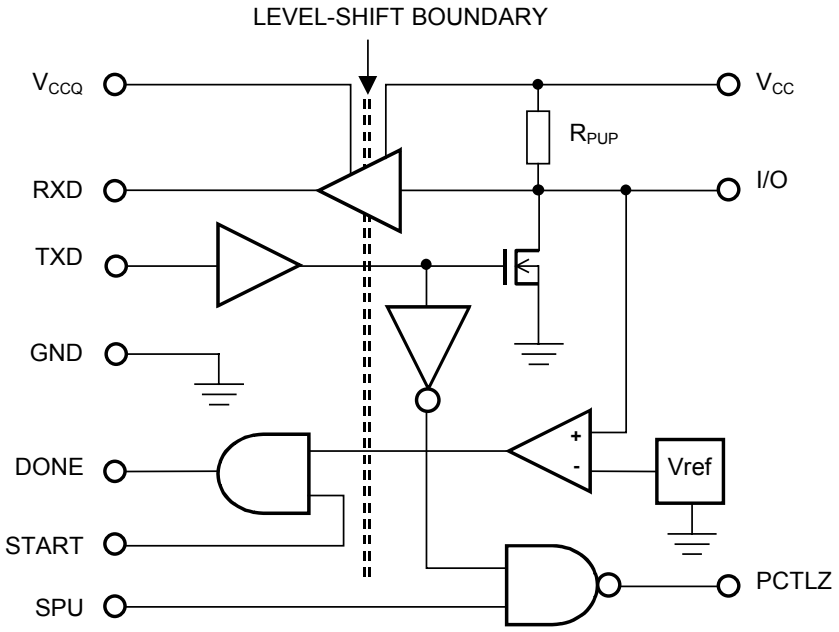
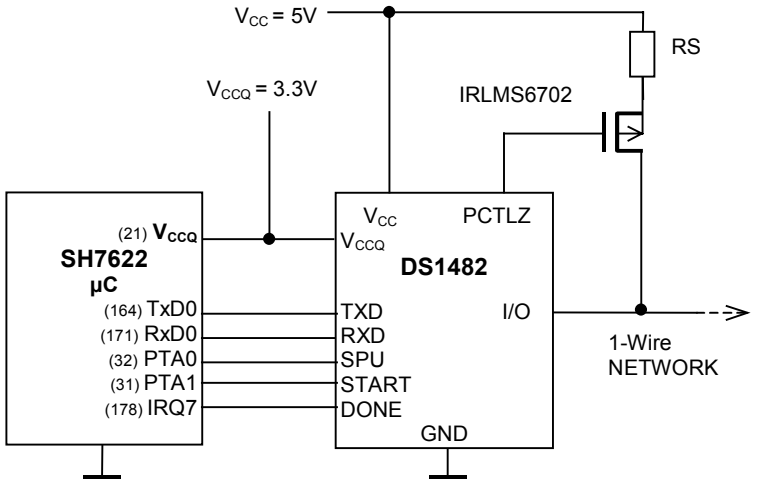


Figure 2. Typical Operating Circuit



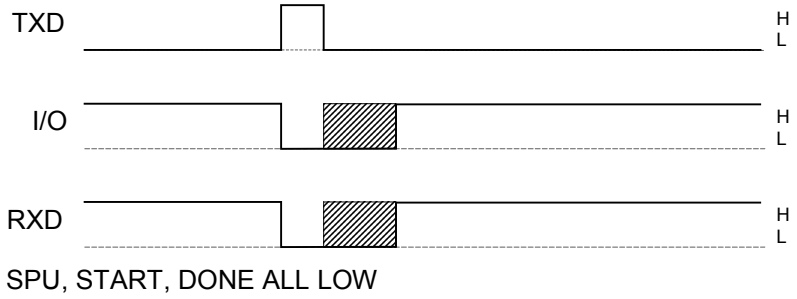
Selecting RS
Assuming that the series resistance of the FET in on-condition can be neglected, the value of RS is limited as follows:
RSmax = 0.0015 x VCCmin/I(standby,max)
RSmin = 0.01 x VCCmax/I(active,min)

Example:
VCCmin = 4.5V, VCCmax = 5.5V
I(standby,max) = 0.15mA
I(active,min) = 12mA

RSmax = 45Ω, RSmin = 4.58Ω

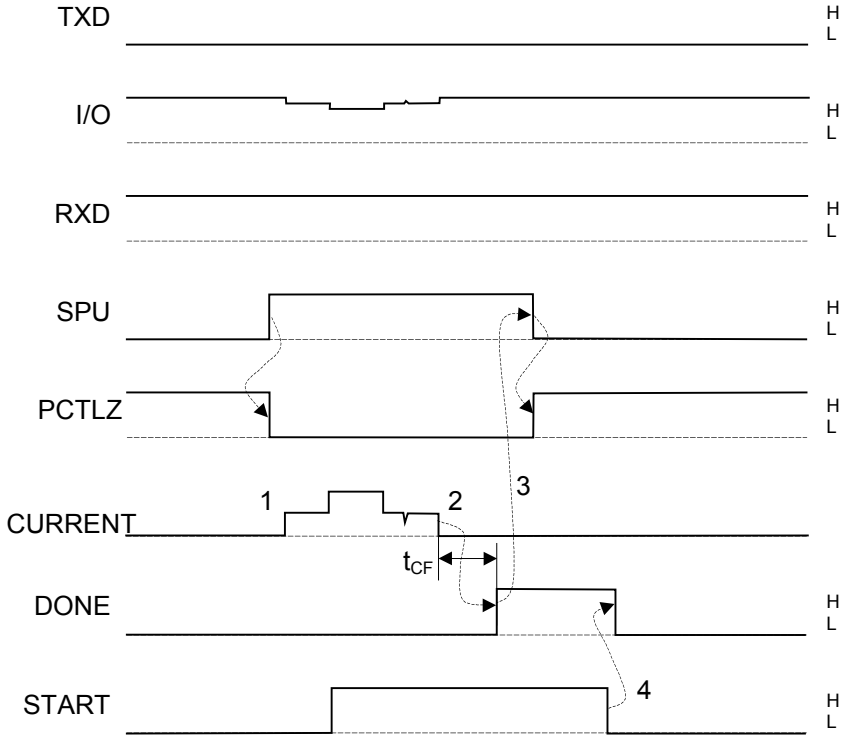
To maximize available power on the 1-Wire line, RS should be close to the lowest permissible value, in this example 5.1Ω ±5%. The effect of the on-chip pullup resistor is negligible.

Figure 3. DS1482 Application Signals, Normal Communication



SPU, START, DONE ALL LOW

Figure 4. DS1482 Application Signals, Strong Pullup Case



Point 1: The 1-Wire slave device starts drawing current (internal micro or numeric processor is running). The strong pullup (SPU) must be activated before the high current phase begins.

Point 2: The 1-Wire slave device no longer draws current. After the deglitching time (t_{CF}) is over, the DONE signal turns high. The START signal must be activated no later than t_{SD} before t_{CF} is over. Typically START is activated shortly after SPU, but not before the 1-Wire slave device has started drawing high current.

Point 3: As soon as the DONE signal is high, the host micro ends the strong pullup by changing SPU to low.

Point 4: While the DONE signal is high, the host micro changes START to low; this may occur simultaneously with the state change of SPU or later. When START changes to low, DONE becomes low.

Figure 5. Timing References TXD to I/O

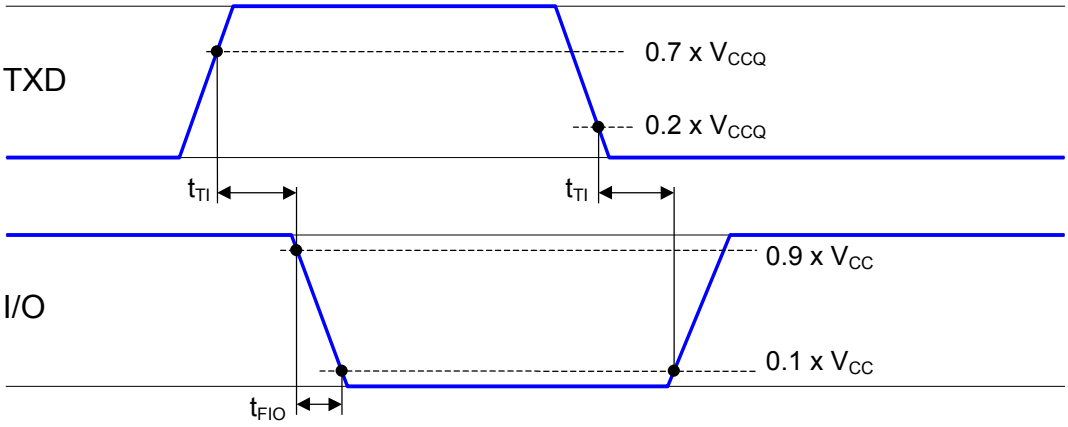


Figure 6. Timing References I/O to RXD

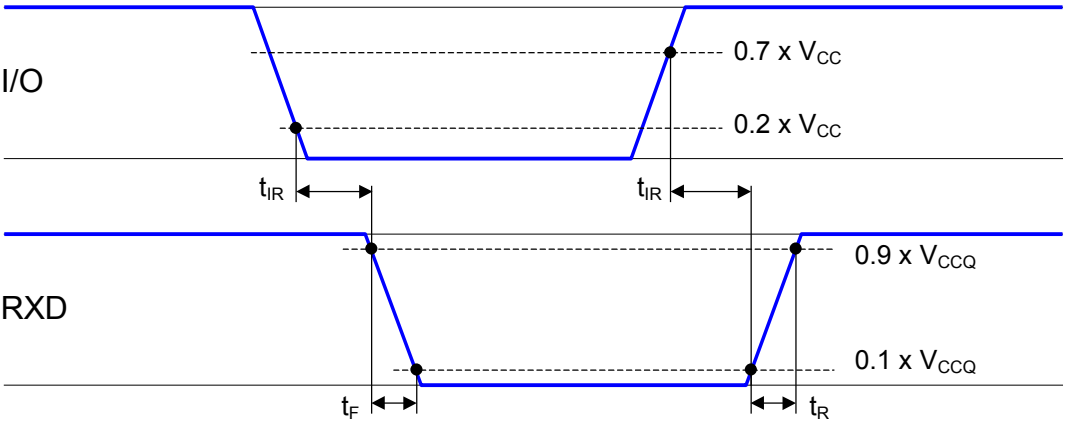


Figure 7. Timing References SPU to PCTLZ

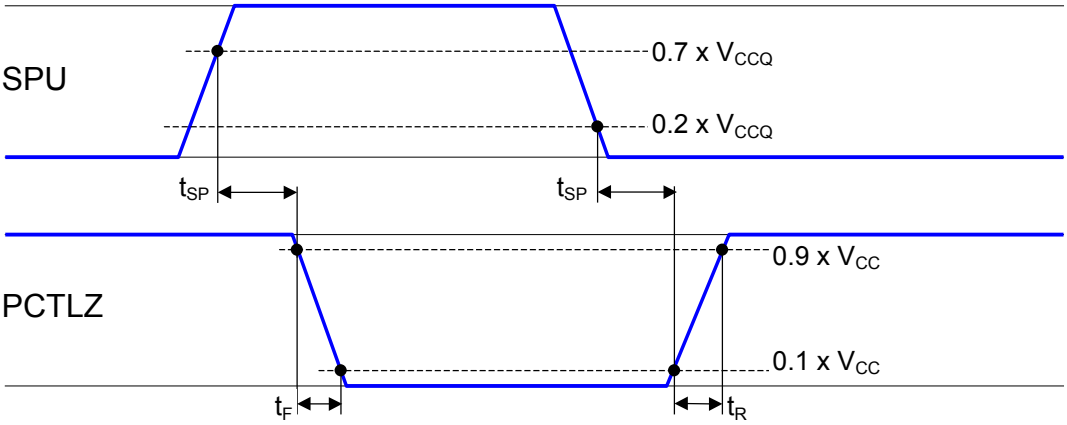
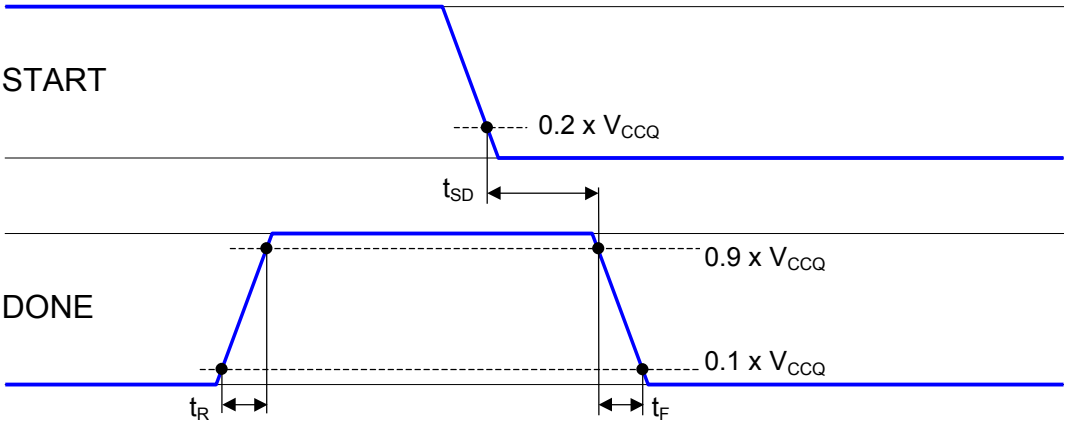


Figure 8. Timing References START to DONE



ABSOLUTE MAXIMUM RATINGS*

Voltage to GND (All Pins)	-0.5V, +6.0V
Combined Source/Sink Current (All Pins)	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (Soldering)	See IPC/JEDEC 020A

ESD requirements are 15kV for the I/O pin and 4kV for all other pins.

* *This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, V_{CCQ} = 3.0V to 3.6V; T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}				150	µA
Supply Current	I_{CCQ}				100	µA
Supply Ramp-up Time (System Requirement)	t_{RCC}	V_{CC}, V_{CCQ} rising from 0 to V_{CCMIN} and V_{CCQMIN}, respectively	0.1			µs
1-Wire Pullup Resistor	R_{PUP}		850		1650	Ω
INPUT PINS SPU, START, TXD						
Input High Voltage	V_{IH}		0.7 x V_{CCQ}			V
Input Low Voltage	V_{IL}				0.2 x V_{CCQ}	V
Input Leakage	I_{LP}	Measured with either 0V or V_{CCQ} on the pin (Note 1)			3	µA
Delay TXD to I/O	t_{TI}	No DC load on I/O; see Figure 5 (Note 2)			100	ns
I/O PIN (1-WIRE)						
Output Low Voltage	V_{OL}	100µA load			0.4	V
Output High Voltage	V_{OH}	No DC load		V_{CC}		V
Pin Leakage Current	I_{LP}	(Note 3)	-1		+1	µA
Input High Voltage	V_{IH}		0.7 x V_{CC}			V
Input Low Voltage	V_{IL}				0.2 x V_{CC}	V
Comparator Reference Voltage	V_{REF}		0.99 x V_{CC}	0.995 x V_{CC}	0.998 x V_{CC}	V
Output Fall Time (50pF Load)	t_{FIO}	0.9 x V_{CC} to 0.1 x V_{CC}	45		150	ns

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT PIN RXD						
Output-Low Voltage	V_{OL}	100µA load			0.4	V
Output-High Voltage	V_{OH}	-100µA load	V_{CCQ} - 0.5V			V
Output Rise Time (50pF Load)	t_R	0.1 x V_{CCQ} to 0.9 x V_{CCQ}			50	ns
Output Fall Time (50pF Load)	t_F	0.9 x V_{CCQ} to 0.1 x V_{CCQ}			50	ns
Delay I/O to RXD (50pF Load)	t_{IR}	See Figure 6 (Note 2)			100	ns
OUTPUT PIN PCTLZ						
Output-Low Voltage	V_{OL}	100µA load			0.4	V
Output-High Voltage	V_{OH}	-100µA load	V_{CC} - 0.5V			V
Output Rise Time (50pF Load)	t_R	0.1 x V_{CC} to 0.9 x V_{CC}			50	ns
Output Fall Time (50pF Load)	t_F	0.9 x V_{CC} to 0.1 x V_{CC}			50	ns
Delay SPU to PCTLZ (50pF Load)	t_{SP}	See Figure 7 (Note 4)			100	ns
OUTPUT PIN DONE						
Output-Low Voltage	V_{OL}	100µA load			0.4	V
Output-High Voltage	V_{OH}	-100µA load	V_{CCQ} - 0.5V			V
Output Rise Time (50pF Load)	t_R	0.1 x V_{CCQ} to 0.9 x V_{CCQ}			50	ns
Output Fall Time (50pF Load)	t_F	0.9 x V_{CCQ} to 0.1 x V_{CCQ}			50	ns
Delay I/O to DONE (50pF Load)	t_{CF}	START at V_{CCQ} (Note 5)	128		500	µs
Delay START to DONE (50pF Load)	t_{SD}	See Figure 8			100	ns

Note 1: The input pins have a weak pulldown.

Note 2: For OD read- or write-1 time slots, TXD should be pulsed high for 1.28µs. The window for sampling RXD begins 1.8µs after TXD has turned high and ends 2.05µs after TXD has turned high. RXD must be sampled inside this window. Correct sampling can be achieved with the particular recommended microcontroller Hitachi SH7622 if the peripheral module operating frequency PΦ is higher or equal to 22MHz.

Note 3: Measured either with V_{CC} on the pin and TXD low or with 0V on the pin and TXD high. This parameter is guaranteed by design, and is not production tested.

Note 4: The PCTLZ signal is gated by TXD. The PCTLZ output is only low if TXD is low.

Note 5: Characteristic of the glitch-eating filter on the output of the load-sensing comparator, i.e., an event where the downstream 1-Wire slave device is sinking high current, ceases sinking the current for less than this amount of time, and resumes sinking the current does not generate high level on DONE; DONE goes high this amount of time after the downstream 1-Wire slave device has ceased sinking high current.