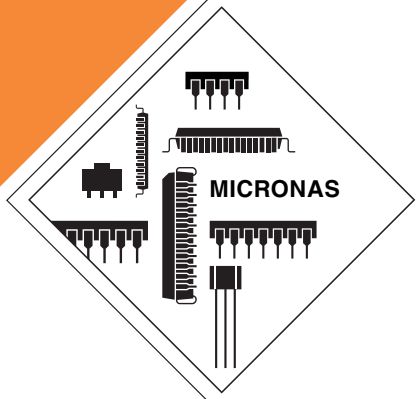


PRELIMINARY DATA SHEET

DPL 3520A, DPL 3519A, DPL 3518A Dolby Pro Logic Processor Family

Edition July 31, 1997
6251-423-1PD

MICRONAS

Contents

Contents, continued

DPL 3520A Dolby*) Pro Logic Processor

Note: This document contains information on a new product.
Specifications and information herein are subject to change without notice.

*) “Dolby”, the double-D symbol and “Pro Logic” are trademarks of Dolby Laboratories Licensing Corporation.

Dolby Pro Logic Processor Family

1. Introduction

The DPL 35xxA processor family is designed to decode Dolby encoded surround sound. The ICs integrate the complete Dolby Surround Pro Logic decoding on chip without any necessary external circuitry. This data sheet describes the features and specifications of all members of the IC family.

The DPL 3518A is designed as a coprocessor to one of the TV sound processing ICs of the MSP 34xx family. It only has digital interfaces. No analog input and output interfaces are supported.

The DPL 3519A is also designed as a coprocessor to the MSP family but has analog output channels in addition to the features of the DPL 3518A. Together with the MSP, a TV set with up to six outputs (L, R, C, SUB, S_L, S_R) can be developed together with headphones and several line outputs.

The DPL 3520A is designed as a stand-alone Dolby Surround Pro Logic decoder. An on-chip A/D converter digitizes analog inputs. The DPL 3520A can also be used as a coprocessor to the MSP 34xx single-chip Multistandard Sound Processor family. This gives another A/D input pair to the system.

The ICs of the DPL family are pin-compatible to the MSP ICs. This speeds up PCB development for customers using MSPs.

The software interface is largely the same as for the MSP 3400C. Volume, tone controls, matrixes and switches use the same registers and values. Thus, the standard MSP 3400C controlling software can be used to control the DPL 3520A. Little overhead is needed to control the Dolby Pro Logic part of the IC.

DPL 3518A Integrated Functions:

- Full Dolby Surround Pro Logic Adaptive Matrix
- Pseudo-surround mode for signals not encoded in Dolby Surround
- PANORAMA sound mode (3-D Surround sound via 2 loudspeakers)
- Noise sequencer
- Automatic input balance control
- 7 kHz low-pass filter
- 100 Hz low-pass filter for subwoofer
- Modified Dolby B-type NR decoder
- 30 ms surround delay according to table created by Dolby Laboratories (1 ms steps)
- 2 I^2S input channels (e.g. MSP and DRPA)
- 2 I^2S output channels, freely programmable with sound channels L/R (resp. L + C/R + C), C/S, Sub or I^2S input
- Mode control: normal/phantom/wide/three channel/center off/panorama sound/stereo bypass
- Surround matrix mode control: adaptive/passive/effect
- Additional surround basewidth effect
- Reverberation of surround signals
- 2 digital input/output pins
- 1 digital input pin

DPL 3519A Integrated Functions (in Addition to all DPL 3518A Functions):

- Master volume control in dB units
- Level Trim for L, C, R, S in dB units, ±12 dB
- Identical treble/bass/loudness function for L, C, R, S
- 5-band equalizer for C channel
- Separate volume control for two surround outputs
- Additional line output for HIFI receiver connection (SCART output). Volume for this output is in dB units.
- 3 pairs of D/A converters
- Scart switches

DPL 3520A Integrated Functions (in Addition to all DPL 3518A and DPL 3519A Functions)

- 1 pair of A/D converters
- Note: the 5-band equalizer for C channel can only be used in coprocessor mode. No parallel AD input possible.

DPL 3520/19/18A Applications:

Dolby Pro Logic Surround System
in television sets
in satellite receivers
in video recorders

2. Functional Description

In the following, the functional description of the DPL 3520A is given. See section 13 for the modified block diagrams of the DPL 3518A and DPL 3519A.

Block diagram: DPL 3520A consists of three blocks:

– analog input section containing channel selection and 2 high-quality A/D converters

– DSP section performing audio baseband processing

– analog output section containing 6 D/A converters with 4-fold oversampling

Control-bus:

– The IC is controlled by I^2C-bus. The I^2C-bus device addresses are $80_{hex}/81_{hex}$, $84_{hex}/85_{hex}$ and $88_{hex}/89_{hex}$.

Clock System:

– Single crystal clock system (18.432 MHz), alternatively external clock.

Packages:

– 68-pin PLCC package

– 64-pin Shrink DIP package

– 52-pin Shrink DIP package

Power Consumption:

– typical: 450 mW at 5V

– typical: 120 mW at 8V

2.1. Features of the Analog Input Section

– three selectable analog pairs of audio baseband inputs (= three SCART inputs)
Input level: ≤ 2V RMS;
input impedance: ≥ 25 kΩ

– one selectable analog mono input;
Input level: ≤ 2V RMS;
input impedance: ≥ 10 kΩ

– 20 Hz to 20 kHz Bandwidth for SCART-to-SCART-copy facilities

– two high-quality A/D converters

2.2. Features of the DSP-Section

– flexible selection of audio sources to be processed

– 4-channel digital input via I^2S-Bus and 4-channel digital output via I^2S-Bus.

– digital baseband processing: volume, bass, treble, loudness on output channels 1 and 2.

– Dolby Pro Logic processing

– 100 Hz low-pass for subwoofer

– 30 ms delay line

A block diagram of the DSP software is shown in Fig. 2–2.

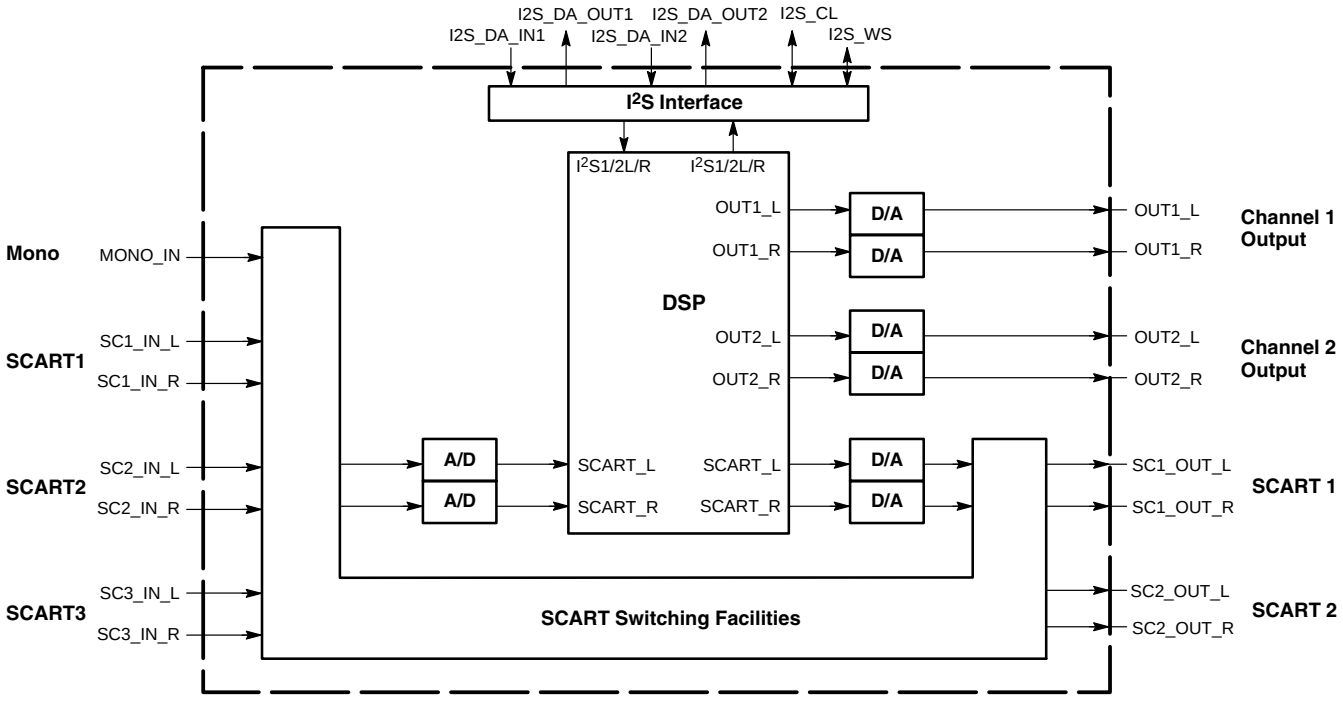


Fig. 2–1: Block diagram of the DPL 3520A

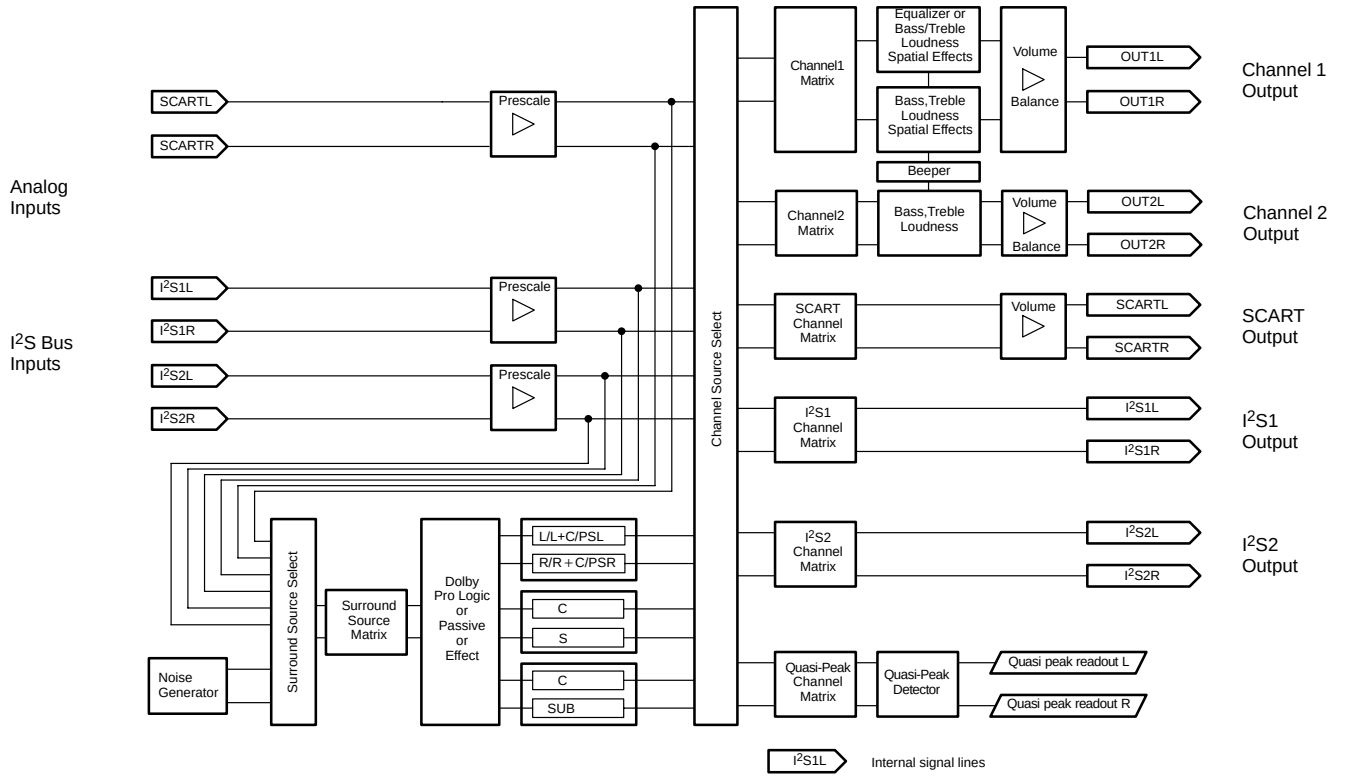


Fig. 2–2: Firmware block diagram

2.3. Features of the Analog Output Section

– channel 1 and 2: two pairs of 4-fold oversampled D/A-converters
Output level per channel: max. 1.4 V_{RMS}
Output resistance: max. 5 kΩ
S/N-Ratio: ≥ 85 dB at maximum volume; max. noise voltage in mute mode: ≤ 3 µV (BW: 20 Hz...16 kHz)

– one pair of four-fold oversampled D/A-converters supplying two selectable pairs of SCART-Outputs.
Output level per channel: max. 2 V_{RMS}
Output resistance: max. 0.5 kΩ
S/N-Ratio: ≥ 85 dB (20 Hz ... 16 kHz)

2.4. SCART Switches

The analog input and output sections offer a wide range of switching facilities, which are shown in Fig. 2–3.

The switches are controlled by the ACB bits defined in the audio processing interface (see section 9. Programming the DSP Part).

If the DPL is switched off by first pulling STANDBYQ low, and then disconnecting the 5 V, but keeping the 8 V power supply (‘**Standby’-mode**), the switches S1, S2, and S3 maintain their position and function. This facilitates the copying from selected SCART-inputs to SCART-outputs in the TV-sets standby mode.

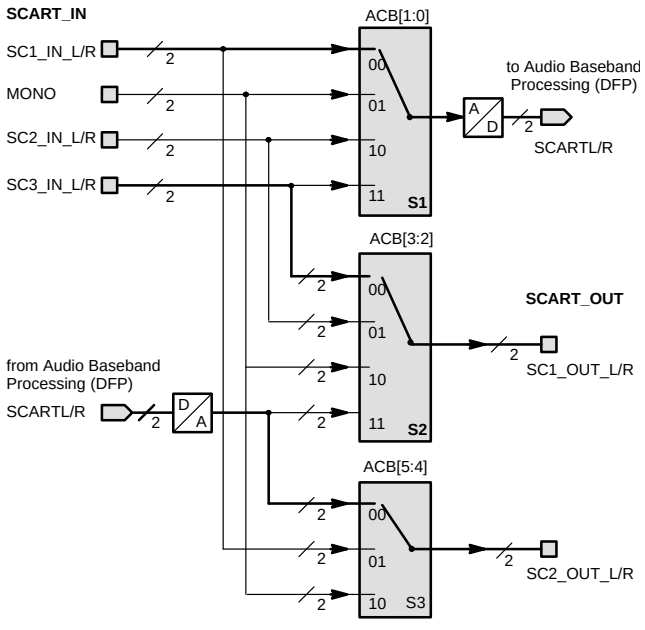
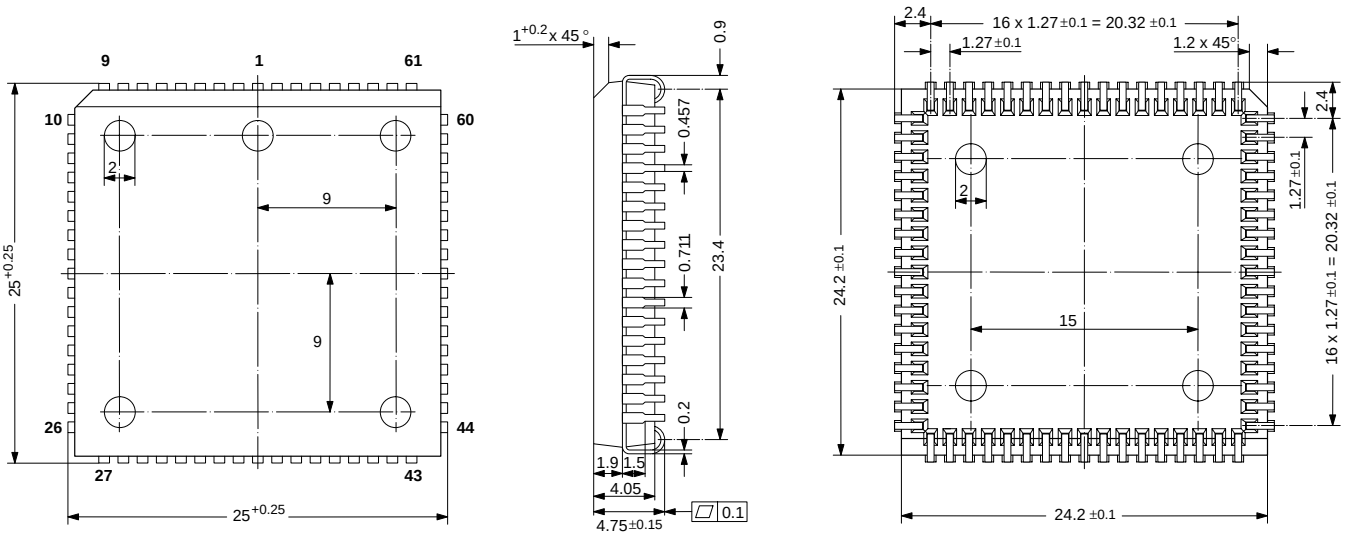


Fig. 2–3: SCART-Switching Facilities
Bold lines determine the default configuration

In case of power-on start or starting from standby, the IC switches automatically to the default configuration, shown in Fig. 2–3. This takes place after the first I²C transmission into the DFP part. By transmitting the ACB register first, the default setting mode can be changed.

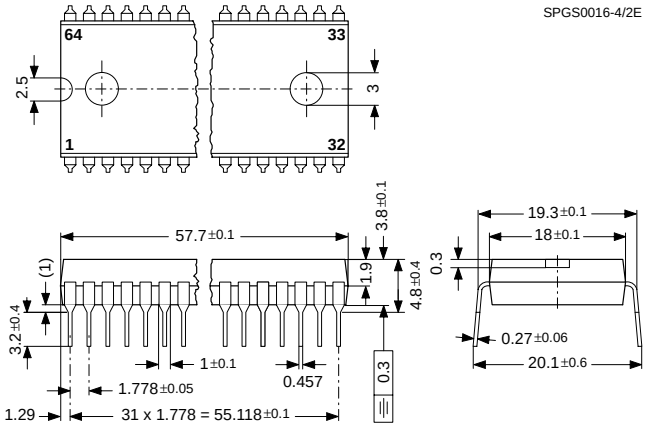
3. Specifications

3.1. Outline Dimensions



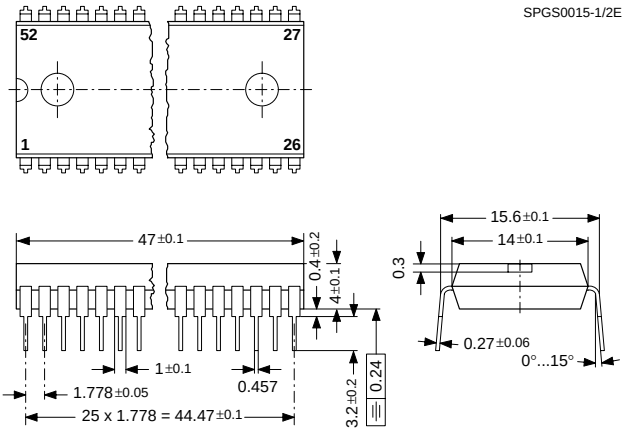
SPGS7004-3/4E

Fig. 3–1:
68-Pin Plastic Leaded Chip Carrier Package
(PLCC68)
Weight approximately 4.8 g
Dimensions in mm



SPGS0016-4/2E

Fig. 3–2:
64-Pin Plastic Shrink Dual-Inline-Package
(PSDIP64)
Weight approximately 9.0 g
Dimensions in mm



SPGS0015-1/2E

Fig. 3–3:
52-Pin Plastic Shrink Dual-Inline-Package
(PSDIP52)
Weight approximately 5.5 g
Dimensions in mm

3.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
DVSS: if not used, connect to DVSS
X = obligatory; connect as described in circuit diagram
AHVSS: connect to AHVSS
20/19: pin description valid for DPL 3520A and DPL 3519A
18: pin description valid for DPL 3518A

Pin No.			Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin				
1	16	14	NC		LV	Not connected
2	–	–	NC		LV	Not connected
3	15	13	NC		LV	Not connected
4	14	12	I2S_DA_IN1	IN	LV	I^2S1 data input
5	13	11	I2S_DA_OUT1	OUT	LV	I^2S1 data output
6	12	10	I2S_WS	OUT	LV	I^2S wordstrobe
7	11	9	I2S_CL	OUT	LV	I^2S clock
8	10	8	I2C_DA	IN/OUT	X	I^2C data
9	9	7	I2C_CL	IN	X	I^2C clock
10	8	–	NC	IN	X	Not connected
11	7	6	STANDBYQ	IN	X	Standby (low-active)
12	6	5	ADR_SEL	IN	X	I^2C-Bus address select
13	5	4	D_CTR_IO0	IN/OUT	LV	Digital control IO 0
14	4	3	D_CTR_IO1	IN/OUT	LV	Digital control IO 1
15	3	–	NC		LV	Not connected
16	2	–	NC		LV	Not connected
17	–	–	NC		LV	Not connected
18	1	2	AUD_CL_OUT	OUT	LV	Audio clock output
19	64	1	D_CTR_IN	IN	LV	Digital control input
20	63	52	XTAL_OUT	OUT	X	Crystal oscillator
21	62	51	XTAL_IN	IN	X	Crystal oscillator
22	61	50	TESTEN	IN	X	Test pin
23	60	49	NC		LV	Not connected
24	59	48	NC		LV	Not connected
25	58	47	NC		LV	Not connected
26	57	46	AVSUP		X	Analog power supply +5 V
27	56	45	AVSS		X	Analog ground
28	55	44	20/19: MONO_IN 18: NC	IN	LV	Mono input

Pin No.			Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin				
29	54	43	VREFTOP		X	Reference voltage
30	53	42	20/19: SC1_IN_R 18: NC	IN	LV	Scart input 1 in, right
31	52	41	20/19: SC1_IN_L 18: NC	IN	LV	Scart input 1 in, left
32	51	–	20/19: ASG1 18: NC		AHVSS	Analog Shield Ground 1
33	50	40	20/19: SC2_IN_R 18: NC	IN	LV	Scart input 2 in, right
34	49	39	20/19: SC2_IN_L 18: NC	IN	LV	Scart input 2 in, left
35	48	–	20/19: ASG2 18: NC		AHVSS	Analog Shield Ground 2
36	47	38	20/19: SC3_IN_R 18: NC	IN	LV	Scart input 3 in, right
37	46	37	20/19: SC3_IN_L 18: NC	IN	LV	Scart input 3 in, left
38	–	–	20/19: ASG4 18: NC		AHVSS	Analog Shield Ground 4
39	45	–	NC		LV	Not connected
40	44	–	NC		LV	Not connected
41	43	–	NC		LV	Not connected
42	42	36	20/19: AGNDC 18: NC		X	Analog reference voltage high voltage part
43	41	35	20/19: AHVSS 18: NC		X	Analog ground
44	40	34	20/19: CAPL_C1 18: NC		X	Volume capacitor Channel1
45	39	33	20/19: AHVSUP 18: NC		X	Analog power supply 8.0 V
46	38	32	20/19: CAPL_C2 18: NC		X	Volume capacitor Channel 2
47	37	31	20/19: SC1_OUT_L 18: NC	OUT	LV	Scart output 1, left
48	36	30	20/19: SC1_OUT_R 18: NC	OUT	LV	Scart output 1, right
49	35	29	20/19:VREF1 18: NC		X	Reference ground 1 high voltage part
50	34	28	20/19: SC2_OUT_L 18: NC	OUT	LV	Scart output 2, left

Pin No.			Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin				
51	33	27	20/19: SC2_OUT_R 18: NC	OUT	LV	Scart output 2, right
–	32	–	NC		LV	Not connected
–	31	–	NC		LV	Not connected
52	30	–	20/19: ASG3 18: NC		AHVSS	Analog Shield Ground 3
53	–	–	NC		LV	Not connected
54	–	–	NC		LV	Not connected
55	–	–	NC		LV	Not connected
56	29	25	20/19: DACC1_L 18: NC	OUT	LV	Analog output Channel 1, left
57	28	24	20/19: DACC1_R 18: NC	OUT	LV	Analog output Channel 1, right
58	27	23	20/19:VREF2 18: NC		X	Reference ground 2 high voltage part
59	26	22	20/19: DACC2_L 18: NC	OUT	LV	Analog output Channel 2, left
60	25	21	20/19: DACC2_R 18: NC	OUT	LV	Analog output Channel 2, right
61	24	20	RESETQ	IN	X	Power-on-reset
62	23	–	NC		LV	Not connected
63	22	–	NC		LV	Not connected
64	21	19	I2S_DA_OUT2	OUT	LV	I^2S2-data output
65	20	18	I2S_DA_IN2	IN	LV	I^2S2-data input
66	19	17	DVSS		X	Digital ground
67	18	16	DVSUP		X	Digital power supply +5 V
68	17	15	NC		LV	Not connected

3.3. Pin Configurations

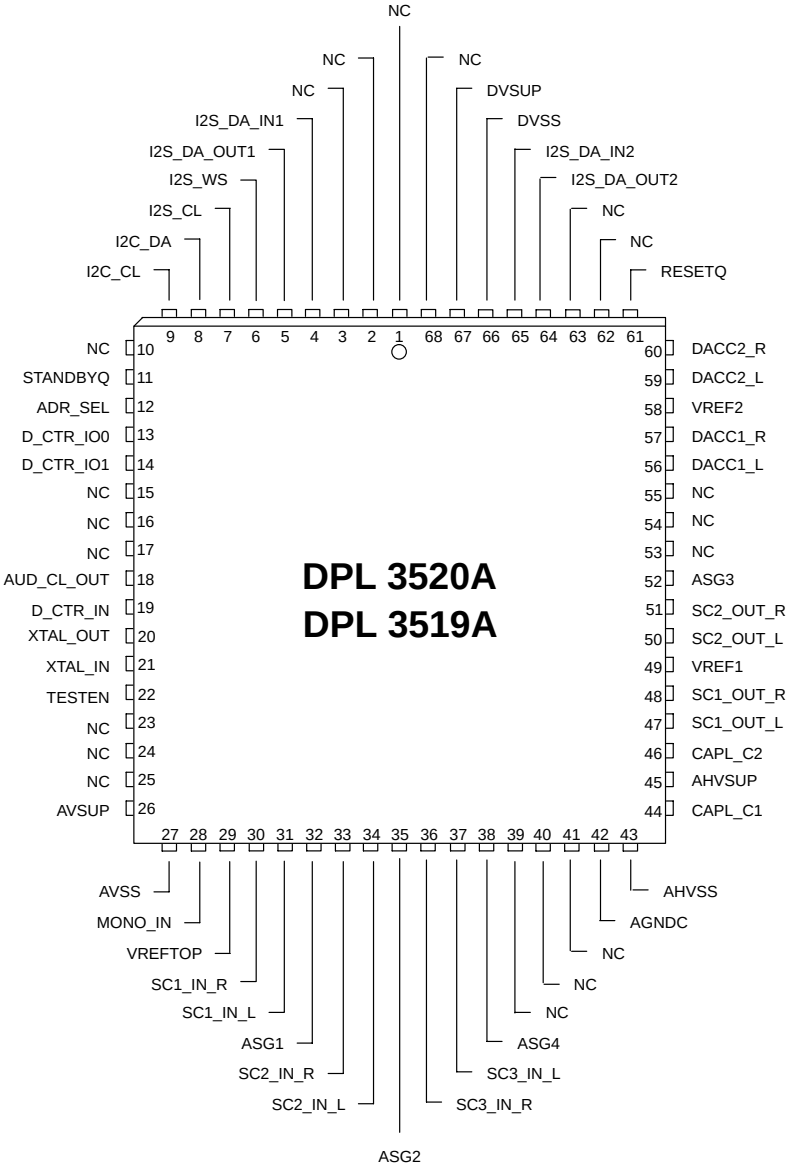


Fig. 3–4: 68-pin PLCC package of the DPL 3519A and DPL 3520A

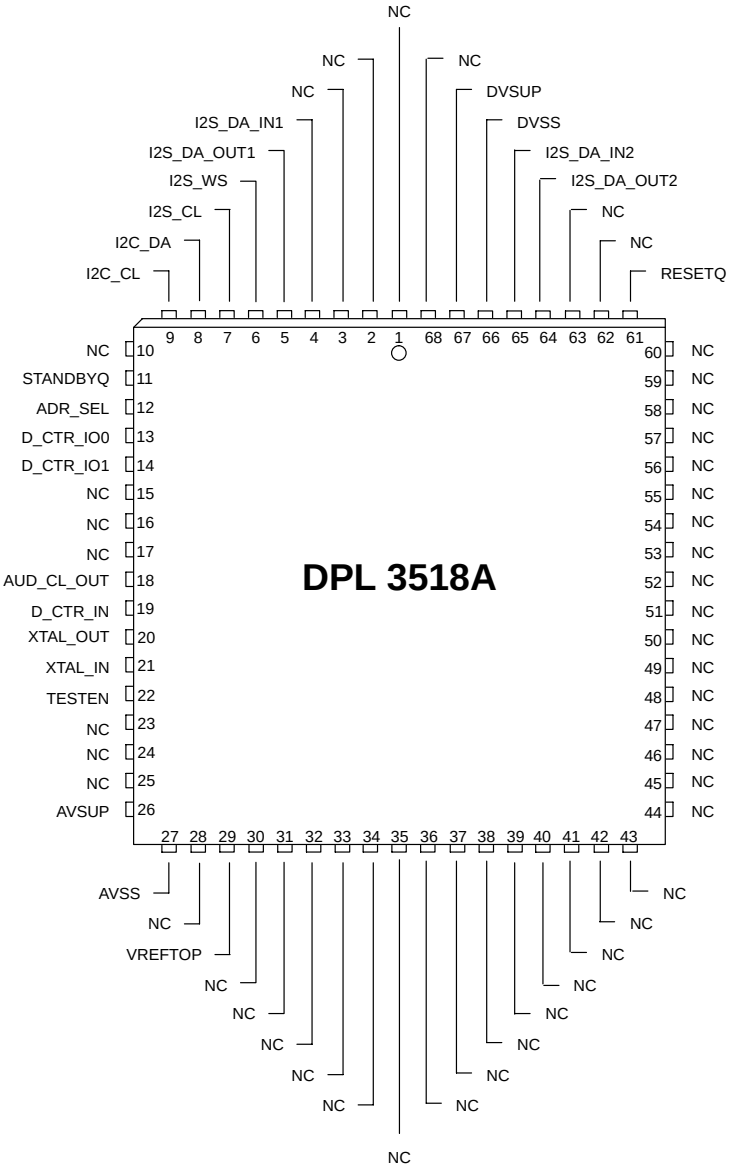


Fig. 3–5: 68-pin PLCC package of the DPL 3518A

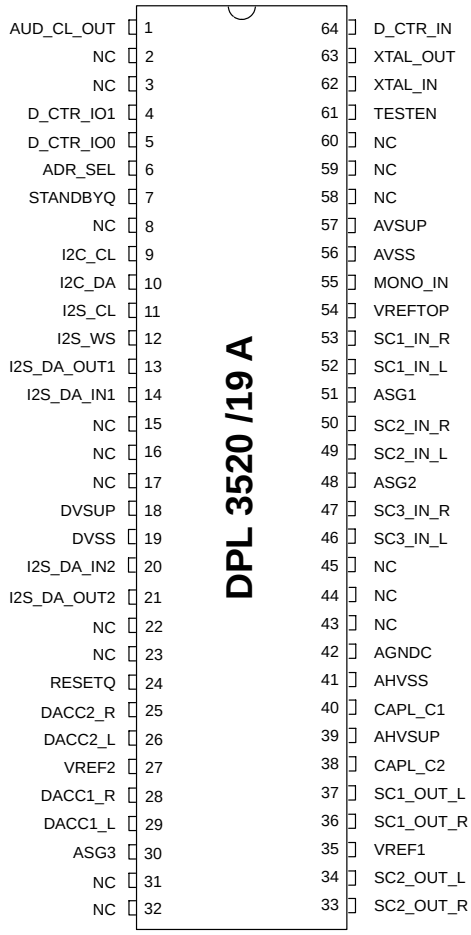


Fig. 3–6: 64-pin PSDIP package of the DPL 3519A and DPL 3520A

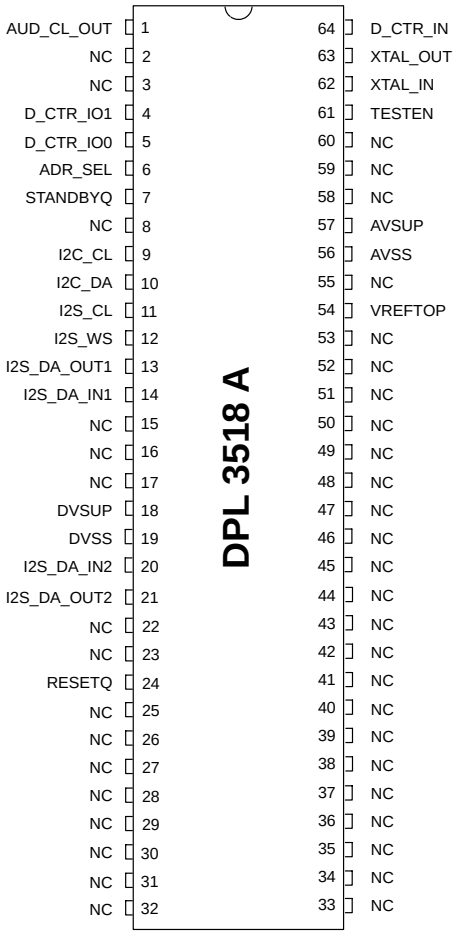


Fig. 3–7: 64-pin PSDIP package of the DPL 3518A

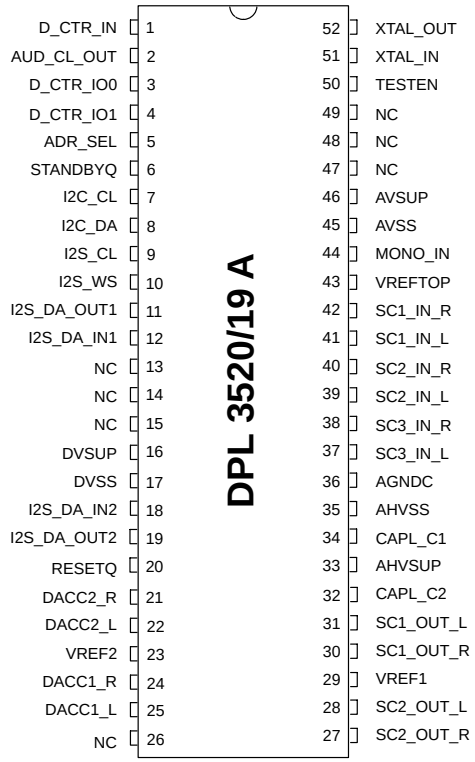


Fig. 3–8: 52-pin PSDIP package of the DPL 3519A and DPL 3520A

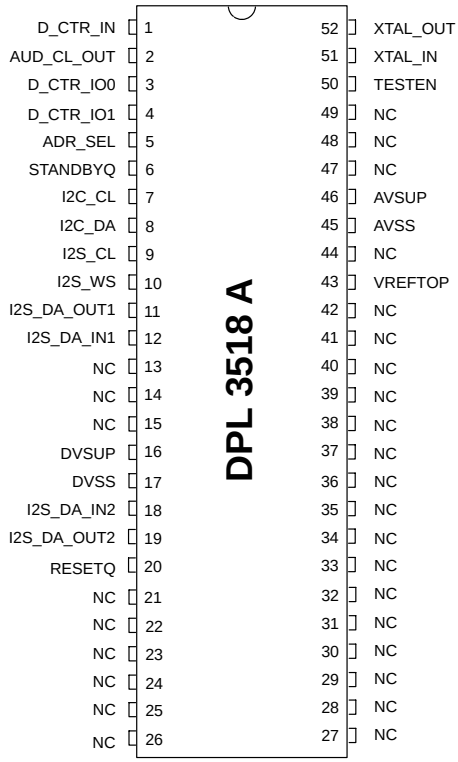


Fig. 3–9: 52-pin PSDIP package of the DPL 3518A

3.4. Pin Circuits (pin numbers refer to PLCC68 package)

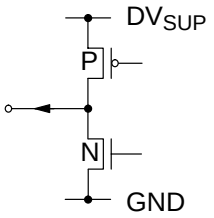


Fig. 3–10: Output Pins 5 and 64 (I^2S_DA_OUT1/2)

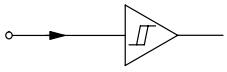


Fig. 3–12: Input Pins 4, 11, 12, 19, 61, 62, and 65 (I^2S_DA_IN1/2, STANDBYQ, ADR_SEL, D_CTR_IN, RESETQ, TESTEN)

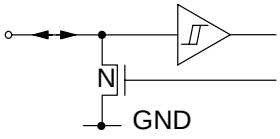


Fig. 3–11: Input/Output Pins 8 and 9 (I^2C_DA, I^2C_CL)

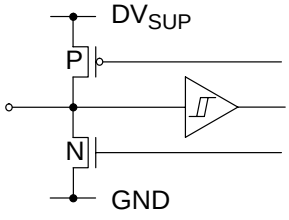


Fig. 3–13: Input/Output Pins 6, 7, 13, and 14 (I^2S_WS, I^2S_CL, D_CTR_IO0/1)

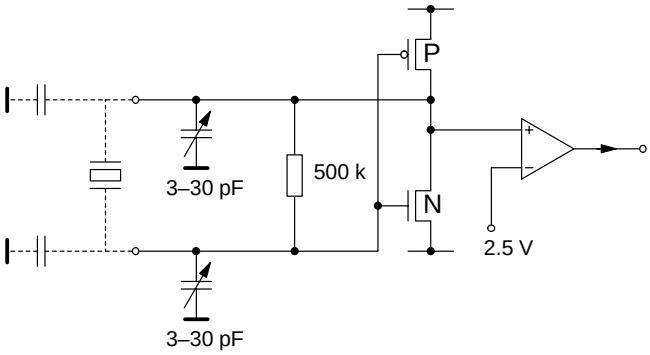


Fig. 3–14: Output/Input Pins 18, 20, and 21 (AUD_CL_OUT, XTALIN/OUT)

Fig. 3–15: Pin 29 (VREFTOP)

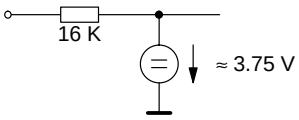


Fig. 3–16: Input Pin 28 (MONO_IN)

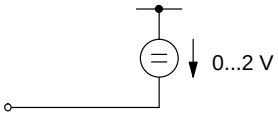


Fig. 3–17: Capacitor Pins 44 and 46 (CAPL_C1, CAPL_C2)

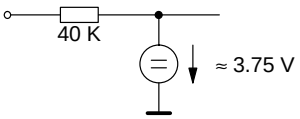


Fig. 3–18: Input Pins 30, 31, 33, 34, 36, and 37 (SC1–3_IN_L/R)

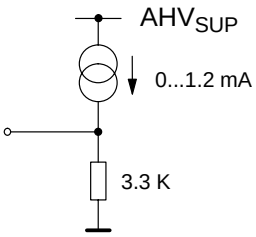


Fig. 3–19: Output Pins 56, 57, 59, and 60 (DACC1_L/R, DACC2_L/R)

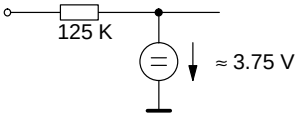


Fig. 3–20: Pin 42 (AGNDC)

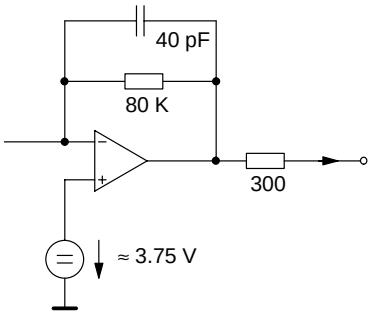


Fig. 3–21: Output Pins 47, 48, 50 and 51 (SC_1/2_OUT_L/R)

3.5. Electrical Characteristics

3.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	70	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP1}	First Supply Voltage	AHVSUP	–0.3	9.0	V
V_{SUP2}	Second Supply Voltage	DVSUP	–0.3	6.0	V
V_{SUP3}	Third Supply Voltage	AVSUP	–0.3	6.0	V
dV_{SUP23}	Voltage between AVSUP and DVSUP	AVSUP, DVSUP	–0.5	0.5	V
P_{TOT}	Chip Power Dissipation PLCC68 without Heat Spreader	AHVSUP, DVSUP, AVSUP		1100	mW
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP2}+0.3	V
I_{Idig}	Input Current, all Digital Pins	–	–20	+20	mA[1)]
V_{Iana}	Input Voltage, all Analog Inputs	SCn_IN_s,[2)] MONO_IN	–0.3	V_{SUP1}+0.3	V
I_{Iana}	Input Current, all Analog Inputs	SCn_IN_s,[2)] MONO_IN	–5	+5	mA[1)]
I_{Oana}	Output Current, all SCART Outputs	SCn_OUT_s[2)]	[3)], [4)]	[3)], [4)]	
I_{Oana}	Output Current, all Analog Outputs except SCART Outputs	DACp_s[2)]	[3)]	[3)]	
I_{Cana}	Output Current, other pins connected to capacitors	CAPL_p,[2)] AGNDC	[3)]	[3)]	

1) positive value means current flowing into the circuit
2) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “C1” or “C2”
3) The Analog Outputs are short circuit proof with respect to First Supply Voltage and Ground.
4) Total chip power dissipation must not exceed absolute maximum rating.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.5.2. Recommended Operating Conditions

at T_A = 0 to 70 °C

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{SUP1}	First Supply Voltage	AHVSUP	7.6	8.0	8.4	V
V_{SUP2}	Second Supply Voltage	DVSUP	4.75	5.0	5.25	V
V_{SUP3}	Third Supply Voltage	AVSUP	4.75	5.0	5.25	V
V_{REIL}	RESET Input Low Voltage	RESETQ			0.45	V_{SUP2}
V_{REIH}	RESET Input High Voltage		0.8			V_{SUP2}
t_{REIL}	RESET Low Time after DVSUP Stable and Oscillator Startup		5			µs
V_{DIGIL}	Digital Input Low Voltage	STANDBYQ, ADR_SEL, TESTEN, D_CTR_IN, D_CTR_IO_0/1			0.25	V_{SUP2}
V_{DIGIH}	Digital Input High Voltage		0.75			V_{SUP2}
t_{STBYQ1}	STANDBYQ Setup Time before Turn-off of Second Supply Voltage	STANDBYQ, DVSUP	1			µs
I^2C-Bus Recommendations						
V_{IMIL}	I^2C-BUS Input Low Voltage	I^2C_CL, I^2C_DA			0.3	V_{SUP2}
V_{IMIH}	I^2C-BUS Input High Voltage		0.6			V_{SUP2}
f_{IM}	I^2C-BUS Frequency	I^2C_CL			1.0	MHz
t_{I2C1}	I^2C START Condition Setup Time	I^2C_CL, I^2C_DA	120			ns
t_{I2C2}	I^2C STOP Condition Setup Time		120			ns
t_{I2C3}	I^2C-Clock Low Pulse Time	I^2C_CL	500			ns
t_{I2C4}	I^2C-Clock High Pulse Time		500			ns
t_{I2C5}	I^2C-Data Setup Time Before Rising Edge of Clock	I^2C_CL, I^2C_DA	55			ns
t_{I2C6}	I^2C-Data Hold Time after Falling Edge of Clock		55			ns
V_{I2SIL}	I^2S-Data Input Low Voltage	I2S_DA_IN1/2			0.25	V_{SUP2}
V_{I2SIH}	I^2S-Data Input High Voltage		0.75			V_{SUP2}
t_{I2S1}	I^2S-Data Input Setup Time before Rising Edge of Clock	I2S_DA_IN1/2, I2S_CL	20			ns
t_{I2S2}	I^2S-Data Input Hold Time after Falling Edge of Clock		0			ns

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{I2SIDL}	I^2S-Input Low Voltage when DPL 3520/19/18A in I2S-Slave-Mode	I2S_CL, I2S_WS			0.25	V_{SUP2}
V_{I2SIDH}	I^2S-Input High Voltage when DPL 3520/19/18A in I2S-Slave-Mode		0.75			V_{SUP2}
f_{I2SCL}	I^2S-Clock Input Frequency when DPL 3520/19/18A in I2S-Slave-Mode	I2S_CL		1.024		MHz
R_{I2SCL}	I^2S-Clock Input Ratio when DPL 3520/19/18A in I2S-Slave-Mode		0.9		1.1	MHz
f_{I2SWS}	I^2S-Wordstrobe Input Frequency when DPL 3520/19/18A in I2S-Slave-Mode	I2S_WS		32.0		kHz
t_{I2SWS1}	I^2S-Wordstrobe Input Setup Time before Rising Edge of Clock when DPL 3520/19/18A in I2S-Slave-Mode	I2S_WS, I2S_CL	60			ns
t_{I2SWS2}	I^2S-Wordstrobe Input Hold Time after Falling Edge of Clock when DPL 3520/19/18A in I2S-Slave-Mode		0			ns
Crystal Recommendations for Master-Slave Application						
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–20		+20	ppm
D_{TEM}	Frequency Variation versus Temperature		–20		+20	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF
C_1	Motional (Dynamic) Capacitance		19	24		fF
Load Capacitance Recommendations for Master-Slave Applications						
C_L	External Load Capacitance[2)]	XTAL_IN, XTAL_OUT	PSDIP 1.5 PLCC 3.3			pF pF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25°C)		18.431		18.433	MHz

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Crystal Recommendations for Stand Alone Application (No Master-Slave Mode possible)						
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–100		+100	ppm
D_{TEM}	Frequency Variation versus Temperature		–50		+50	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF
Load Capacitance Recommendations for Stand Alone Application (No Master-Slave Mode possible)						
C_L	External Load Capacitance[2)]	XTAL_IN, XTAL_OUT	PSDIP 1.5 PLCC 3.3			pF pF
Amplitude Recommendation for Operation with External Clock Input (C_{load} after reset = 22 pF)						
V_{XCA}	External Clock Amplitude	XTAL_IN	0.7			V_{pp}
Analog Input and Output Recommendations						
C_{AGNDC}	AGNDC-Filter-Capacitor	AGNDC	–20%	3.3		µF
	Ceramic Capacitor in Parallel		–20%	100		nF
C_{inSC}	DC-Decoupling Capacitor in front of SCART Inputs	SCn_IN_s[1)]	–20%	330	+20%	nF
V_{inSC}	SCART Input Level				2.0	V_{RMS}
V_{inMONO}	Input Level, Mono Input	MONO_IN			2.0	V_{RMS}
R_{LSC}	SCART Load Resistance	SCn_OUT_s[1)]	10			kΩ
C_{LSC}	SCART Load Capacitance				7.5	nF
C_{VMA}	Channel1/2 Volume Capacitor	CAPL_s[1)]		10		µF
C_{FMA}	Channel1/2 Filter Capacitor	DACp_s[1)]	–10%	1	+10%	nF
$C_{VREFTOP}$	VREFTOP-Filter-Capacitor	VREFTOP	–20%	10		µF

1) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “C1” or “C2”

2) External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match 18.432 MHz as closely as possible. Due to different layouts of customer PCBs, the matching capacitor size should be defined in the application. The suggested values (1.5 pF/3.3 pF) are figures based on experience with various PCB layouts.

3.5.3. Characteristics

at T_A = 0 to 70 °C, f_{CLOCK} = 18.432 MHz, V_{SUP1} = 7.6 to 8.4 V, $V_{SUP2,3}$ = 4.75 to 5.25 V for min./max. values

(Typical values are measured at T_A = 25 °C, AHVSUP = 8 V, DVSUP = 5 V, AVSUP = 5 V.)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
DCO							
f_{CLOCK}	Clock Input Frequency	XTAL_IN		18.432		MHz	
D_{CLOCK}	Clock High to Low Ratio		45		55	%	
t_{JITTER}	Clock Jitter (verification not provided in production test)				50	ps	
V_{xtalDC}	DC-Voltage Oscillator			2.5		V	
$t_{Startup}$	Oscillator Startup Time at VDD Slew-rate of 1 V / 1 µs	XTAL_IN, XTAL_OUT		0.4	1.0	ms	
Power Supply							
I_{SUP1A}	First Supply Current (active) Analog Volume for channel1/2 at 0dB Analog Volume for channel1/2 at –30dB at T_j = 27 °C	AHVSUP	 8.2 5.6	 14.8 10.0	 22.0 15.0	 mA mA	f = 18.432 MHz AHVSUP = 8 V DVSUP = 5 V AVSUP = 5 V
I_{SUP2A}	Second Supply Current (active)	DVSUP	60	65	70	mA	f = 18.432 MHz DVSUP = 5 V
I_{SUP3A}	Third Supply Current (active)	AVSUP		25		mA	f = 18.432 MHz AVSUP = 5 V
I_{SUP1S}	First Supply Current (standby mode) at T_j = 27 °C	AHVSUP	2.8	5.0	7.2	mA	STANDBYQ = low VSUP = 8 V
Audio Clock Output							
V_{APUAC}	Audio Clock Output AC Voltage	AUD_CL_OUT	1.2			V_{pp}	40 pF load
V_{APUDC}	Audio Clock Output DC Voltage		0.4		0.6	V_{SUP1}	
Digital Output							
V_{DCTROL}	Digital Output Low Voltage	D_CTR_IO0 D_CTR_IO1			0.4	V	I_{DDCTR} = 1 mA
V_{DCTROH}	Digital Output High Voltage		4.0			V	I_{DDCTR} = –1 mA
I^2C Bus							
V_{IMOL}	I^2C-Data Output Low Voltage	I^2C_DA			0.4	V	I_{IMOL} = 3 mA
I_{IMOH}	I^2C-Data Output High Current				1	µA	V_{IMOH} = 5 V
t_{IMOL1}	I^2C-Data Output Hold Time after Falling Edge of Clock	I^2C_DA, I^2C_CL	15			ns	
t_{IMOL2}	I^2C-Data Output Setup Time before Rising Edge of Clock		100			ns	f_{IM} = 1 MHz DVSUP = 5 V
I^2S Bus							
V_{I2SOL}	I^2S Output Low Voltage	I2S_WS, I2S_CL, I2S_DA_OUT	0.4			V	I_{I2SOL} = 1 mA
V_{I2SOH}	I^2S Output High Voltage				4.0	V	I_{I2SOH} = –1 mA
f_{I2SCL}	I^2S-Clock Output Frequency	I2S_CL		1204		kHz	DVSUP = 5 V
f_{I2SWS}	I^2S-Wordstrobe Output Frequency	I2S_WS		32.0		kHz	DVSUP = 5 V

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$t_{I2S1/I2S2}$	I^2S-Clock High/Low-Ratio	I2S_CL	0.9	1.0	1.1		
t_{I2S3}	I^2S-Data Setup Time before Rising Edge of Clock	I2S_CL, I2S_DA_OUT	200			ns	DVSUP = 4.75 V
t_{I2S4}	I^2S-Data Hold Time after Falling Edge of Clock		12			ns	DVSUP = 5.25 V
t_{I2S5}	I^2S-Wordstrobe Setup Time before Rising Edge of Clock	I2S_CL, I2S_WS	100			ns	DVSUP = 4.75 V
t_{I2S6}	I^2S-Wordstrobe Hold Time after Falling Edge of Clock		50			ns	DVSUP = 5.25 V
Analog Ground							
V_{AGNDC0}	AGNDC Open Circuit Voltage	AGNDC	3.64	3.73	3.84	V	$R_{load} \geq 10\ M\Omega$
R_{outAGN}	AGNDC Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C		70 70	125	180 180	kΩ kΩ	3 V ≤ V_{AGNDC} ≤ 4 V
Analog Input Resistance							
R_{inSC}	SCART Input Resistance at T_j = 27 °C from T_A = 0 to 70 °C	SCn_IN_s[1)]	25 25	40	58 58	kΩ kΩ	f_{signal} = 1 kHz, I ≤ 0.05 mA
R_{inMONO}	MONO Input Resistance at T_j = 27 °C from T_A = 0 to 70 °C	MONO_IN	10 10	16	23 23	kΩ kΩ	f_{signal} = 1 kHz, I ≤ 0.1 mA
Audio Analog-to-Digital-Converter							
V_{AICL}	Analog Input Clipping Level for Analog-to-Digital-Conversion	SCn_IN_s,[1)] MONO_IN	2.00	2.12	2.25	V_{RMS}	f_{signal} = 1 kHz
SCART Outputs							
R_{outSC}	SCART Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	SCn_OUT_s[1)]	0.20 0.20	0.33	0.46 0.5	kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
dV_{OUTSC}	Deviation of DC-Level at SCART Output from AGNDC Voltage		–70		+70	mV	
A_{SCtoSC}	Gain from Analog Input to SCART Output	SCn_IN_s[1)] MONO_IN → SCn_OUT_s[1)]	–1.0	0	+0.5	dB	f_{signal} = 1kHz
$f_{rSCtoSC}$	Frequency Response from Analog Input to SCART Output bandwidth: 0 to 20000 Hz		–0.5	0	+0.5	dB	with respect to 1 kHz
V_{outSC}	Signal Level at SCART-Output during full-scale digital input signal from DSP	SCn_OUT_s[1)]	1.8	1.9	2.0	V_{RMS}	f_{signal} = 1 kHz

1) "n" means "1", "2" or "3", "s" means "L" or "R", "p" means "C1" or "C2"

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Channel 1 and 2 Outputs							
R_{outMA}	Channel1/2 Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	DACp_s[1]	2.1 2.1	3.3	4.6 5.0	kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
$V_{outDCMA}$	DC-Level at Channel1/2-Output for Analog Volume at 0 dB for Analog Volume at –30 dB		1.74 –	1.94 61	2.28 –	V mV	
V_{outMA}	Signal Level at Channel1/2-Output during full-scale digital input signal from DSP for Analog Volume at 0 dB		1.23	1.37	1.51	V_{RMS}	f_{signal} = 1 kHz
Analog Performance							
SNR	Signal-to-Noise Ratio						
	from Analog Input to DSP	MONO_IN, SCn_IN_s[1]	85	88		dB	Input Level = –20 dB with resp. to V_{AICL}, f_{sig} = 1 kHz, equally weighted 20 Hz ... 16 kHz[2]
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1] → SCn_OUT_s[1]	93	96		dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz ... 20 kHz
	from DSP to SCART Output	SCn_OUT_s[1]	85	88		dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz ... 15 kHz[3]
	from DSP to Channel1/2-Output for Analog Volume at 0 dB for Analog Volume at –30 dB	DACp_s[1]	85 78	88 83		dB dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz ... 15 kHz[3]
THD	Total Harmonic Distortion						
	from Analog Input to DSP	MONO_IN, SCn_IN_s[1]			0.05	%	Input Level = –3 dBr with resp. to V_{AICL}, f_{sig} =1kHz, equally weighted 20 Hz ...16 kHz, R_{Load} = 30 kΩ[2]
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s → SCn_OUT_s[1]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 20 kHz, R_{Load} = 30 kΩ
	from DSP to SCART Output	SCn_OUT_s[1]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 16 kHz, R_{Load} = 30 kΩ[3]
	from DSP to Channel1/2 Output	DACp_s[1]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 16 kHz, R_{Load} = 30 kΩ[3]

1) "n" means "1", "2" or "3", "s" means "L" or "R", "p" means "C1" or "C2"
2) DSP measured at I^2S-Output
3) DSP Input at I^2S-Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
XTALK	Crosstalk attenuation – PLCC68 – PSDIP64						Input Level = –3 dB, f_{sig} = 1 kHz, unused analog inputs connected to ground by Z<1 kΩ
	between left and right channel within SCART Input/Output pair (L→R, R→L)						equally weighted 20 Hz ... 20 kHz
	SCn_IN → SCn_OUT[1)]	PLCC68 PSDIP64	80 80			dB dB	[2)]
	SCn_IN → DSP[1)]	PLCC68 PSDIP64	80 80			dB dB	
	DSP → SCn_OUT[1)]	PLCC68 PSDIP64	80 80			dB dB	[3)]
	between left and right channel within channel1/2 Output pair						equally weighted 20 Hz ... 16 kHz
	DSP → DACp[1)]	PLCC68 PSDIP64	80 75			dB dB	[3)]
	between SCART Input/Output pairs[1)] D = disturbing program O = observed program						(equally weighted 20 Hz ... 20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D: MONO/SCn_IN → SCn_OUT O: MONO/SCn_IN → SCn_OUT[1)]	PLCC68 PSDIP64	100 100			dB dB	
	D: MONO/SCn_IN → SCn_OUT O: or unsel. MONO/SCn_IN → DSP[1)]	PLCC68 PSDIP64	95 95			dB dB	[2)]
	D: MONO/SCn_IN → SC1_OUT O: DSP → SCn_OUT[1)]	PLCC68 PSDIP64	100 100			dB dB	[3)]
	D: MONO/SCn_IN → unselected O: DSP → SC1_OUT[1)]	PLCC68 PSDIP64	100 100			dB dB	[3)]
	Crosstalk between channel 1 and channel 2 Output pairs DSP → DACp[1)]	PLCC68 PSDIP64	95 90			dB dB	(equally weighted 20 Hz ... 16 kHz)[3)] same signal source on left and right disturbing channel, effect on each observed output channel
	Crosstalk from channel 1 and channel 2 to SCART Output and vice versa D = disturbing program O = observed program						(equally weighted 20 Hz ... 20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D: MONO/SCn_IN/DSP → SCn_OUT O: DSP → DACp[1)]	PLCC68 PSDIP64	90 85			dB dB	SCART output load resistance 10 kΩ
	D: MONO/SCn_IN/DSP → SCn_OUT O: DSP → DACp[1)]	PLCC68 PSDIP64	95 85			dB dB	SCART output load resistance 30 kΩ
	D: DSP → DACp O: MONO/SCn_IN → SCn_OUT[1)]	PLCC68 PSDIP64	100 95			dB dB	[3)]
	D: DSP → DACp O: DSP → SCn_OUT[1)]	PLCC68 PSDIP64	100 95			dB dB	

1) "n" means "1", "2" or "3", "s" means "L" or "R", "p" means "C1" or "C2"
2) DSP measured at I^2S-Output
3) DSP Input at I^2S-Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
PSRR: rejection of noise on AHVSUP at 1 kHz							
PSRR	AGNDC	AGNDC		80		dB	
	From analog Input to DSP	MONO_IN SCn_IN_s[1)]		69		dB	
	From analog Input to SCART Output	MONO_IN SCn_IN_s,[1)] SCn_OUT_s[1)]		74		dB	
	From DSP to SCART Output	SCn_OUT_s[1)]		70		dB	
	From DSP to channel1/2 Output	DACp_s[1)]		80		dB	

1) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “C1” or “C2”

3.5.4. Measurements According to Dolby Specifications, Typical Values

(Typical values are measured at T_A = 25 °C, AHVSUP = 8 V, DVSUP = 5 V, AVSUP = 5 V.)

Crosstalk at cardinal point at High Level Input (+15 dB @ 1 kHz = 0 dB Full Scale = 2 Vrms)				
Channel	**L**	**C**	**R**	**S**
Left:	+0.17	–60	–68	–57
Center:	–53	0.0	–53	–63
Right:	–68	–62	+0.03	–60
Surround:	–56	–70	–56	+0.02

Crosstalk at cardinal point at Low Level Input (–20dB @ 1kHz = –35dBdB Full Scale)				
Channel	**L**	**C**	**R**	**S**
Left:	+0.08	–44	–46	–41
Center:	–45	0.0	–46	–41
Right:	–45	–44	0.05	–41
Surround:	–39	–44	–44	–2.58

Frequency Response Characteristics				
Mode	**L**	**C**	**R**	**S**
Normal	20/15.4k	100/15.4k	20/15.4k	20/7k
Wide	20/15.4k	20/15.4k	20/15.4k	20/7k
Phantom	20/15.4k	————————	20/15.4k	20/7k

SNR Measurements				
	L	**C**	**R**	**S**
Weighted	–69dB	–69dB	–69dB	–69dB

Measured on the Dolby Stand Alone Board.
Conditions: 355 mVrms @ SCART1IN with 2 kHz
Scart Prescale = 20 h,
Vol = –9 dB
100 mVrms output @DAC1out

measured with CCIR/ARM (System One: CCIR–2k, AVG)

4. I²C-Bus Interface

As a slave receiver, the DPL can be controlled via I²C-bus. Access to internal memory locations is achieved by subaddressing. The MODE_REG, the CONTROL register and the DFP processor have separate subaddressing register banks.

In order to allow for more DPL or MSP ICs to be connected to the control bus, an ADR_SEL pin was implemented. With ADR_SEL pulled to high, low, or left open, the DPL responds to changed device addresses. Thus, three identical devices can be selected.

By means of the RESET bit in the CONTROL register, all devices with the same device address are reset.

The IC is selected by asserting a special device address in the address part of an I²C-transmission. A device address pair is defined as a write address (80 hex, 84 hex, or 88 hex) and a read address (81 hex, 85 hex, or 89 hex). Writing is done by sending the device write address first, followed by the subaddress byte, two address bytes, and two data bytes. For reading, the read address has to be transmitted first by sending the device write address (80 hex, 84 hex, or 88 hex), followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is done by sending the device read address (81 hex, 85 hex, or 89 hex) and reading two bytes of data. Refer to Fig. 4–1: I²C-Bus Protocol and section 4.2.: Proposal for DPL I²C-Telegrams.

Due to the internal architecture of the DPL, the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms. If the receiver (DPL) cannot receive another complete byte of data until it has performed some other function, it can hold the clock line I2C_CL LOW to force the transmitter into a wait state. The positions within a transmission where this may happen are indicated by 'Wait' in section 4.1. The maximum wait period of the DPL during normal operation mode is less than 1 ms.

I²C-Bus error conditions:
If an internal error occurs, the DPLs wait period is extended to a maximum of 1.8 ms. Afterwards, the DPL does not acknowledge (NAK) the device address. The data line will be left HIGH by the DPL and the clock line will be released. The master can then generate a STOP condition to abort the transfer.

By means of NAK, the master is able to recognize the error state and to reset the IC via I²C-Bus. While transmitting the reset protocol (see 4.1.) to 'CONTROL', the master must ignore the 'Not Acknowledge Bits' (NAK) of the DPL.

Table 4–1: I²C-Bus Device and Subaddresses

Name	Binary Value	Hex Value	Hex Value	Hex Value	Mode	Function
		ADR_SEL=				
		low	high	left open		
DPL	**1000 xx0x**	**80/81**	**84/85**	**88/89**	**R/W**	**DPL device address**
CONTROL	0000 0000	00			W	software reset
WR_MR	0001 0000	10			W	write address MODE_REG
RD_MD	0001 0001	11			W	read address MODE_REG
WR_DFP	0001 0010	12			W	write address DFP
RD_DFP	0001 0011	13			W	read address DFP

Table 4–2: Control Register

Name	MSB	14	13..1	LSB
CONTROL	RESET	0	0	0

4.1. Protocol Description

Write to DFP or MODE_REG

S	hex 80	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from DFP or MODE_REG

S	hex 80	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	S	hex 81	Wait	ACK	data-byte high	ACK	data-byte low	NAK	P

Write to the Control Register

S	hex 80	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I^2C_DA from slave (=DPL, grey) or master (=CCU, hatched)
NAK = Not Acknowledge-Bit: HIGH on I^2C_DA from master (=CCU, hatched) to indicate 'End of Read' or from DPL indicating internal error state
Wait = I^2C-Clock line held low by the slave (=DPL) while interrupt is serviced (<1 ms)

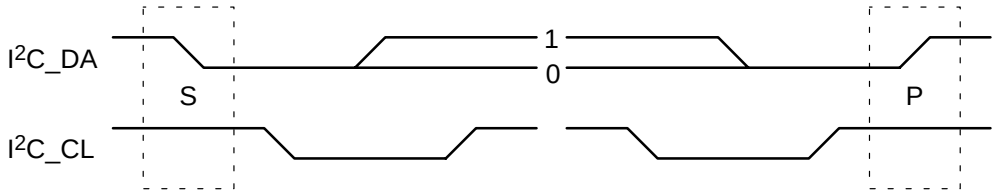


Fig. 4–1: I^2C-bus protocol (MSB first; data must be stable while clock is high)

4.2. Proposal for DPL I^2C-Telegrams

4.2.1. Symbols

daw Write Device Address
dar Read Device Address
< Start Condition
> Stop Condition
aa Address Byte
dd Data Byte

4.2.2. Write Telegrams

`<daw 00 dd dd>` software RESET
`<daw 10 aa aa dd dd>` write data into MODE_REG register
`<daw 12 aa aa dd dd>` write data into DFP register

4.2.3. Read Telegrams

`<daw 11 aa aa <dar dd dd>` read data from MODE_REG register
`<daw 13 aa aa <dar dd dd>` read data from DFP register

4.2.4. Examples

`<80 00 80 00>` RESET DPL statically
`<80 00 00 00>` clear RESET
`<80 12 00 08 03 20>` set channel source 1 to DOLBYLR and Matrix to STEREO

4.3. Start-Up Sequence

After power on or RESET, the IC is in an inactive state. The CCU has to transmit the required coefficient set for a given operation via the I^2C-bus.

5. Audio PLL and Crystal Specifications

5.1. Operation with Crystal

The DPL requires a 18.432 MHz (12 pF, parallel) crystal. The clock supply of the whole system depends on the DPL operation mode:

1. Stand-Alone
The system clock runs free on the crystal's 18.432 MHz.

2. I^2S slave operation:
In this case, the system clock is locked to a synchronizing signal (I2S_WS) supplied by the coprocessor chip.

Remark on using the crystal:
External capacitors are required at each crystal pin to ground. They are necessary for tuning the open-loop frequency of the internal PLL and for stabilizing the frequency in closed-loop operation. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match the center of the tolerance range between 18.433 and 18.431 MHz as closely as possible.

5.2. Operation without Crystal

When used together with a member of the MSP family, the DPL can be driven by the 18.432 MHz clock supplied by the MSP. The clock input is: XTAL_IN (connection via coupling capacitor (C>1nF)). No crystal is used in this mode.

6. I^2S-Bus Interface

By means of this standardized interface, additional feature processors can be connected to the DPL. Two possible formats are supported: The standard mode (MODE_REG[4]=0) selects the SONY format, where the I2S_WS signal changes at the word boundaries. The so-called PHILIPS format, which is characterized by a change of the I2S_WS signal one I2S_CL period before the word boundaries, is selected by setting MODE_REG[4]=1.

The DPL normally serves as the slave on the I^2S interface (default setting after power-up). I^2S-clock and word strobe lines are input to the DPL and the master clock is synchronized to 576 times the I2S_WS rate (32 kHz). By setting MODE_REG[3]=0, the DPL is switched to Master Mode. Now, these lines are input to the DPL and the master clock is synchronized to 576 times the I2S_WS rate (32 kHz).

The I^2S-bus interface consists of six pins:

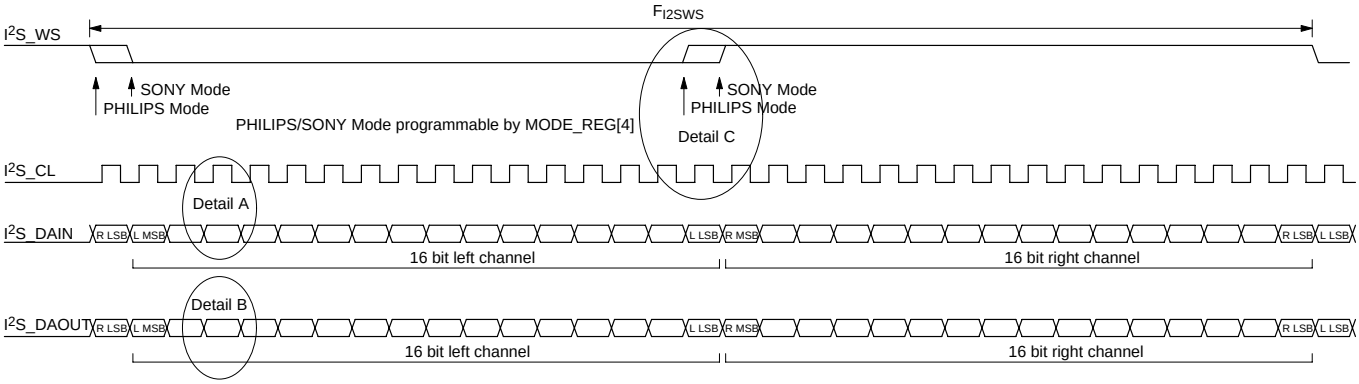
1. I2S_DA_IN1, I2S_DA_IN2:
For input, four channels (two channels per line, 2×16 bits) per sampling cycle (32 kHz) are transmitted.

2. I2S_DA_OUT1, I2S_DA_OUT2:
For output, four channels (two channels per line, 2×16 bits) per sampling cycle (32 kHz) are transmitted.

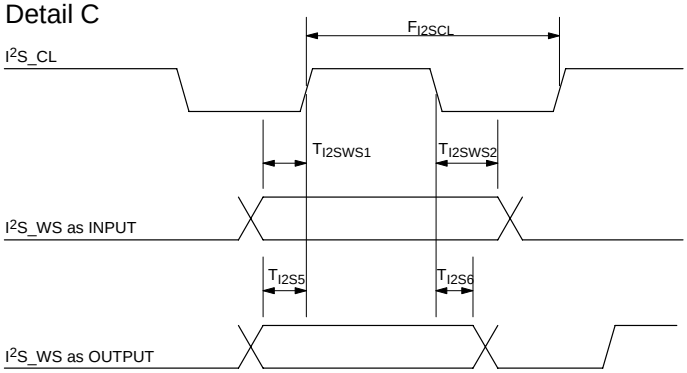
3. I2S_CL:
Gives the timing for the transmission of I^2S serial data (1.024 MHz).

4. I2S_WS:
The I2S_WS word strobe line defines the left and right sample.

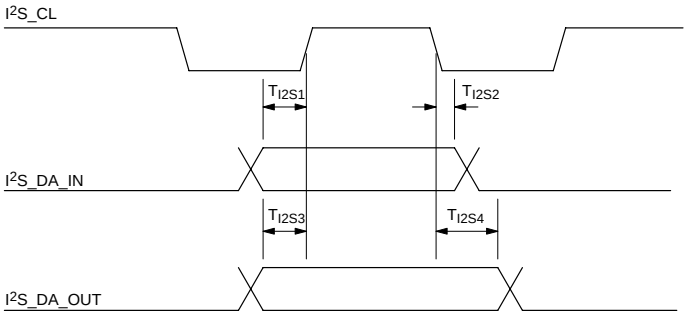
6.1. I²S Bus Timing Diagram



Detail C



Detail A,B



7. Power-up Sequence

The reset pin should not be high (>0.45 DVSUP, see recommended operation conditions) before the 5 Volt digital powersupply (DVSUP) is >4.75 Volt **and** the DPL-Clock is running (Delay: 1 ms max, 0.5 ms typ.).

This means, if the reset low-high edge starts with a delay of 2 ms after DVSUP>4.75 Volt, even under worst case conditions, the reset is ok.

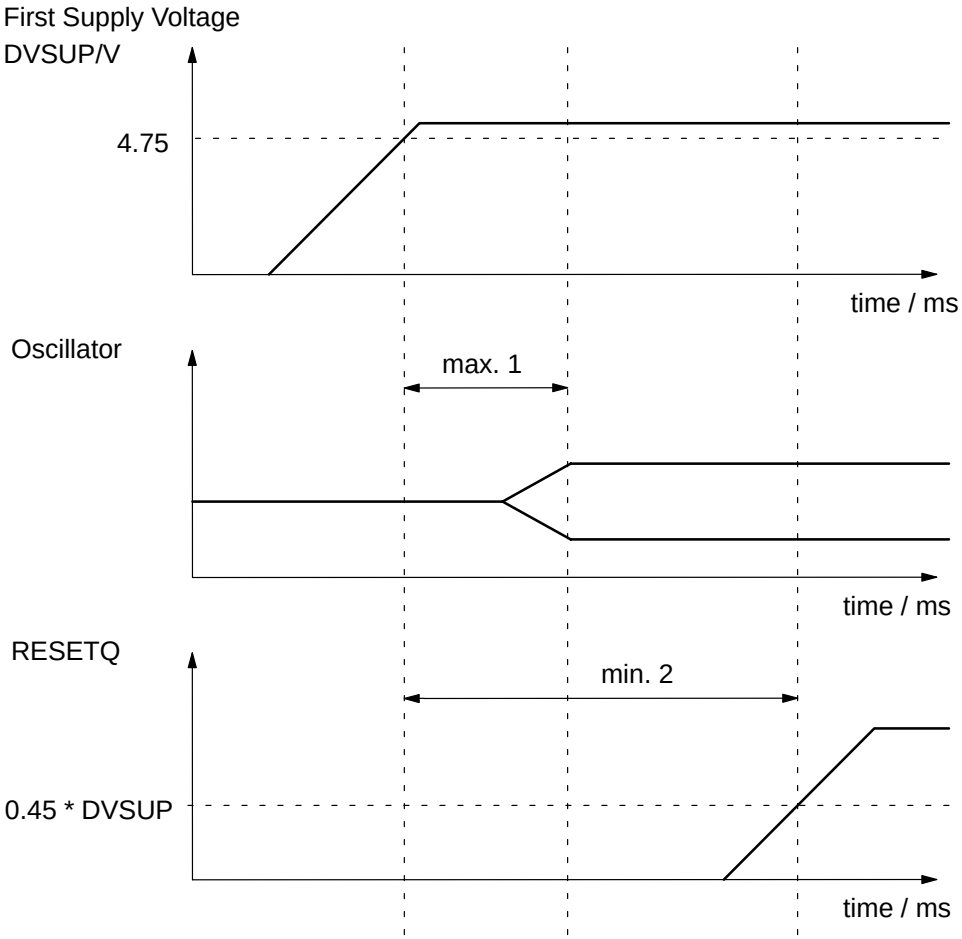


Fig. 7–1: Power-up sequence

8. Programming the Mode Register

All transmissions on the control bus are 16 bits wide.

Table 8–1: DPL mode register

Register	Write Address (hex)	Function
MODE_REG	0083	mode register

The register ‘MODE_REG’ contains the control bits determining the operation mode of the DPL; Table 8–2 explains all bit positions.

Table 8–2: Control word ‘MODE_REG’

MODE_REG 0083_{hex}					
Bit	**Function**	**Comment**	**Definition**	**Reset condition**	**Recommendation**
[0]	not used			0	0
[1]	DCTR_TRI	Digital control IO 0/1 tristate	0 : active 1 : tristate	1	0
[2]	I2S_TRI	I^2S outputs tristate (I2S_CL, I2S_WS, I2S_DA_OUT)	0 : active 1 : tristate	1	0
[3]	I2S_MODE	Master/Slave mode of the I^2S-bus	0 : Master 1 : Slave	1	X
[4]	I2S_WS_MODE	WS due to the Sony or Philips-Format	0 : Sony 1 : Philips	0	X
[5]	AUDIO_CL_OUT	Switch Audio_Clock_Output to tristate	0 : on 1 : tristate	0	X
[15:6]	not used			0	0

9. Programming the DSP Part

9.1. Summary of the DSP Control Registers

Control registers are 16 bits wide. Transmissions via I^2C-bus have to take place in 16-bit words. Single data entries are 8-bit. Some of the defined 16-bit words are divided into low and high byte, thus holding two different control entities. All control registers are readable.

Note: Unused parts of the 16-bit registers must be zero.

Table 9–1: Summary of the DSP Control Registers

Name	I^2C Bus Address	High /Low	Adjustable Range, Operational Modes	Reset Mode	Valid for
Standard MSP like Control Registers					
Volume channel 1	0000_{hex}	H	[+12 dB ... –114 dB, MUTE]	MUTE	19/20
Volume / Mode channel 1		L	1/8 dB Steps, Reduce Volume / Tone Control	00_{hex}	19/20
Balance channel 1 [L/R]	0001_{hex}	H	[0..100 / 100 % and vv][–127..0 / 0 dB and vv]	100%/100%	19/20
Balance Mode channel 1		L	[Linear mode / logarithmic mode]	linear mode	19/20
Bass channel 1	0002_{hex}	H	[+20 dB ... –12 dB]	0 dB	19/20
Treble channel 1	0003_{hex}	H	[+15 dB ... –12 dB]	0 dB	19/20
Loudness channel 1	0004_{hex}	H	[0 dB ... +17 dB]	0 dB	19/20
Loudness Filter Characteristic		L	[NORMAL, SUPER_BASS]	NORMAL	19/20
Spatial effect strength channel 1	0005_{hex}	H	[–100%...OFF...+100%]	OFF	19/20
Spatial effect mode/customize		L	[SBE, SBE+PSE]	SBE+PSE	19/20
Volume channel 2	0006_{hex}	H	[+12 dB ... –114 dB, MUTE]	MUTE	19/20
Volume / Mode channel 2		L	1/8 dB Steps, Reduce Volume / Tone Control	00_{hex}	19/20
Volume SCART channel	0007_{hex}	H	[00_{hex} ... $7F_{hex}$],[+12 dB ... –114 dB, MUTE]	00_{hex}	19/20
Volume / Mode SCART channel		L	[Linear mode / logarithmic mode]	linear mode	19/20
Channel 1 source	0008_{hex}	H	[SCART, DOLBYLR, DOLBYCS, DOLBYCSUB, I2S1, I2S2]	00_{hex} (undefined source)	19/20
Channel 1 matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	19/20
Channel 2 source	0009_{hex}	H	[SCART, DOLBYLR, DOLBYCS, DOLBYCSUB, I2S1, I2S2]	00_{hex} (undefined source)	19/20
Channel 2 matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	19/20
SCART channel source	$000a_{hex}$	H	[SCART, DOLBYLR, DOLBYCS, DOLBYCSUB, I2S1, I2S2]	00_{hex} (undefined source)	19/20
SCART channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	19/20
I^2S1 channel source	$000b_{hex}$	H	[SCART, DOLBYLR, DOLBYCS, DOLBYCSUB, I2S1, I2S2]	00_{hex} (undefined source)	all
I^2S1 channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	all
Quasi-peak detector source	$000c_{hex}$	H	[SCART, DOLBYLR, DOLBYCS, DOLBYCSUB, I2S1, I2S2]	00_{hex} (undefined source)	all

Name	I²C Bus Address	High /Low	Adjustable Range, Operational Modes	Reset Mode	Valid for
Quasi-peak detector matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	all
Prescale SCART	$000d_{hex}$	H	[00_{hex} ... $7F_{hex}$]	00_{hex}	20
Prescale I²S2	0012_{hex}	H	[00_{hex} ... $7F_{hex}$]	10_{hex}	all
ACB Register (SCART Switches and DIG_OUT Pins)	0013_{hex}	H	Bits [7..0]	00_{hex}	19/20
Beeper	0014_{hex}	H/L	[00_{hex} ... $7F_{hex}$]/[00_{hex} ... $7F_{hex}$]	0/0	19/20
Prescale I²S1	0016_{hex}	H	[00_{hex} ... $7F_{hex}$]	10_{hex}	all
Mode Tone Control*)	0020_{hex}	H	[BASS/TREBLE, EQUALIZER]	BASS/TREB	19(/20)*)
Equalizer channel 1 band 1*)	0021_{hex}	H	[+12 dB ... −12 dB]	0dB	19(/20)*)
Equalizer channel 1 band 2*)	0022_{hex}	H	[+12 dB ... −12 dB]	0dB	19(/20)*)
Equalizer channel 1 band 3*)	0023_{hex}	H	[+12 dB ... −12 dB]	0dB	19(/20)*)
Equalizer channel 1 band 4*)	0024_{hex}	H	[+12 dB ... −12 dB]	0dB	19(/20)*)
Equalizer channel 1 band 5*)	0025_{hex}	H	[+12 dB ... −12 dB]	0dB	19(/20)*)
Balance channel 2 [L/R]	0030_{hex}	H	[0...100 / 100% and vv][–127...0 / 0 dB and vv]	100%/100%	19/20
Balance Mode channel 2		L	[Linear mode / logarithmic mode]	linear mode	19/20
Bass channel 2	0031_{hex}	H	[+20 dB ... –12 dB]	0 dB	19/20
Treble channel 2	0032_{hex}	H	[+15 dB ... –12 dB]	0 dB	19/20
Loudness channel 2	0033_{hex}	H	[0 dB ... +17 dB]	0 dB	19/20
Loudness filter characteristic		L	[NORMAL, SUPER_BASS]	NORMAL	19/20
I²S2 channel source	0038_{hex}	H	[SCART, DOLBYLR, DOLBYCS, DOLBYCSUB, I2S1, I2S2]	00_{hex} (undefined source)	all
I²S2 channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	all
Surround Processing Control Registers					
Surround decoder mode	0040_{hex}	H	[ADAPTIVE, PASSIVE, EFFECT]	ADAPTIVE	all
Surround reproduction mode		L	[NORMAL, PHANTOM, WIDE, DOLBY_3_STEREO, CENTER_OFF, PANORAMA]	NORMAL	all
Surround source	0041_{hex}	H	[SCART, I2S1, I2S2, NOISE]	00_{hex} (undefined source)	all
Surround source matrix		L	[SOUNDA, SOUNDB, STEREO, NOISEL, NOISER, NOISEC, NOISES]	SOUNDA	all
Surround delay	0042_{hex}	H	[0..31 ms]	0	all
Surround input balance control	0043_{hex}	H	[−12..+12 dB]	0	all
Input balance mode	0043_{hex}	L	[AUTOMATIC, MANUAL]	AUTOMATIC	all
Surround spatial effect	0044_{hex}	H	[0..100%]	00_{hex}	all
Panorama sound effect	0045_{hex}	H	[0..100%]	00_{hex}	all
Surround reverberation	0046_{hex}	H	[0..100%]	00_{hex}	all

*) Equalizing function only for SOUNDA (=Center) possible. Equalizer and AD input cannot work simultaneously. In the DPL 3520A the equalizer can only be used in coprocessor mode (input via I²C and not via AD converter).

9.1.1. Volume Channel 1 and Channel 2

Volume Channel 1	**0000_{hex} (DPL 3519/20)**	**11 MSBs**
Volume Channel 2	**0006_{hex} (DPL 3519/20)**	**11 MSBs**
+12 dB	0111 1111 000x	$7F0_{hex}$
+11.875 dB	0111 1110 111x	$7EE_{hex}$
+0.125 dB	0111 0011 001x	732_{hex}
0 dB	0111 0011 000x	730_{hex}
–0.125 dB	0111 0010 111x	$72E_{hex}$
–114.125 dB	0000 0001 001x	012_{hex}
–114 dB	0000 0001 000x	010_{hex}
Mute	0000 0000 xxxx RESET	$00x_{hex}$
Fast Mute	1111 1111 111x	FFE_{hex}

The highest given positive 11-bit number ($7F0_{hex}$) yields in a maximum possible gain of 12 dB. Decreasing the volume register by 1 LSB decreases the volume by 0.125 dB. Volume settings lower than the given minimum mute the output. With large scale input signals, positive volume settings may lead to signal clipping.

With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. Going back from Fast Mute should be done to the volume step before Fast Mute was activated.

Clipping Mode Channel 1	**0000_{hex} (DPL 3519/20)**	**3 LSBs**
Clipping Mode Channel 2	**0006_{hex} (DPL 3519/20)**	**3 LSBs**
Reduce Volume	x000 RESET	0_{hex}
Reduce Tone Control	x001	1_{hex}
Compromise Mode	x010	2_{hex}

If the clipping mode is set to “Reduce Volume”, the following clipping procedure is used: To prevent severe clipping effects with bass, treble, or equalizer boosts, the internal volume is automatically limited to a level where, in combination with either bass, treble, or equalizer setting, the amplification does not exceed 12 dB.

If the clipping mode is “Reduce Tone Control”, the bass or treble value is reduced if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced, where amplification together with volume exceeds 12 dB.

If the clipping mode is “Compromise Mode”, the bass or treble value and volume are both reduced by half, if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced by half, where amplification together with volume exceeds 12 dB.

Example:	**Vol.: +6 dB**	**Bass: +9 dB**	**Treble: +5 dB**
Reduce Volume	3	9	5
Reduce Tone Control	6	6	5
Compromise	4.5	7.5	5

9.1.2. Balance Channel 1 and Channel 2

Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected. In linear mode, a step by 1 LSB decreases or increases the balance by about 0.8% (exact figure: 100/127). In logarithmic mode, a step by 1 LSB decreases or increases the balance by 1 dB.

Balance Mode Channel 1	**0001_{hex} (DPL 3519/20)**	**LSB**
Balance Mode Channel 2	**0030_{hex} (DPL 3519/20)**	**LSB**
linear	xxx0 RESET	0_{hex}
logarithmic	xxx1	1_{hex}

Balance Channel 1 [L/R]	**0001_{hex} (DPL 3519/20)**	**H**
Balance Channel 2 [L/R]	**0030_{hex} (DPL 3519/20)**	**H**
Left muted, Right 100%	0111 1111	$7F_{hex}$
Left 0.8%, Right 100%	0111 1110	$7E_{hex}$
Left 99.2%, Right 100%	0000 0001	01_{hex}
Left 100%, Right 100%	0000 0000 RESET	00_{hex}
Left 100%, Right 99.2%	1111 1111	FF_{hex}
Left 100%, Right 0.8%	1000 0010	82_{hex}
Left 100%, Right muted	1000 0001	81_{hex}

Balance Channel 1 [L/R]	**0001_{hex} (DPL 3519/20)**	**H**
Balance Channel 2 [L/R]	**0030_{hex} (DPL 3519/20)**	**H**
Left –127 dB, Right 0 dB	0111 1111	$7F_{hex}$
Left –126 dB, Right 0 dB	0111 1110	$7E_{hex}$
Left –1 dB, Right 0 dB	0000 0001	01_{hex}
Left 0 dB, Right 0 dB	0000 0000 RESET	00_{hex}
Left 0 dB, Right –1 dB	1111 1111	FF_{hex}
Left 0 dB, Right –127 dB	1000 0001	81_{hex}
Left 0 dB, Right –128 dB	1000 0000	80_{hex}

9.1.3. Bass Channel 1 and Channel 2

Bass Channel 1	**0002_{hex} (DPL 3519/20)**	**H**
Bass Channel 2	**0031_{hex} (DPL 3519/20)**	**H**
+20 dB	0111 1111	$7F_{hex}$
+18 dB	0111 1000	78_{hex}
+16 dB	0111 0000	70_{hex}
+14 dB	0110 1000	68_{hex}
+12 dB	0110 0000	60_{hex}
+11 dB	0101 1000	58_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive bass settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain.

Loudspeaker channel: Bass and Equalizer cannot work simultaneously (see Table: Mode Tone Control). If Equalizer is used, Bass and Treble coefficients must be set to zero and vice versa.

9.1.4. Treble Channel 1 and Channel 2

Treble Channel 1	**0003_{hex} (DPL 3519/20)** **H**	
Treble Channel 2	**0032_{hex} (DPL 3519/20)** **H**	
+15 dB	0111 1000	78_{hex}
+14 dB	0111 0000	70_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive treble settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set treble to a value that, in conjunction with volume, would result in an overall positive gain.

Loudspeaker channel: Treble and Equalizer cannot work simultaneously (see Table: Mode Tone Control). If Equalizer is used, Bass and Treble coefficients must be set to zero and vice versa.

9.1.5. Loudness Channel 1 and Channel 2

Loudness Channel 1	**0004_{hex} (DPL 3519/20)** **H**	
Loudness Channel 2	**0033_{hex} (DPL 3519/20)** **H**	
+17 dB	0100 0100	44_{hex}
+16 dB	0100 0000	40_{hex}
+1 dB	0000 0100	04_{hex}
0 dB	0000 0000 RESET	00_{hex}

Mode Loudness Channel 1	**0004_{hex} (DPL 3519/20)** **L**	
Mode Loudness Channel 2	**0033_{hex} (DPL 3519/20)** **L**	
Normal (constant volume at 1 kHz)	0000 0000 RESET	00_{hex}
Super Bass (constant volume at 2 kHz)	0000 0100	04_{hex}

Loudness increases the volume of low and high frequency signals, while keeping the amplitude of the 1 kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain.

By means of ‘Mode Loudness’, the corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.

9.1.6. Spatial Effects Channel 1

Spatial Effect Strength Channel 1	**0005_{hex} (DPL 3519/20)** **H**
Enlargement 100%	0111 1111 $7F_{hex}$
Enlargement 50%	0011 1111 $3F_{hex}$
Enlargement 1.5%	0000 0001 01_{hex}
Effect off	0000 0000 RESET 00_{hex}
Reduction 1.5%	1111 1111 FF_{hex}
Reduction 50%	1100 0000 $C0_{hex}$
Reduction 100%	1000 0000 80_{hex}

Spatial Effect Mode Channel 1	**0005_{hex} (H nibble) (DPL 3519/20)** **L**
Stereo Basewidth Enlargement (SBE) and Pseudo Stereo Effect (PSE). (Mode A)	0000 RESET 0_{hex} 0000 0_{hex}
Stereo Basewidth Enlargement (SBE) only. (Mode B)	0010 2_{hex}

Spatial Effect Customize Coefficient Channel 1	**0005_{hex} (L nibble) (DPL 3519/20)** **L**
max high pass gain	0000 RESET 0_{hex}
2/3 high pass gain	0010 2_{hex}
1/3 high pass gain	0100 4_{hex}
min. high pass gain	0110 6_{hex}
automatic	1000 8_{hex}

There are several spatial effect modes available:

Mode A (low byte = 00_{hex}) is compatible to the formerly used spatial effect. Here, the kind of spatial effect depends on the source mode. If the incoming signal is in mono mode, Pseudo Stereo Effect is active; for stereo signals, Pseudo Stereo Effect and Stereo Basewidth Enlargement is effective. The strength of the effect is controllable by the upper byte. A negative value reduces the stereo image. A rather strong spatial effect is recommended for small TV sets where loudspeaker spacing is rather close. For large-screen TV sets, a more moderate spatial effect is recommended. In mode A, even in case of stereo input signals, Pseudo Stereo Effect is active, which reduces the center image.

In Mode B, only Stereo Basewidth Enlargement is effective. For mono input signals, the Pseudo Stereo Effect has to be switched on.

It is worth mentioning that all spatial effects affect amplitude and phase response. With the lower 4 bits, the frequency response can be customized. A value of 0000_{bin} yields a flat response for center signals (L = R) but a high pass function of L or R only signals. A value of 0110_{bin} has a flat response for L or R only signals but a lowpass function for center signals. By using 1000_{bin}, the frequency response is automatically adapted to the sound material by choosing an optimal high pass gain.

9.1.7. Volume SCART Channel

Linear Mode	
Volume SCART	**0007_{hex} H (DPL 3519/20)**
OFF	0000 0000 RESET 00_{hex}
0 dB gain (digital full scale (FS) to 2 V_{RMS} output)	0100 0000 40_{hex}
+6 dB gain (–6 dBFS to 2 V_{RMS} output)	0111 1111 $7F_{hex}$

Logarithmic Mode	
Volume SCART	**0007_{hex} 11 MSBs (DPL 3519/20)**
+12 dB	0111 1111 000x $7F0_{hex}$
+11.875 dB	0111 1110 111x $7EE_{hex}$
+0.125 dB	0111 0011 001x 732_{hex}
0 dB	0111 0011 000x 730_{hex}
–0.125 dB	0111 0010 111x $72E_{hex}$
–114.125 dB	0000 0001 001x 012_{hex}
–114 dB	0000 0001 000x 010_{hex}
Mute	0000 0000 0000 RESET 000_{hex}

Volume Mode SCART	**0007_{hex} LSB (DPL 3519/20)**
linear	xxx0 RESET 0_{hex}
logarithmic	xxx1 1_{hex}

9.1.8. Channel Source Modes

Channel 1 source	**0008_{hex} H (DPL 3519/20)**
Channel 2 source	**0009_{hex} H (DPL 3519/20)**
SCART source	**$000a_{hex}$ H (DPL 3519/20)**
I^2S1 source	**$000b_{hex}$ H (DPL 3518/19/20)**
I^2S2 source	**0038_{hex} H (DPL 3518/19/20)**
Quasi-peak detector source	**$000c_{hex}$ H (DPL 3518/19/20)**
SCART (20)	0000 0010 02_{hex}
DOLBYLR (18/19/20)	0000 0011 03_{hex}
DOLBYCS (18/19/20)	0000 0100 04_{hex}
I2S1 (18/19/20)	0000 0101 05_{hex}
I2S2 (18/19/20)	0000 0110 06_{hex}
DOLBYCSUB (18/19/20)	0000 0111 07_{hex}

DOLBYLR denotes a signal pair consisting of surround decoder output for the left and right loudspeakers. The signal content depends on the used surround reproduction mode. DOLBYCS is the signal pair for the center and surround information (if there is any, depending on the surround reproduction mode). DOLBYCSUB is a signal pair consisting of the center information and a subwoofer channel. The subwoofer channel is the sum of all low frequency components (fg=100Hz) of the L, R and C channels.

The I^2S2 source must not be 00_{hex}. It should be one of the mentioned values, otherwise the SCART source will not work properly.

If the equalizer is switched on, SCART as source is no longer valid, i.e. AD input is no longer possible.

9.1.9. Channel Matrix Modes

Channel 1 matrix	**0008_{hex} (DPL 3519/20)**	**L**
Channel 2 matrix	**0009_{hex} (DPL 3519/20)**	**L**
SCART matrix	**$000a_{hex}$ (DPL 3519/20)**	**L**
I^2S1 matrix	**$000b_{hex}$ (DPL 3518/19/20)**	**L**
I^2S2 matrix	**0038_{hex} (DPL 3518/19/20)**	**L**
Quasi-peak detector matrix	**$000c_{hex}$ (DPL 3518/19/20)**	**L**
SOUNDA, LEFT or CENTER	0000 0000 RESET	00_{hex}
SOUNDB, RIGHT, SURROUND or SUB-WOOFER	0001 0000	10_{hex}
STEREO	0010 0000	20_{hex}
MONO	0011 0000	30_{hex}
SUM/DIFF	0100 0000	40_{hex}
AB_XCHANGE	0101 0000	50_{hex}
PHASE_CHANGE_B	0110 0000	60_{hex}
PHASE_CHANGE_A	0111 0000	70_{hex}
A_ONLY	1000 0000	80_{hex}
B_ONLY	1001 0000	90_{hex}
INV_STEREO	1111 0000	$F0_{hex}$

The sum/difference mode can be used together with the quasi-peak detector to determine the sound material mode. If the difference signal on channel B (right) is near to zero, and the sum signal on channel A (left) is high, the incoming audio signal is mono. If there is a significant level on the difference signal, the incoming audio is stereo.

The inv_stereo mode can be used to phase invert outputs via the I^2S interfaces. This gives the option to correct phase relations with outputs of attached processors.

9.1.10. SCART Prescale

Volume Prescale SCART	**$000d_{hex}$ (DPL 3520)**	**H**
OFF	0000 0000 RESET	00_{hex}
0 dB gain (2 V_{RMS} input to digital full scale)	0001 1001	19_{hex}
+14 dB gain (400 mV_{RMS} input to digital full scale)	0111 1111	$7F_{hex}$

9.1.11. I^2S1 and I^2S2 Prescale

Volume Prescale I^2S1	**0016_{hex} H (DPL 3518/19/20)**
Volume Prescale I^2S2	**0012_{hex} H (DPL 3518/19/20)**
OFF	00_{hex}
0 dB gain	10_{hex} RESET
+18 dB gain	$7F_{hex}$

9.1.12. ACB Register, Definition of the SCART-Switches and DIG_CTR_OUT Pins

ACB Register	0013_{hex} H (DPL 3519/20)	
DFP In Selection		
SCART1_IN	xxxx xx00	RESET
MONO_IN	xxxx xx01	
SCART2_IN	xxxx xx10	
SCART3_IN	xxxx xx11	
SCART1_OUT Selection		
SCART3_IN	xxxx 00xx	RESET
SCART2_IN	xxxx 01xx	
MONO_IN	xxxx 10xx	
DA_SCART	xxxx 11xx	
SCART2_OUT Selection		
DA_SCART	xx00 xxxx	RESET
SCART1_IN	xx01 xxxx	
MONO_IN	xx10 xxxx	
DIG_CTR_OUT1		
low	x0xx xxxx	RESET
high	x1xx xxxx	
DIG_CTR_OUT2		
low	0xxx xxxx	RESET
high	1xxx xxxx	
RESET: The RESET state is taken at the time of the first write transmission on the control bus to the audio processing part (DFP). By writing to the ACB register first, the RESET state can be redefined.		

9.1.13. Beeper

Beeper Volume	0014_{hex} H (DPL 3519/20)	
OFF	0000 0000 RESET	00_{hex}
Maximum Volume (full digital scale FDS)	0111 1111	$7F_{hex}$

Beeper Frequency	0014_{hex} L (DPL 3519/20)	
16 Hz (lowest)	0000 0001	01_{hex}
1 kHz	0100 0000	40_{hex}
4 kHz (highest)	1111 1111	FF_{hex}

A squarewave beeper can be added to the loudspeaker channel and the headphone channel. The addition point is just before loudness and volume adjustment.

9.1.14. Mode Tone Control

Mode Tone Control	00020_{hex} H (DPL 3519/20)	
Bass and Treble	0000 0000 RESET	00_{hex}
Equalizer	1111 1111	FF_{hex}

By means of ‘Mode Tone Control’, Bass/Treble or Equalizer may be activated.

The Equalizer must also not be used simultaneously with AD input (Source mode = SCART).

9.1.15. Equalizer Channel 1

Band 1 1 (below 120 Hz)	**00021_{hex} H (DPL 3519)**
Band 2 (center: 500 Hz)	**00022_{hex} H (DPL 3519)**
Band 3 (center: 1500 Hz)	**00023_{hex} H (DPL 3519)**
Band 4 (center: 5000 Hz)	**00024_{hex} H (DPL 3519)**
Band 5 (above 10000 Hz)	**00025_{hex} H (DPL 3519)**
+12 dB	0110 0000 60_{hex}
+11 dB	0101 1000 58_{hex}
+1 dB	0000 1000 08_{hex}
+1/8 dB	0000 0001 01_{hex}
0 dB	0000 0000 00_{hex} RESET
–1/8 dB	1111 1111 FF_{hex}
–1 dB	1111 1000 $F8_{hex}$
–11dB	1010 1000 $A8_{hex}$
–12 dB	1010 0000 $A0_{hex}$

With positive equalizer settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set Equalizer bands to a value that, in conjunction with volume, would result in an overall positive gain.

The Equalizer must not be used simultaneously with Bass and Treble (Mode Tone Control must be set to FF to use the Equalizer). If Bass and Treble are used, Equalizer coefficients must be set to zero.

The Equalizer must also not be used simultaneously with AD input (Source mode = SCART).

9.1.16. Surround Decoder Modes

Surround Decoder Modes	**0040_{hex} H (DPL 3518/19/20)**
ADAPTIVE (Dolby Pro Logic)	0000 0000 00_{hex} RESET
PASSIVE	0001 0000 10_{hex}
EFFECT	0010 0000 20_{hex}

The surround decoder mode specifies which method is being used to create four output channels out of two input channels. For Dolby Pro Logic operation the matrix must be switched to ADAPTIVE. Even sound material not encoded in Dolby Surround will produce good surround effects in this mode. All surround reproduction modes can be used together with the ADAPTIVE mode. The PASSIVE mode should only be used together with WIDE mode. The EFFECT mode is intended to get surround effects even in case of mono transmissions (Note: For mono signals, Dolby Pro Logic will only reproduce signals via the center channel. All other channels will be muted). For a more detailed description see section 10.2. “Useful combinations of the surround decoder and reproduction modes”.

9.1.17. Surround Reproduction Modes

Surround Reproduction Modes	0040_{hex} L (DPL 3518/19/20)
NORMAL	0000 0000 00_{hex} RESET
PHANTOM	0001 0000 10_{hex}
WIDE	0010 0000 20_{hex}
THREE_CHANNEL	0011 0000 30_{hex}
CENTER_OFF	0100 0000 40_{hex}
PANORAMA	0101 0000 50_{hex}

The standard mode to reproduce Dolby Pro Logic Surround is NORMAL. All four channels L, C, R, S are in operation. Low Frequency signals of the C channel are distributed to the L and R loudspeakers. This enables the center speaker to be a smaller model than the L and R speaker. If all three front speakers are identical and capable of reproducing low bass information, and if equal power is available in the L, C and R amplifiers, then it may be beneficial to use the WIDE mode. The center channel will then contain the full frequency range signal. The NORMAL and WIDE modes using 4 or 5 loudspeakers give the optimum solution for surround reproduction. Other modes using less loudspeakers create inferior surround effects.

If no center speaker is available, the PHANTOM mode prevents loss of the center information by splitting it up equally to the L and R speakers.

If no surround speaker is available the THREE_CHANNEL mode can be used. This mode will confine the sound to the front speakers.

The CENTER_OFF mode provides a simple way to optimize the manual input balance. While switched off, the balance control can be adjusted for minimum dialogue level.

Surround sound can be reproduced to a certain extent even with two loudspeakers. The PANORAMA mode mixes all four surround decoder outputs to the L and R output channel without any loss of information.

9.1.18. Surround Source Modes

Surround Source Modes		0041_{hex} H (DPL 3518/19/20)
NOISE	(18/19/20)	0000 0001 01_{hex}
SCART	(20)	0000 0010 02_{hex}
I2S1	(18/19/20)	0000 0101 05_{hex}
I2S2	(18/19/20)	0000 0110 06_{hex}

Select the source to be fed to the surround decoder block. The NOISE mode selects a built-in noise generator. If the equalizer is switched on, SCART as source is no longer valid, i.e. AD input is no longer possible.

9.1.19. Surround Source Matrix Modes

Surround Source Matrix (Sound Source)	0041_{hex} L (DPL 3518/19/20)
SOUNDA	0000 0000 00_{hex} RESET
SOUNDB	0001 0000 10_{hex}
STEREO	0010 0000 20_{hex}
MONO	0011 0000 30_{hex}
Surround Source Matrix (Noise Source)	**0041_{hex} L (DPL 3518/19/20)**
NOISE_L	1010 0000 $a0_{hex}$
NOISE_C	1011 0000 $b0_{hex}$
NOISE_R	1100 0000 $c0_{hex}$
NOISE_S	1101 0000 $d0_{hex}$

Select the mode of the sound source. Real Dolby Pro Logic Surround sound can only be displayed in the STEREO mode. Mono modes such as SOUNDA, SOUNDB and MONO will not produce a surround effect unless the surround decoder mode is switched to EFFECT.

If the equalizer is switched on, the SCART source mode is no longer valid.

The modes NOISE_L, NOISE_C, NOISE_R and NOISE_S create an input signal to the decoder that will result in a noise signal on the L, C, R and S outputs.

9.1.20. Surround Delay

Surround Delay	0042_{hex} H (DPL 3518/19/20)	
5 ms (lowest)	0000 0101	05_{hex}
6 ms	0000 0110	06_{hex}
31 ms (highest)	0001 1111	$1F_{hex}$

For Dolby Pro Logic designs, only 20 ms fixed or 15–30 ms variable delay must be used.

9.1.21. Surround Manual Input Balance

Surround Manual Input Balance	0043_{hex} H (DPL 3518/19/20)	
Left muted, Right 100%	0111 1111	$7F_{hex}$
Left 0.8%, Right 100%	0111 1110	$7E_{hex}$
Left 99.2%, Right 100%	0000 0001	01_{hex}
Left 100%, Right 100%	0000 0000 RESET	00_{hex}
Left 100%, Right 99.2%	1111 1111	FF_{hex}
Left 100%, Right 0.8%	1000 0010	82_{hex}
Left 100%, Right muted	1000 0001	81_{hex}

In automatic balance mode this register has no effect.

9.1.22. Surround Input Balance Mode

Surround Input Balance Mode	0043_{hex} L (DPL 3518/19/20)	
Automatic balance	0000 0000	00_{hex}
Manual balance	0100 0000	40_{hex}

Automatic balance mode is recommended.

9.1.23. Surround Spatial Effect

Surround Spatial Effect	0044_{hex} H (DPL 3518/19/20)	
OFF	0000 0000 RESET	00_{hex}
0.8%	0000 0001	01_{hex}
99.2%	0111 1110	$7E_{hex}$
100%	1111 1111	$7F_{hex}$

Increases the perceived basewidth of the reproduced left and right front channels. Recommended value: 50% = 40_{hex}. In contrast to the spatial effect for channel 1, the surround spatial effect is optimized for Dolby Pro Logic. The difference is most obvious for the Phantom and Panorama reproduction modes.

9.1.24. Panorama Sound Effect

Panorama Sound Effect	0045_{hex} H (DPL 3518/19/20)	
OFF	0000 0000 RESET	00_{hex}
0.8%	0000 0001	01_{hex}
99.2%	0111 1110	$7E_{hex}$
100%	0111 1111	$7F_{hex}$

Strength of the surround effect in PANORAMA mode. Recommended value: 66% = 54_{hex}. Delay should be set to the max. value: 31 ms and reverberation should be off. This register only has the correct effect in PANORAMA mode (Surround Reproduction Mode is set to PANORAMA). It must be zero (OFF) in non PANORAMA modes)

9.1.25. Surround Reverberation

Surround Reverberation	0046_{hex} H (DPL 3518/19/20)	
OFF	0000 0000 RESET	00_{hex}
0.8%	0000 0001	01_{hex}
99.2%	0111 1110	$7E_{hex}$
100%	0111 1111	$7F_{hex}$

Reverberation will be added to the surround channel. Due to the maximally implemented 31 ms only dry sounds will be affected. The effect will be rather weak for source material which already contains a certain amount of reverberation. It can be used to create a more reverberant sound when using the EFFECT decoder mode for mono signals. Recommended value: not more than 66% = 54_{hex}. Delay should be set to the maximum value: 31 ms.

9.2. Summary of Readable Registers

All readable registers are 16-bit wide. Transmissions via I^2C-bus have to take place in 16-bit words.

These registers are not writable.

Name	Address	High/Low	Output Range	
Digital input level register	0018_{hex}	H		single bits
Quasi peak readout left	0019_{hex}	H&L	[00_{hex} ... $7FFF_{hex}$]	16-bit two's complement
Quasi peak readout right	$001a_{hex}$	H&L	[00_{hex} ... $7FFF_{hex}$]	16-bit two's complement

9.2.1. Quasi Peak Detector

Quasi peak readout left	**0019_{hex} H+L (DPL 3518/19/20)**
Quasi peak readout right	**$001a_{hex}$ H+L (DPL 3518/19/20)**
Quasi peak readout	[0_{hex} ... $7FFF_{hex}$] values are 16-bit two's complement

The quasi peak readout register can be used to read out the quasi peak level of any input source, in order to adjust all inputs to the same normal listening level. The refresh rate is 32 kHz. The feature is based on a filter time constant:

attack-time: 1.3 ms
decay-time: 37 ms

9.2.2. Digital Input Level Register

Used to read back the input level of certain digital input pins:

Pin	Bit
D_CTR_IN	X––– ––––
D_CTR_IO1	–X–– ––––
D_CTR_IO0	––X– ––––

A high level on the input pins gives a "1", a low level gives "0".

10. Further Explanations and Application Hints

10.1. Overview of the Surround Decoder and Reproductions Modes

The register 0040hex H ”surround decoder modes” define which method should be used to create a multichannel signal out of an stereo input.

The register 0040hex L ”sound reproduction modes” define which method should be used to mix the multichannel output to the actually used loudspeakers (or final output channels).

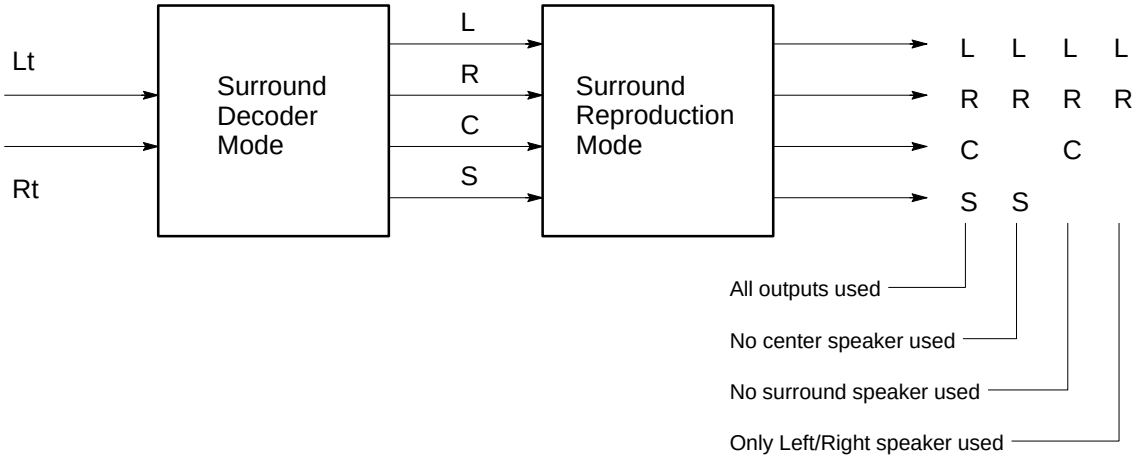


Fig. 10–1: Surround Decoder and Reproduction Mode Principle

The PANORAMA sound reproduction mode mixes all 4 channels into 2 output channels. Fig 10–2 gives the internal processing of this mode. All other reproduction modes are according to the Dolby specification.

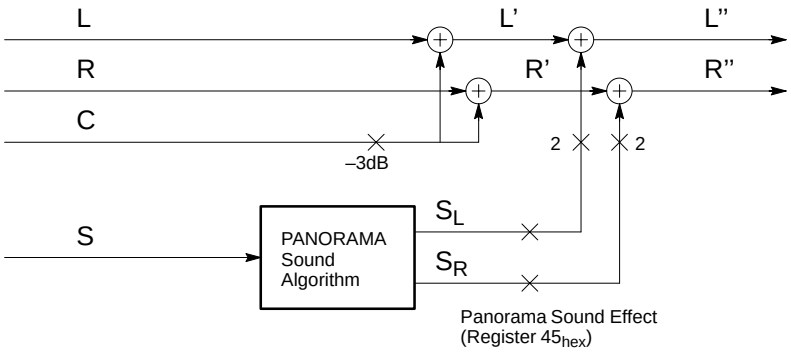


Fig. 10–2: Surround Spatial Effect and PANORAMA Sound Processing

10.2. Useful Combinations of the Surround Decoder and Reproduction Modes

In principle, the ”surround decoder modes” and the ”sound reproduction modes” modes could be orthogonal (all ”surround decoder modes” can be used with all ”sound reproduction modes”) but there are some combinations that do not create ”good” sound.

10.2.1. Useful Combinations with the ADAPTIVE Surround Decoder Mode

NORMAL	all output channels used, L and R speakers have better bass capability
WIDE	all output channels used, L,R and C speakers all have good bass capability
PHANTOM	no center speaker used (note: the center output channel C is muted automatically)
THREE_CHANNEL	no surround speaker used (creates a STEREO like effect, but with better center stage reproduction) (Note: the surround output channel is not automatically muted)
CENTER_OFF	systems with center speaker, only for adjustment of manual input balance. (Note: Dolby suggests to use the adaptive input balance always)
PANORAMA	only L and R speaker used (creates a surround like effect with only 2 speakers) (Note: the left and right output channels L&R are not muted automatically)

10.2.2. Useful Combinations with the PASSIVE Surround Decoder Mode

The passive surround decoder (which is defined by Dolby) uses no center speaker! In no cases, a center speaker should be connected to the output (or if, the center speaker should be muted). Only two modes are useful (all other modes give inferior results!):

WIDE	L, R and S speakers used. Do not connect speakers to the center channel
PANORAMA	only L and R speaker used (creates a surround like effect with only 2 speakers, result is inferior to the combination with the ADAPTIVE mode)

10.2.3. Useful Combinations with the EFFECT Surround Decoder Mode

The EFFECT surround decoder mode is intended for MONO sources. MONO sources give no surround effect in the ADAPTIVE and PASSIVE modes. In order to give the customer means to create surround sound even in presence of mono signals, the EFFECT mode can be used.

NORMAL	all output channels used, L and R speakers have better bass capability. The center channel may need a lower volume to compensate for the dominant center.
WIDE	all output channels used, L,R and C speakers all have better bass capability. The center channel may need a lower volume to compensate for the dominant center. or: no center speaker used (no center speaker connected)
PANORAMA	only L and R speaker used (creates a surround like effect with only 2 speakers, result is inferior to the combination with the ADAPTIVE mode)

10.3. Further Notes

1. The ADAPTIVE mode seems to get better results compared to the PASSIVE in all cases, even for source signals that are not encoded in Dolby Surround.

2. Using the EFFECT mode for mono signals creates a very dry surround signal. This can be somewhat compensated with the Surround Reverberation Register (0046hex H).

3. For small speaker spacing the perceived basewidth can be increased by using Surround Spatial Effect (Register 0044hex H). This also works best for the ADAPTIVE mode.

4. Surround Spatial Effect can be used in combination with PANORAMA. This also works best for the ADAPTIVE mode.

5. The adaptive input balance is recommended for the ADAPTIVE mode. In PASSIVE or EFFECT mode, the input balance can be switched to manual in middle position.

6. In PANORAMA mode, the strength of the surround signal can be controlled by the Panorama Sound Effect Register (0045hex H). In other modes, this register has no effect and should be set to 0.

10.4. Input and Output Levels for Dolby Pro Logic Operation

The analog inputs are able to accept 2 Vrms input level without overloading any stage before the volume control. The nominal input level (input sensitivity) is 350 mV. This gives 15 dB headroom. The scart prescale value should be set to 0 dB (25_{dec}).

I^2S-inputs should have the same headroom when entering the DPL. The nominal input level is –15 dBFS. The highest possible input level of 0 dBFS is accepted without internal overflow. The I^2S-prescale value should be set to 0 dB (25_{dec}).

With higher prescale values lower input sensitivities can be accommodated. A higher input sensitivity is not possible, because at least 15 dB headroom is required for every input according to the Dolby specifications.

A full-scale left only input (2 Vrms) will produce a full-scale left only output with 0 dB volume. The typical output levels are 1.37 Vrms for channel 1 and 2 and 1.9 Vrms for SCART outputs. The I^2S-channels yield 0 dBFS. The same holds true for right only signals. A full-scale input level on both inputs (Lin=Rin=2 Vrms) will give a center only output with maximum level. The typical output levels are 1.37 Vrms for channel 1 and 2 outputs and 1.9 Vrms for SCART outputs. The I^2S-channels yield 0 dBFS. A full-scale input level on both inputs (but Lin and Rin with inverted phases) will give a surround-only signal with maximum level.

For reproducing Dolby Pro Logic according to its specifications, the center and surround outputs must be amplified by 3 dB with respect to the L and R output signals. This can be done in two ways:

1. By implementing 3 dB more amplification for center and surround loudspeaker outputs.

2. By always selecting volume for L and R 3 dB lower than center and surround. Method 1 is preferable, as method 2 lowers the achievable SNR for left and right signals by 3 dB.

10.5. Dolby Qualification

Qualification testing for Dolby approval requires the device to be switched to plain Dolby Pro Logic without any sound effects. Effects, such as PANORAMA, Surround Spatial Effect or Surround Reverberations must be switched off.

The surround decoder must be switched to ADAPTIVE.

For Dolby Pro Logic designs only 20 ms fixed or 15–30 ms variable delay must be used.

10.6. Phase Relationship of Outputs

The analog output signals channel 1, channel 2 and SCART2 of the DPL all have the same phases. The user does not need to correct output phases when using these analog outputs directly. The SCART1 output has opposite phase.

Using the I^2S-outputs for other DSPs or D/A converters, care has to be taken to adjust for the correct phase. If the attached coprocessor is one of the MSP family, the following schematics help to determine the phase relationship:

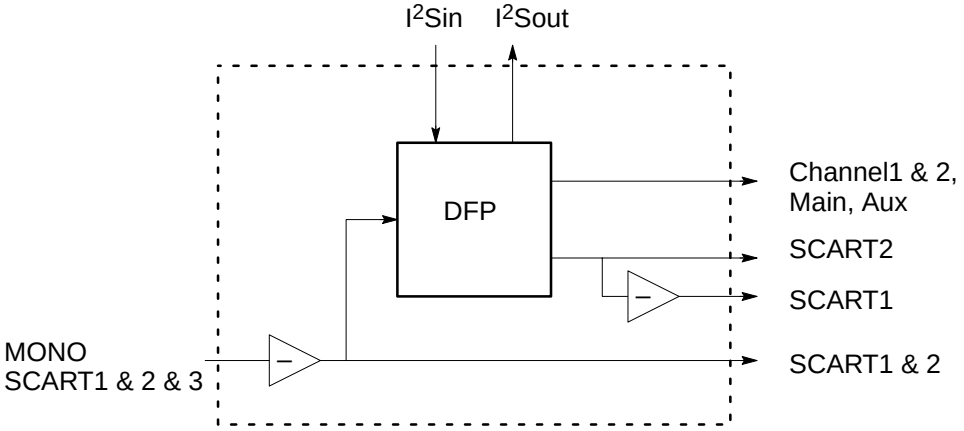


Fig. 10–3: Phase Diagram of DPL, MSPB, MSPC (>c6) and MSPD

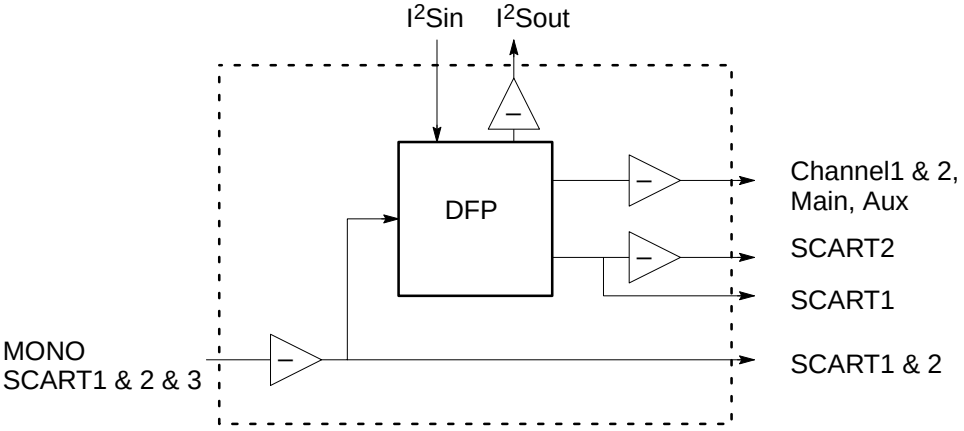


Fig. 10–4: Phase Diagram of MSPC (≦c6)

10.7. Minimum Control Transmissions for the DPL 3520A

The following listing contains the minimum data transfer for setting up the DPL in stand alone mode. The file resets registers even though these registers are already reset by the hardware reset. This is to ensure, that even without external reset, the original state is restored. Note: the trap is the transmission to register 56dez=38hex. This register must not be 0 (which it is after reset). This is mentioned in the data sheet on page 39 (9.1.8. channel source modes). The format of the listing is the same as the log format of our demo software (without the comments). You can create a file with these transmission codes and execute it via our demo software. Use the I2C –> Init from File – menu.

```
16, 131, 0, 38      ! 131=83hex = MODE_REG:
                    ! dig_out, i2s and audioclock out set
                    ! to tristate, i2s master, i2s sony
                    ! mode
18, 0, 103, 0       ! volume channel1 = –12dB
18, 1, 0, 0         ! balance channel1 = 0dB/0dB
18, 2, 0, 0         ! bass channel1 = 0dB
18, 3, 0, 0         ! treble channel1 = 0dB
18, 4, 0, 0         ! loudness channel1 = 0dB
18, 5, 0, 0         ! spat effect channel1 off
18, 6, 103, 0       ! volume channel2 = –12dB
18, 7, 103, 1       ! volume SCART = –12dB
18, 8, 3, 32        ! channel1 source = DOLBYLR,
                    ! matrix = STEREO
18, 9, 4, 32        ! channel2 source = DOLBYCS,
                    ! matrix = STEREO
18, 10, 7, 16       ! SCART source = DOLBYCSUB,
                    ! matrix = SOUNDB (=subwoofer)
18, 13, 29, 0       ! prescale SCART = 29dez
18, 19, 12, 0       ! ACB: SCART2_OUT,
                    ! SCART1_OUT=DA_SCART
                    ! (=subwoofer), DFPin=SCART1_IN
                    ! (=Lt, Rt input to SCART1)
18, 32, 0, 0        ! Tone control = bass/treble
18, 48, 0, 0        ! balance channel2 = 0dB/0dB
18, 49, 0, 0        ! bass channel2 = 0dB
18, 50, 0, 0        ! treble channel2 = 0dB
18, 51, 0, 0        ! loudness channel2 = 0dB
18, 56, 2, 0        ! I2S2 source = SCART !
                    ! although this is not used it must be
                    ! set !
18, 64, 0, 0        ! surround decoder mode =
                    ! ADAPTIVE, Surround
                    ! reproduction mode = NORMAL
18, 65, 2, 32       ! Surround Source = SCART,
                    ! surround source mode = STEREO
18, 66, 18, 0       ! surround delay = 24ms
18, 67, 0, 0        ! surround input balance mode =
                    ! AUTOMATIC
18, 68, 0, 0        ! surround spatial effect = off
18, 69, 0, 0        ! panorama sound effect = off
18, 70, 0, 0        ! surround reverberation = off
```

format:
<16|18>, <adr>, <high byte>, <low byte>

16 means: write transmission to MODEREG
18 means: write transmission to DFP

all values in decimal

11. Application Principle of the DPL 3520A

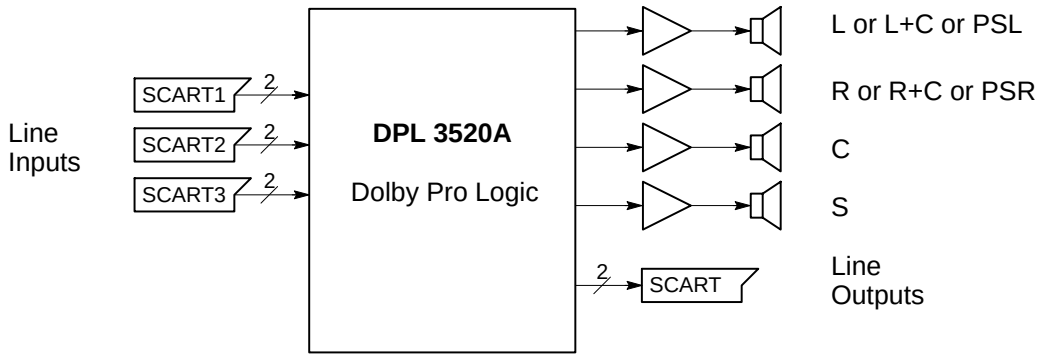
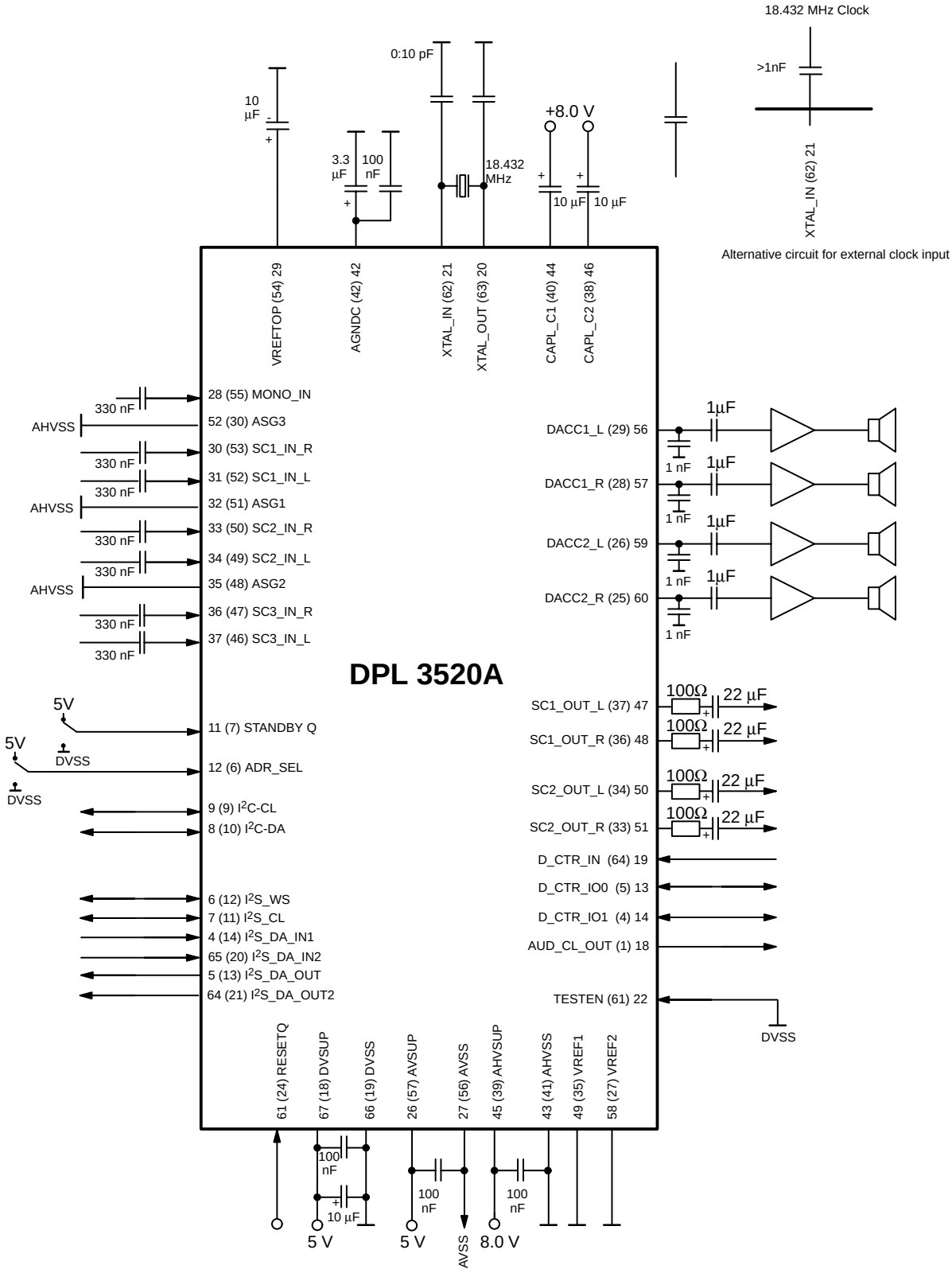


Fig. 11–1: Standard configuration

12. Application Circuit Diagram of the DPL 3520A



Note: Pin numbers refer to the PLCC68 package, numbers in brackets refer to the PSDIP64 package.

13. Dolby Pro Logic Processor Family

13.1. DPL 3518A: Basic Dolby Pro Logic Coprocessor for the MSP Family

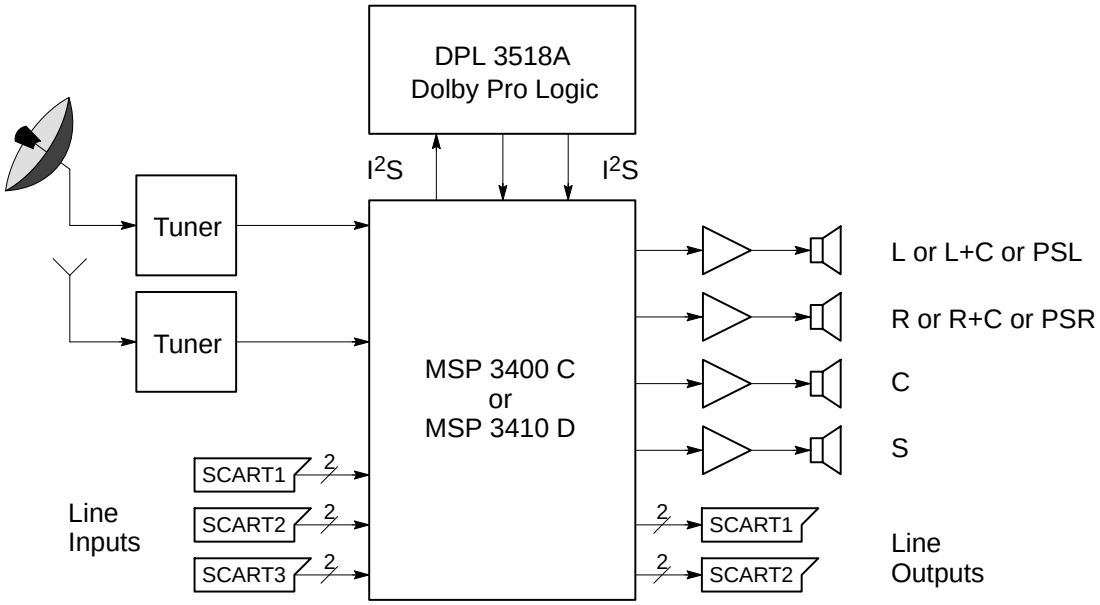


Fig. 13–1: Standard configuration

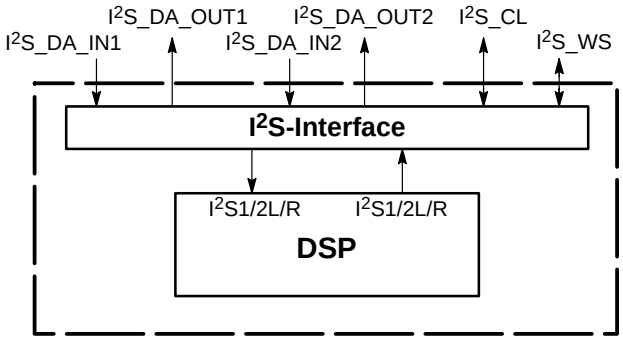


Fig. 13–2: Architecture of the DPL 3518A

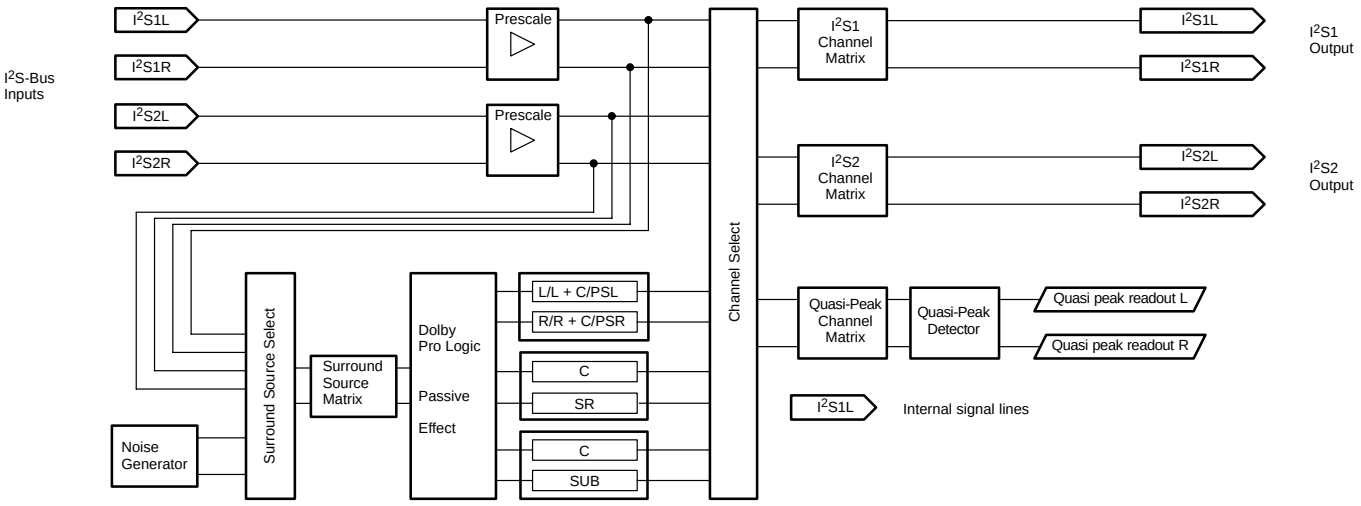


Fig. 13–3: Baseband processing of the DPL 3518A

13.2. DPL 3519A: Advanced Dolby Pro Logic Coprocessor for the MSP Family

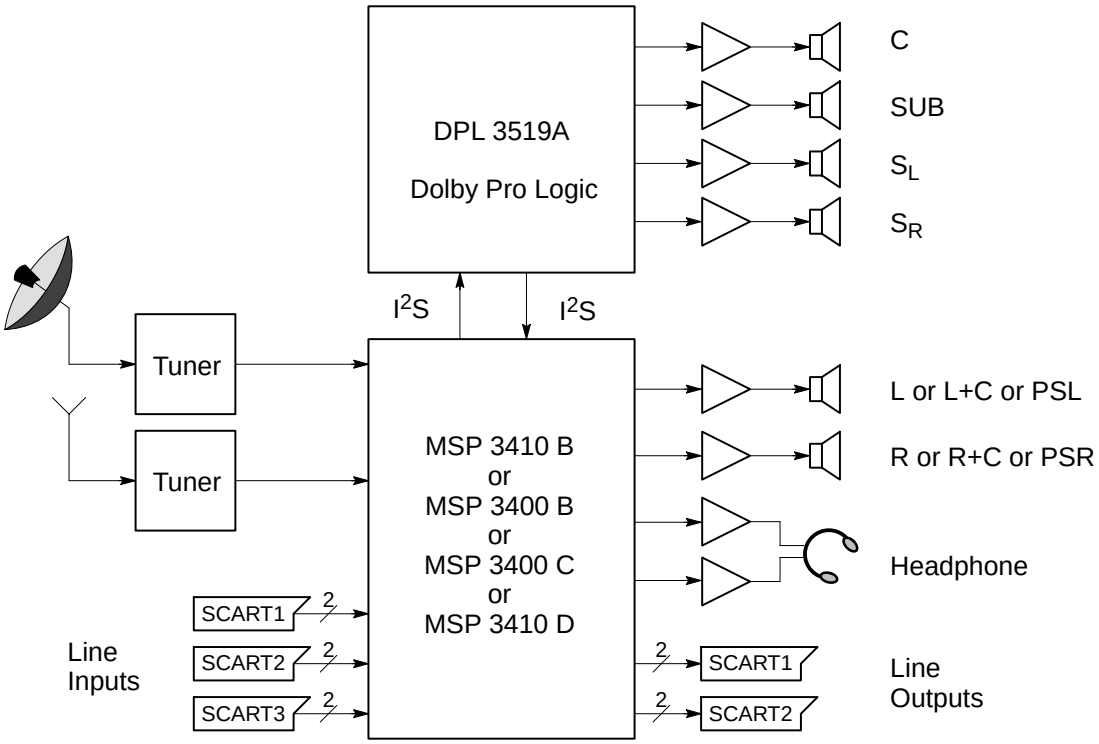


Fig. 13–4: Standard configuration

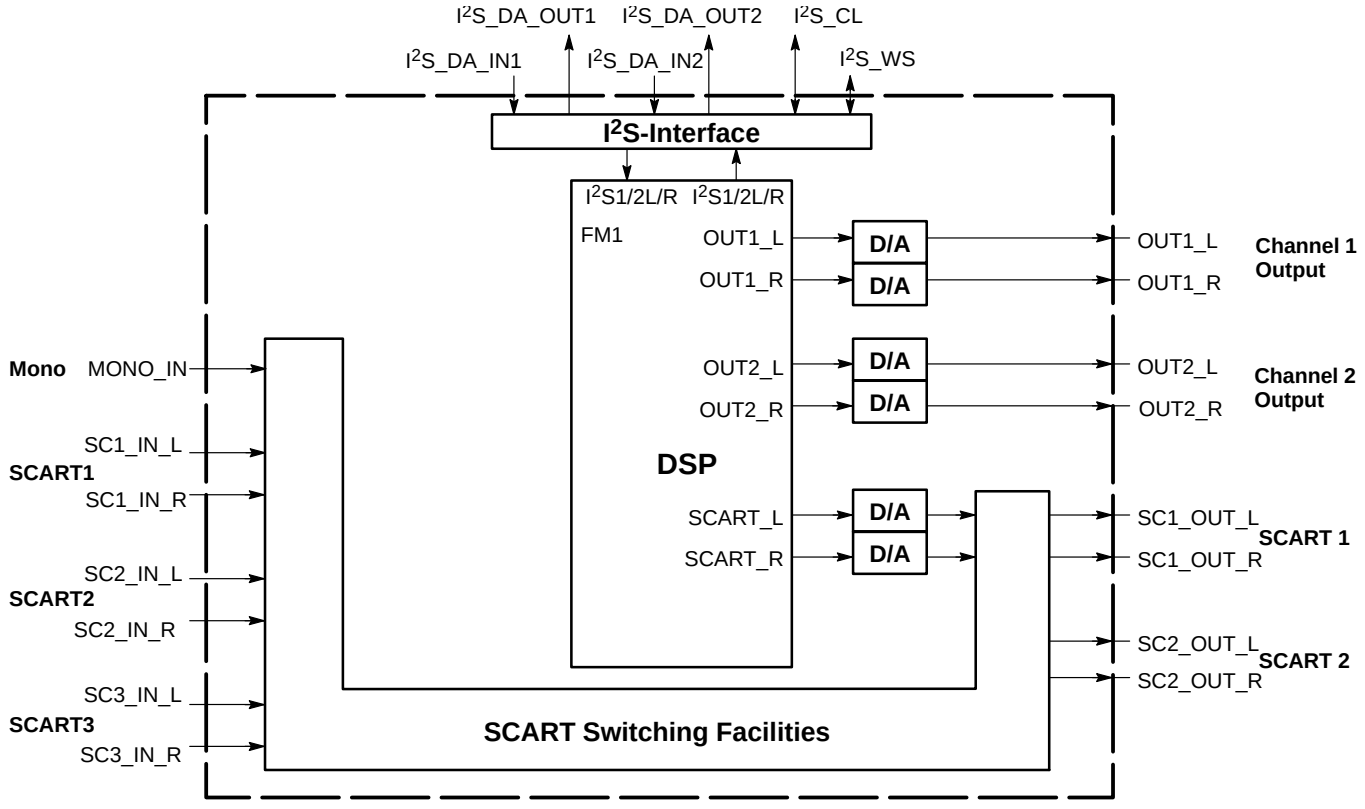


Fig. 13–5: Architecture of the DPL 3519A

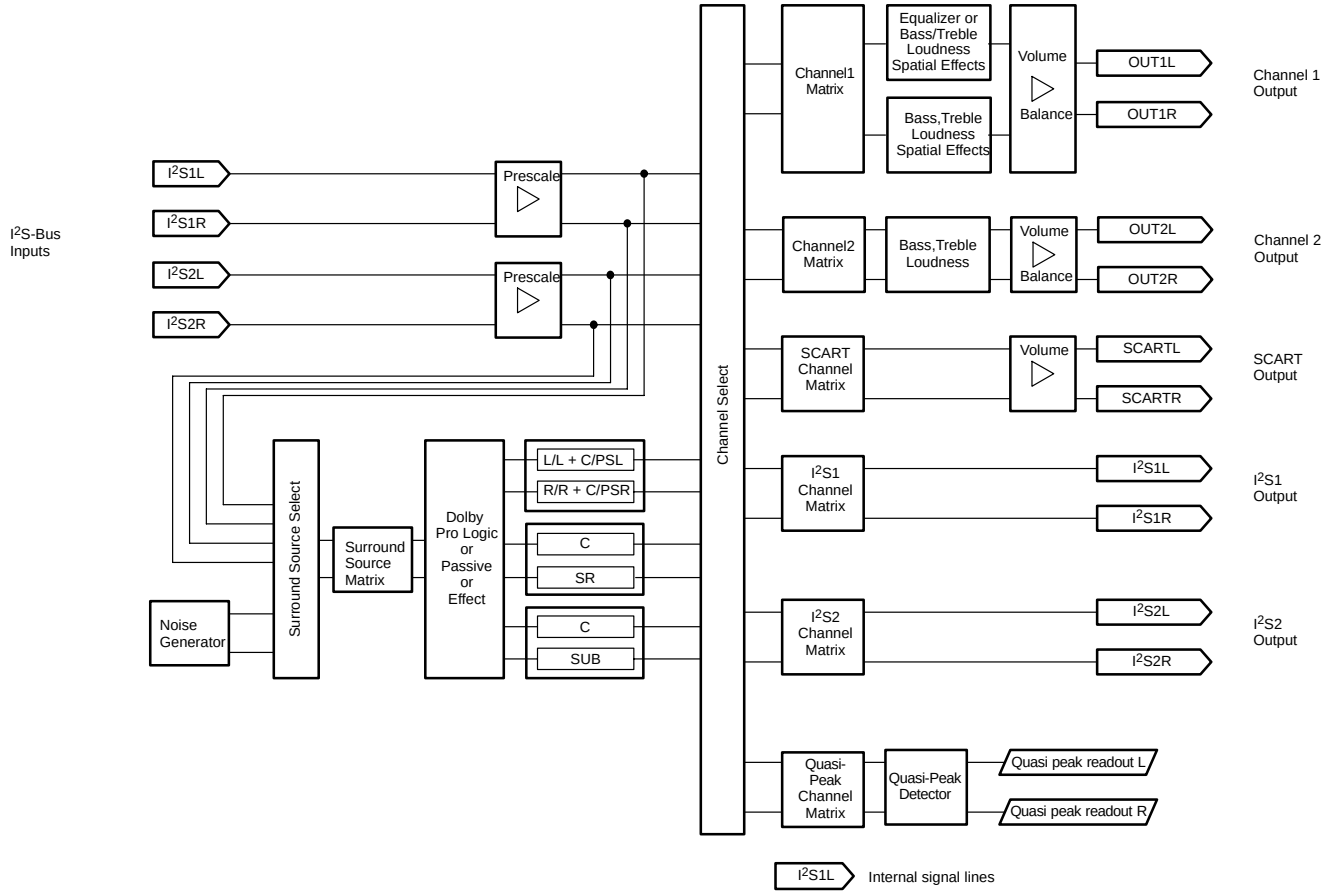


Fig. 13–6: Baseband processing of the DPL 3519A

14. IC Failure Report

Three errors have been detected on the A1 versions of following ICs: DPL 3518A, DPL 3519A, and DPL 3520A.

1. The register for the I^2S2 channel source does not work. Instead of using register 38_{hex}, register $0c_{hex}$ (Quasi peak detector source) is used. So, the I^2S2 source is always the same as the source for the Quasi peak detector. Nevertheless 38_{hex} must be programmed to a value other than the reset state of 00_{hex} (See note in chapter 9.1.8.).

2. If the DPL is used with manual input balance, the lower 4 bits in register 43 must be zero. Only the upper 4 bits can be programmed.

3. The fast mute feature (registers 00hex and 06hex) does not work. Use normal mute instead.

These errors will be corrected with version A2.

15. Data Sheet History

1. Preliminary Data Sheet: “DPL 3520A, DPL 3519A, DPL 3518A Dolby Pro Logic Processor Family”, July 31, 1997, 6251-423-1PD. First release of the preliminary data sheet.

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