National Semiconductor

PRELIMINARY

DP83266 MACSI™ Device (FDDI Media Access Controller and System Interface)

General Description

The DP83266 Media Access Controller and System Interface (MACSI) implements the ANSI X3T9.5 Standard Media Access Control (MAC) protocol for operation in an FDDI token ring and provides a comprehensive System Interface.

The MACSI device transmits, receives, repeats, and strips tokens and frames. It produces and consumes optimized data structures for efficient data transfer. Full duplex architecture with through parity allows diagnostic transmission and self testing for error isolation and point-to-point connections.

The MACSI device includes the functionality of both the DP83261 BMAC™ device and the DP83265 BSI-2™ device with additional enhancements for higher performance and reliability.

Features

- Over 9 kBytes of on-chip FIFO
- 5 DMA channels (2 Output and 3 Input)
- 12.5 MHz to 33 MHz operation
- Full duplex operation with through parity
- Supports JTAG boundary scan
- Real-time Void stripping indicator for bridges
- On-chip address bit swapping capability
- 32-bit wide Address/Data path with byte parity
- Programmable transfer burst sizes of 4 or 8 32-bit words
- Receive frame filtering services
- Frame-per-Page mode controllable on each DMA channel
- Demultiplexed Addresses supported on ABus
- New multicast address matching feature
- ANSI X3T9.5 MAC standard defined ring service options
- Supports all FDDI Ring Scheduling Classes (Synchronous, Asynchronous, etc.)
- Supports Individual, Group, Short, Long and External Addressing
- Generates Beacon, Claim, and Void frames
- Extensive ring and station statistics gathering
- Extensions for MAC level bridging
- Enhanced SBus compatibility
- Interfaces to DRAMs or directly to system bus
- Supports frame Header/Info splitting
- Programmable Big or Little Endian alignment

Block Diagram

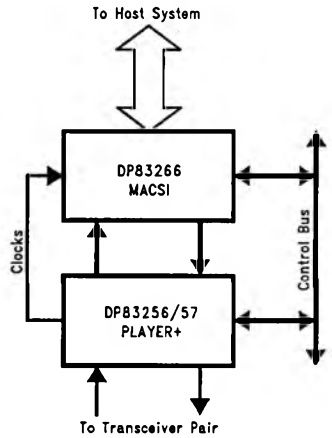

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FIGURE 1-1. FDDI Chip Set Block Diagram