

# DM5445/DM7445 BCD to Decimal Decoders/Drivers

### **General Description**

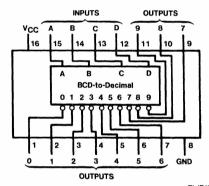
These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10–15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

#### **Features**

- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

# **Connection Diagram**

#### **Dual-In-Line Package**



TL/F/6517-1

Order Number DM5445J, DM5445W or DM7445N See NS Package Number J16A, N16E or W16A

#### **Function Table**

No.	Inputs			Outputs										
	D	С	В	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Τ
1	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
2	L	L	Н	L	Н	Η	L	Н	Н	Н	Н	Н	Н	Н
3	L	L	Н	H	Н	H	Н	L	Н	Н	Н	Н	Н	Н
4	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
5	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Τ
6	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
7	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
8	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
9	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
1	Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
N	н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
V	Н	Н	L	L	н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Α	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	Н	Н	L	Н	Н	Н	Н	Н	Η	Н	Н	Н	Η,
1	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
D						,								

H = High Level (Off), L = Low Level (On)

### **Absolute Maximum Ratings (Note)**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage7VInput Voltage5.5VOutput Voltage30V

Operating Free Air Temperature Range

DM54 −55°C to +125°C DM74 0°C to +70°C Storage Temperature Range −65°C to +150°C Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

### **Recommended Operating Conditions**

Symbol	Parameter	DM5445				Units		
	rarameter	Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	٧
V <sub>IH</sub>	High Level Input Voltage	2			2			٧
VIL	Low Level Input Voltage			0.8			0.8	٧
V <sub>OH</sub>	High Level Output Voltage			30			30	V
loL	Low Level Output Current			20			20	mA
TA	Free Air Operating Temperature	-55		125	0		70	°C

# Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

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Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units	
VI	Input Clamp Voltage	$V_{CC} = Min, I_1 = -12 \text{ mA}$				-1.5	٧	
ICEX	High Level Output Current	$V_{CC} = Min, V_O = 30V$ $V_{IL} = Max, V_{IH} = Min$				250	μΑ	
V <sub>OL</sub>	Low Level Output Voltage	$V_{CC} = Min, I_{OL}$ $V_{IH} = Min, V_{IL} = Min, V_{IL$			0.2	0.4	V	
		$I_{OL} = 80 \text{ mA}$ $V_{CC} = \text{Min}$			0.5	0.9	•	
fį	input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 5.5V$				1	mA	
I <sub>IH</sub>	High Level Input Current	$V_{CC} = Max, V_I = 2.4V$				40	μА	
I <sub>IL</sub>	Low Level Input Current	$V_{CC} = Max, V_1 = 0.4V$				-1.6	mA	
Icc	Supply Current	V <sub>CC</sub> = Max	DM54		43	62	mA.	
		(Note 2)	DM74		43	70		

# **Switching Characteristics** at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	$C_L = 15  pF$ $R_L = 100 \Omega$		49.5	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output			49.5	ns

Note 1: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25$ °C.

Note 2: I<sub>CC</sub> is measured with all inputs grounded and all outputs open.

# **Logic Diagram**

